TI 6130.6

HARDWARE DESIGN DATA (HDD) INSTRUCTION BOOK

FLIGHT DATA INPUT/OUTPUT (FDIO) SYSTEM

VOLUME 1

SECTIONS 1 THROUGH 10

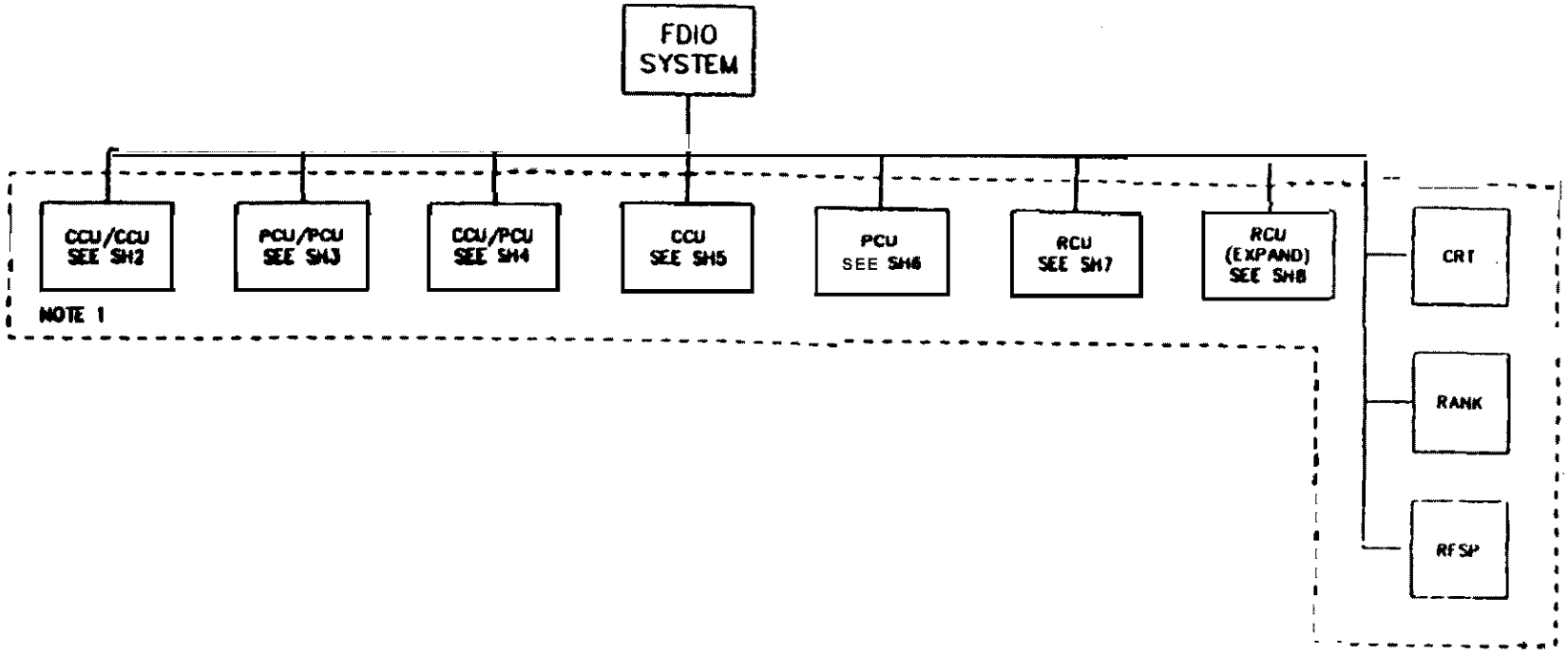
99-0195/05

November 7, 2002

Operational Support
National En Route Automation Division, AOS-300
Federal Aviation Administration
William J. Hughes Technical Center
Atlantic City International Airport, New Jersey 08405

REVISION HISTORY

Level/Revision	*Date*	*CCD/PTR Number*	*Comments*
01	June 1999	N20716 N20442	initial release by the FAA. Refer to Order 6130.1, Chapter 253.
02	March 2000	N21168	Refer to Order 6130.1, Chapter 255.
03	September 2000	N21818 N21601 N19843	Refer to Order 6130.1, Chapter 259.
04	May 2002	N22914 N23047	Refer to SSM-FDIO-001.
05	November 2002	N23645 N23463	Refer to SSM-FDIO-002.



NOTE 1: THE REQUIREMENTS OF THE SITE WILL DETERMINE THE CONFIGURATION OF THE CABINET ASSEMBLIES AND THE PERIPHERAL ELEMENTS USED. SECTION 9 HAS MORE DETAILED INFORMATION OF EACH SITE'S REQUIREMENTS.

FDIO FAMILY TREE (SHEET 1)

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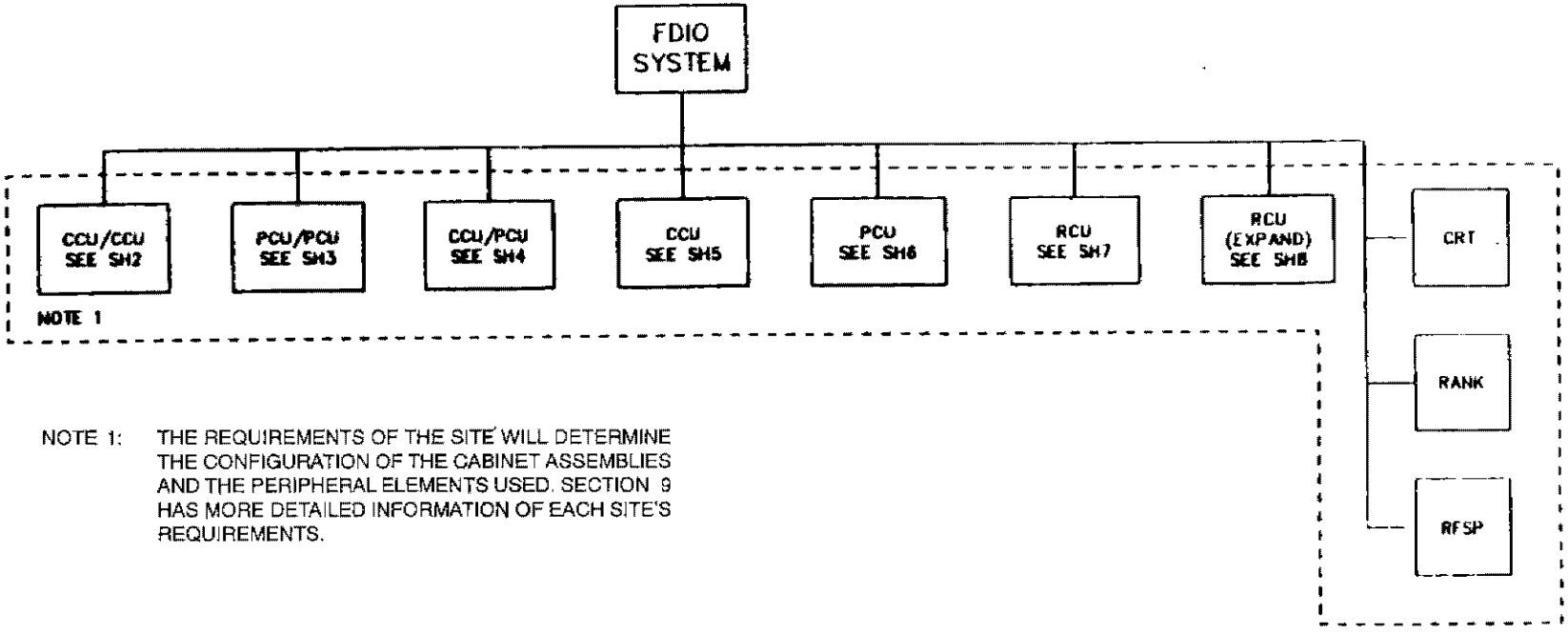
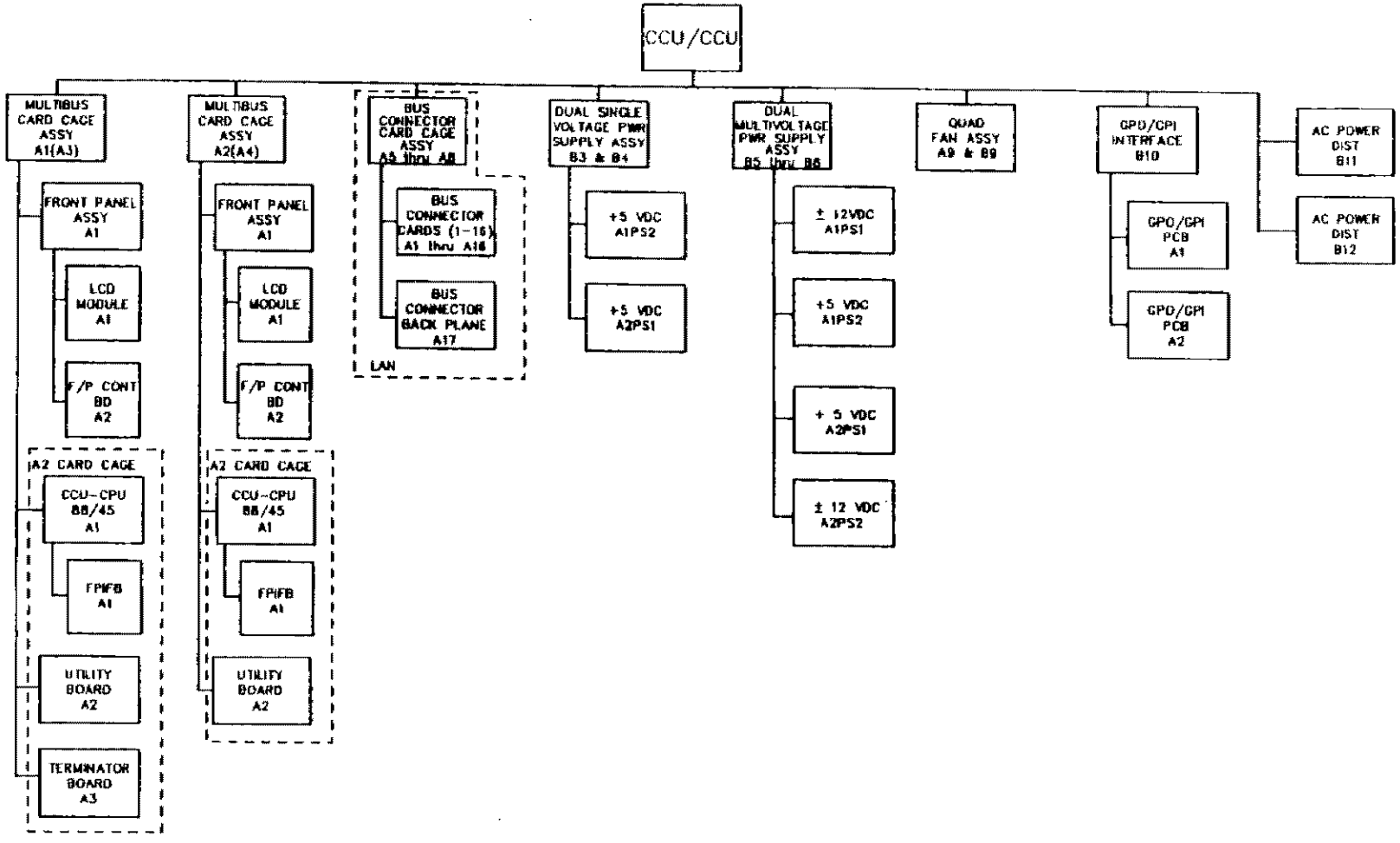


NOTE 1: THE REQUIREMENTS OF THE SITE WILL DETERMINE THE CONFIGURATION OF THE CABINET ASSEMBLIES AND THE PERIPHERAL ELEMENTS USED. SECTION 9 HAS MORE DETAILED INFORMATION OF EACH SITE'S REQUIREMENTS.

FDIO FAMILY TREE (SHEET 1)



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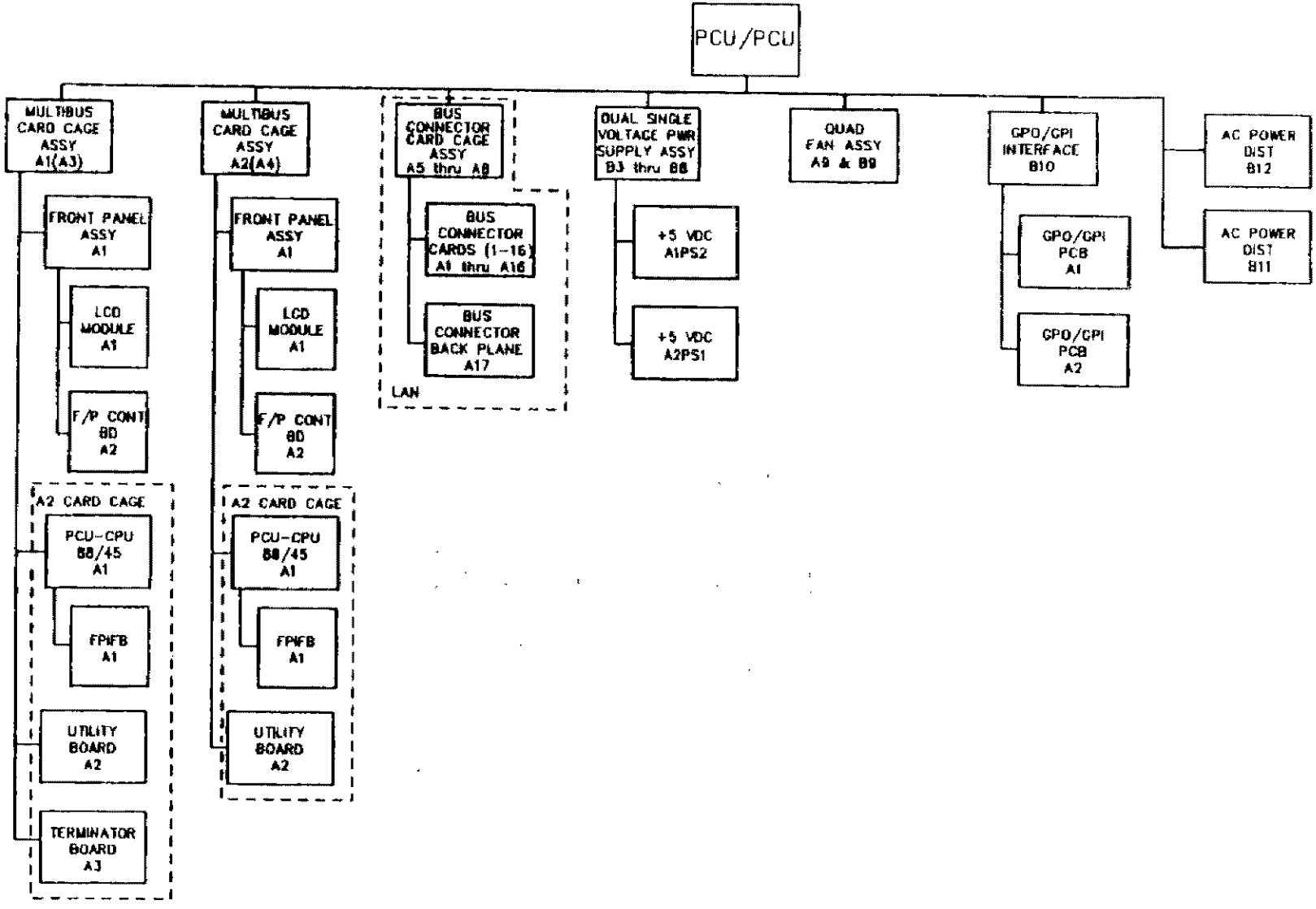

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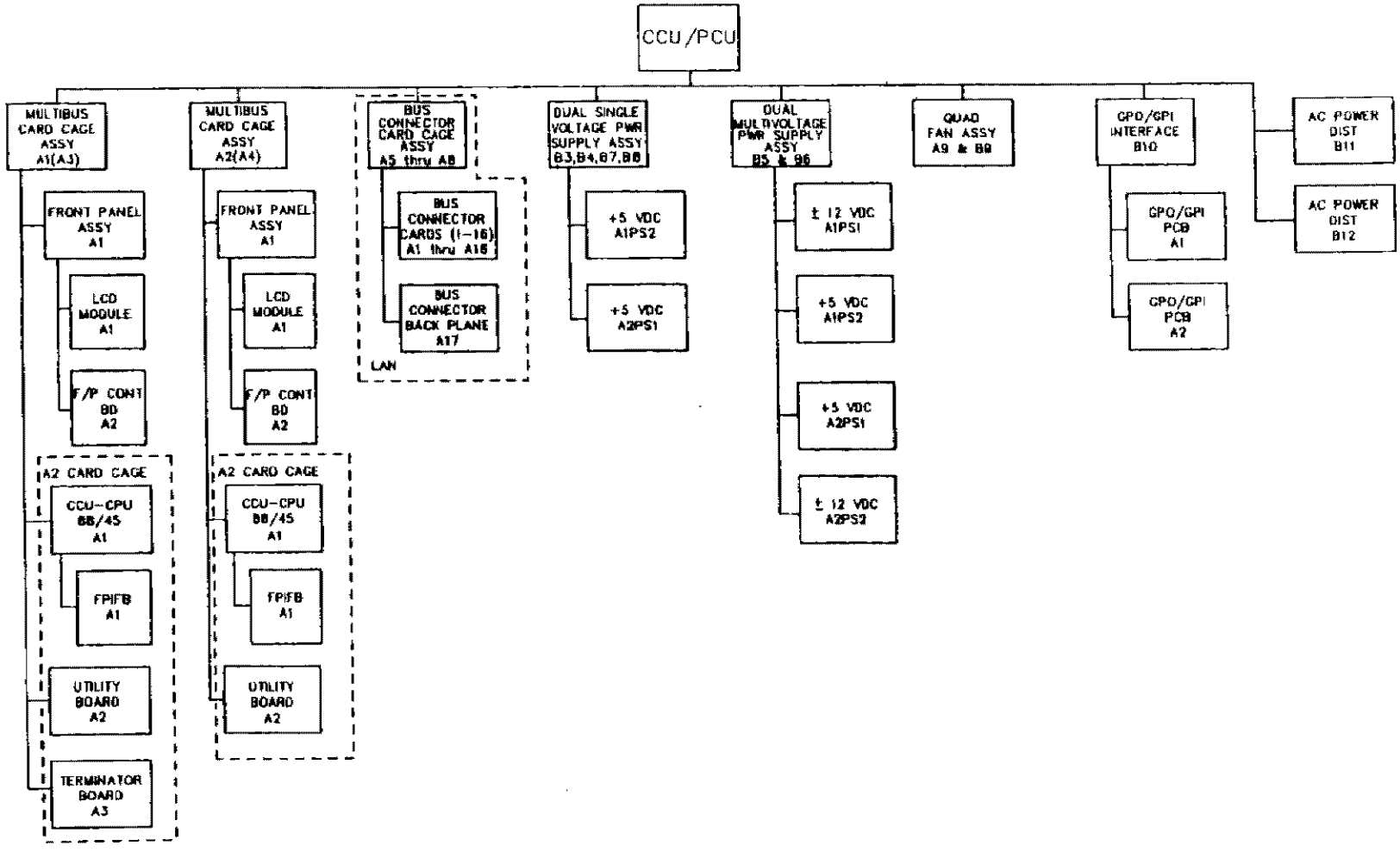

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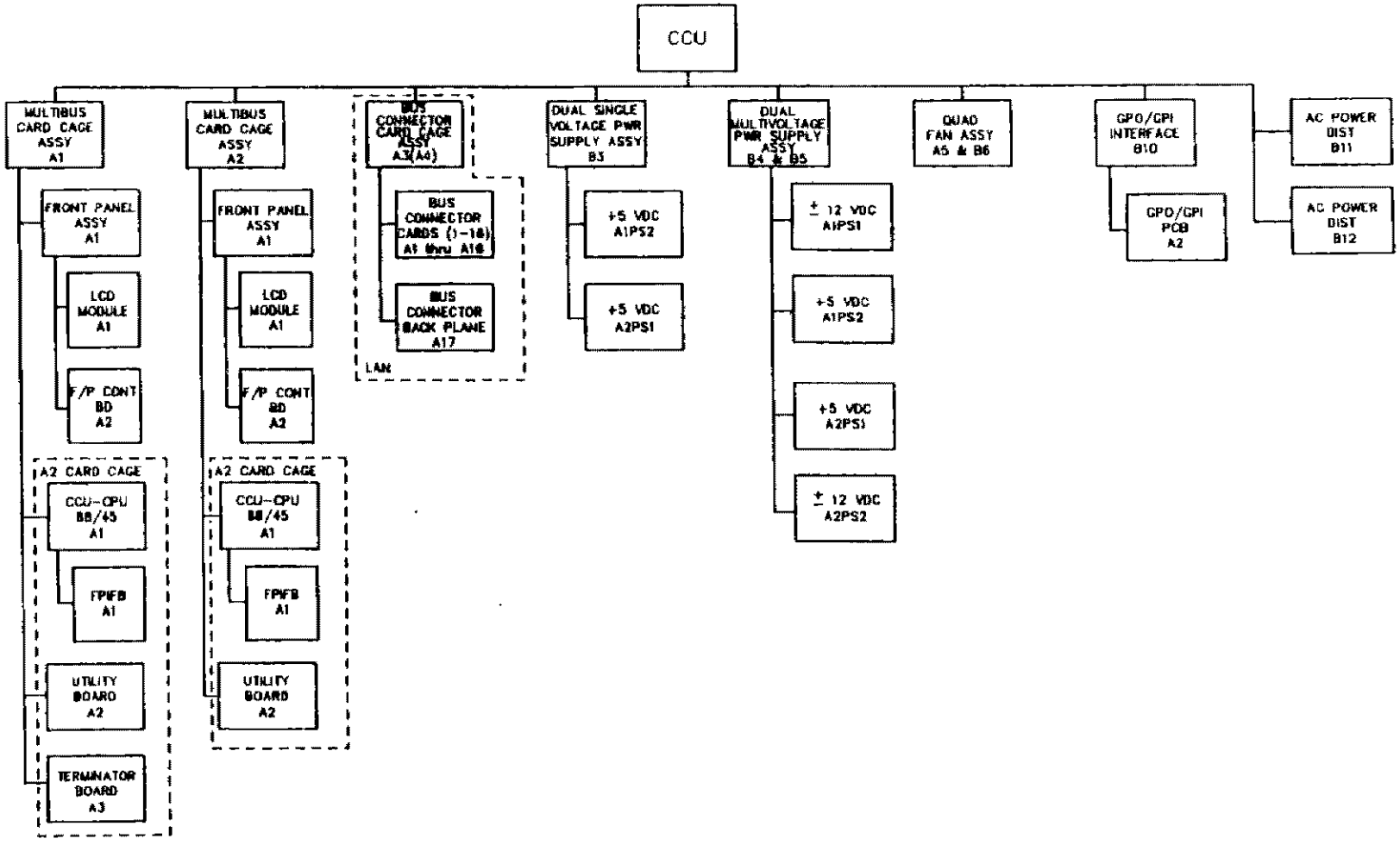

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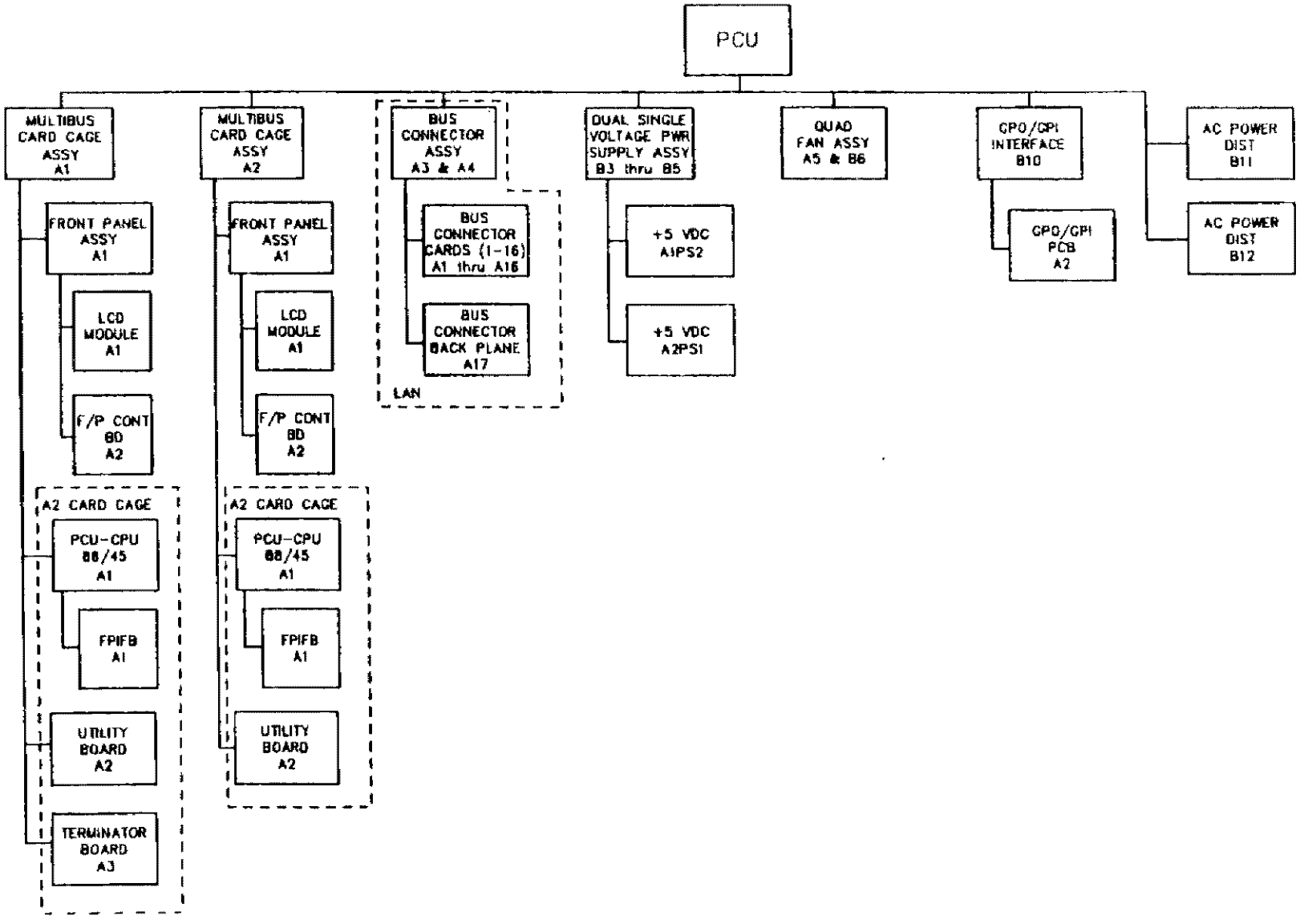

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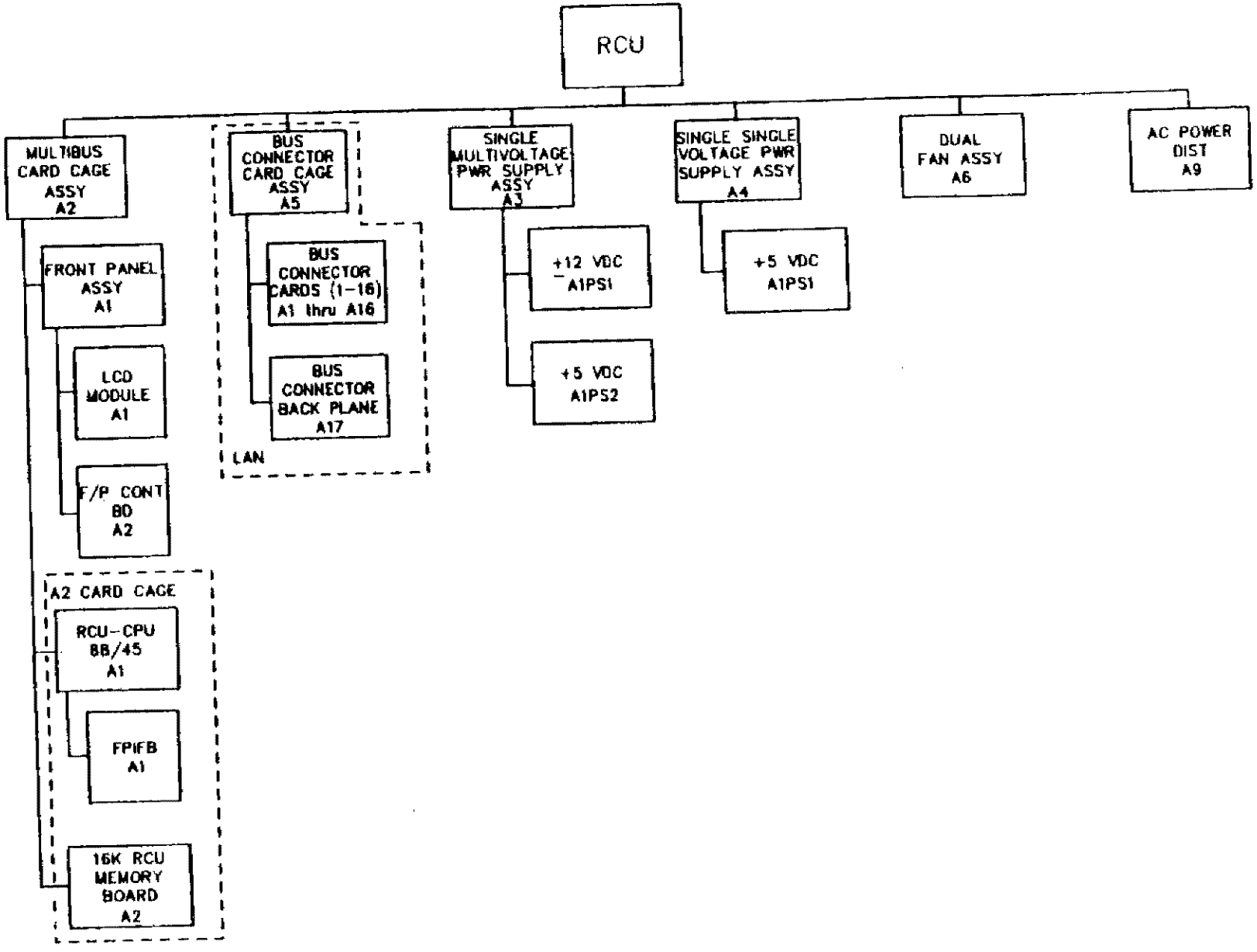
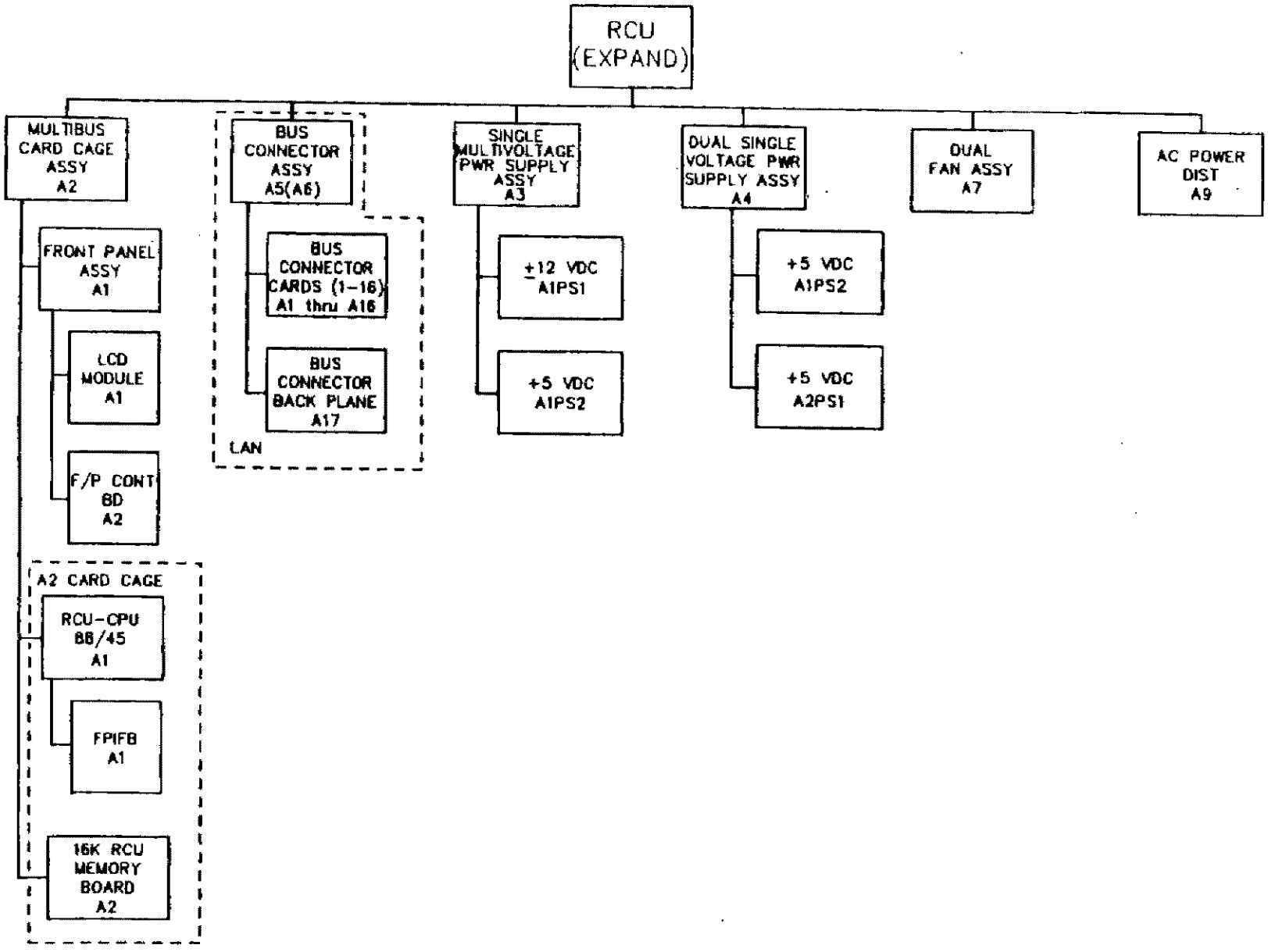


FDIO FAMILY TREE (SHEET 7)



FDIO FAMILY TREE (SHEET 8 — END)

1.0 GENERAL INFORMATION AND REQUIREMENTS

1.1 INTRODUCTION

1.1.1 Purpose

The purpose of the Hardware Design Data (HDD) Instruction Book is to provide guidance to personnel who install, operate, and maintain specific hardware units of the Flight Data Input/Output (FDIO) system equipment.

1.1.2 Scope

The HDD covers general system information, detailed technical descriptions, operation, operating principles, system standards, and periodic preventative and corrective maintenance procedures for the FDIO system. The manual also includes component parts information, installation, integration and check-out information, computer software information and supporting data (such as block diagrams, blocked schematics, and board illustrations), and trouble-shooting flowcharts.

1.1.3 Applicability

The HDD is an instruction and reference document for personnel who install, operate, and maintain the FDIO system. The information in the HDD is applicable to all FDIO system configurations. The manual describes and illustrates the seven possible configurations using various combinations of system control elements within a cabinet. FDIO peripheral elements are also described. The Family Tree in the front matter illustrates the equipment configuration of the FDIO system.

1.1.3.1 Applicable Documents. This paragraph contains reference and supporting documents pertinent to the HDD (FDIO-51B). Originators are as indicated.

a. FDIO Documents are prepared by Federal Systems Group (FSG) Inc., a division of Wespercorp.

1.	FDIO/CLIN-51G1	Overall Computer Program Description (OCPD)
2.	FDIO/CLIN-51G2	Computer Program Functional Specification (CPFS)
3.	FDIO/CLIN-51G3	Software Interface Control Document (SICD)
4.	FDIO/CLIN-51G4	Program Design Specification (PDS)
5.	FDIO/CLIN-51A1	System Design Data Manual (SD)

b. Federal Aviation Administration (FAA) Documents:

1.	FAA-E-2711A	Flight Data Input-Output Specification
2.	FAA-D-2494/B	Technical Instruction Book Manuscripts

1.1.3.2 HDD Organization. The HDD manual is composed of front matter information, 12 major sections, and an appendix of acronyms and abbreviations. The HDD organization is modeled after the outline provided in FAA-D-2494/B, Technical Instruction Book Manuscripts. Titles and descriptions of each section are as follows:

Section	Title and Description
Front Matter	Comprises front cover, revision history, table of contents, list of illustrations, list of tables, and FDIO family tree chart.
1	General Information and Requirements — provides a reference source for determining the purpose, physical and functional characteristics, operational capabilities, and limitations of the equipment.
2	Technical Description — provides a description of the technical details of the equipment.
3	Operation — contains all of the procedures necessary to operate the equipment.
4	Standards and Tolerances — provides lists of equipment parameters, the standard value assigned to each parameter, and the initial and operating tolerances and limits imposed on each standard.
5	Periodic Maintenance — contains performance maintenance checks.
6	Maintenance Procedures — procedures required for various maintenance activities, both periodic and incidental, and associated safety precautions.
7	Corrective Maintenance — contains instructions to diagnose faults, trouble-shoot, repair, and overhaul reparable items.
8	Parts List — contains a list of the descriptive and source data necessary for procurement of all electrical and selected mechanical parts used in the FDIO system.
9	Installation, Integration, and Checkout — contains information directly related to installation, integration, and checkout.
10	Computer Software — includes firmware publication information on the FDIO firmware. User guides and reference manuals for other programs used in the FDIO system are also included.
11	Trouble-shooting Support Data — contains diagrams and other illustrative data for supporting the trouble-shooting and maintenance procedures.
12	Personal Computer-Remote Control Unit (PC-RCU) Replacement — covers general system information, equipment requirements, operation, operating principles, and periodic preventative and corrective maintenance procedures.
A	List of Abbreviations includes definitions of terms, acronyms, and mnemonics.

1.2 EQUIPMENT DESCRIPTION

FDIO distributes flight plan data, weather information, and general information messages between an Air Route Traffic Control Center (ARTCC) Host computer, ARTCC printer peripherals and associated Air Traffic Control Tower (ATCT) remote sites. Those remote sites having Radar Approach Control (RAPCON) and Terminal Radar Control (TRACON) capability are included in the ATCT designation. The FDIO system does not alter the standard operating routine of the ARTCC computer system.

The FDIO replacement system will allow the ATCT remote sites to interface via modems with a Central Control Unit (CCU) at the ARTCC which is connected to the Host via a Peripheral Adapter Module Replacement Item (PAMRI) and a General Purpose Input (GPI) General Purpose Output (GPO) pair. The ARTCC Replacement Flight Strip Printers (RFSP) will interface directly with a Printer Control Unit (PCU) at the ARTCC which is connected to the Host through a PAMRI and GPI/GPO pair.

The FDIO system consists of the following control and peripheral elements:

a. CCU — A control element providing interface between the Host and up to 28 Remote Control Units (RCU) using modems. CCUs are located only at the ARTCC. The CCU consists of the following:

   1. Two Multibus card cage assemblies (-001 and -002). (Assembly 001 has Termination, assembly 002 is without Termination.)

   2. Two Bus Connector (BC) card cage assemblies.

   3. Associated power supplies for Multibus and BC assemblies.

   4. Cabling.

   5. Two (Quad) fan assemblies.

   6. Two alternating current (ac) power distribution assemblies.

NOTE

Two Multibus card cage assemblies are needed to satisfy redundancy requirements. The BC card cage assembly is controlled by the Multibus that is acting as primary.

b. PCU — A control element providing interface between the Host and up to 28 RFSP peripheral elements. PCUs are located only in the ARTCC. The PCU consists of the following:

   1. Two Multibus card cage assemblies (-003 and -004). (Assembly 003 has termination, assembly 004 is without Termination.)

   2. Two BC card cage assemblies.

   3. Associated power supplies for Multibus and BC assemblies.

   4. Cabling.

   5. Two (Quad) fan assemblies.

   6. Two ac power distribution assemblies.

NOTE

Two Multibus card cage assemblies are needed to satisfy redundancy requirements. The BC card cage assembly is controlled by the Multibus that is acting as primary.

c. RCU — A control element which receives signals from the modem connected to the CCU at the ARTCC. The RCU routes these signals to RFSP, Replacement Alphanumeric Keyboard (RANK), and Cathode Ray Tube (CRT) elements through serial channels. RCUs are located only at remote sites. The RCU consists of the following:

1. One Multibus card cage assembly (-005).

NOTE

There is no redundancy in the RCU.

2. One BC card cage assembly. (RCU Expanded contains two BC card cage assemblies.)
3. Associated power supplies for Multibus and BC assembly.
4. Cabling.
5. One dual fan assembly.
6. AC power distribution assembly.

d. RFSP — Peripheral element replacing the existing enroute and terminal printers. Printers provide printout of flight strip messages at the ARTCC and ATCT remote sites; in addition, they print pertinent flight data, echo locally composed FDIO messages, or log error messages at the ARTCC and ATCT remote sites.

e. CRT — Peripheral element used to display flight strip messages, general information messages, weather data, and a composition and editing area for FDIO messages. CRTs are located only at ATCT sites.

f. RANK — Peripheral element used to provide operator interface for Host FDIO message entry. RANKs are located only at ATCT sites.

g. Modulator-Demodulator (modem) — Government Furnished Equipment (GFE) element used to provide communication between ARTCC CCUs and ATCT RCUs. Modems use in-place telephone transmission lines to link sites. Located at ARTCC and ATCT.

The control elements are grouped into a cabinet assembly according to the site equipment configuration. CCU and PCU cabinet assemblies will always be located at the central ARTCC sites. RCU cabinet assemblies will be located only in ATCT remote sites.

Each CCU and PCU control element communicates with the Host through the GPI/GPO pair. The FDIO control elements communicate with their associated peripheral elements through the BCs located in the control cabinets.

1.2.1 FDIO Configuration Differences

Significant differences between the control cabinet configurations are outlined in table 1-1. This table lists the number of Multibus assemblies, BC card cage assemblies, power supplies, ac power distribution

assemblies, and fan assemblies in each configuration. Other differences in the configuration makeup are called out in Paragraph 1.3.1, Cabinet Assembly Configuration.

TABLE 1-1. FDIO SYSTEM CONFIGURATIONS

Control Cabinet Config.	Multibus Assys.	BC Card Cage Assys.	Power Supply Assys.	AC Power Distrib. Assys.	Fan Assys.
CCU/CCU	4 (two 001 & two 002)	4	6	2	2
PCU/PCU	4 (two 003 & two 004)	4	6	2	2
CCU/PCU	4 (one 001, one 002, one 003, & one 004)	4	6	2	2
CCU	2 (one 001 & one 002)	2	3	2	2
PCU	2 (one 003 & one 004)	2	3	2	2
RCU	1 (one 005)	1	2	1	1
RCU Expanded	1 (one 005)	2	2	1	1

1.3 RELATIONSHIP OF UNITS

The relationship of the control and peripheral elements is illustrated in figure 1-1. Information to be sent from the Host to remote groups is communicated to the CCU control element and sent via a modem to the modem connected to the RCU at the remote site. Data being sent from the remote site to the ARTCC is received at the CCU cabinet assembly via the modem from the remote site. That data is then communicated to the Host through the GPI/GPO pair in the PAMRI. CCU cabinet assemblies can communicate with up to 28 modems, each modem communicating with a modem connected to the RCU control cabinet. CCU/CCU cabinet assemblies can communicate with up to 56 modems.

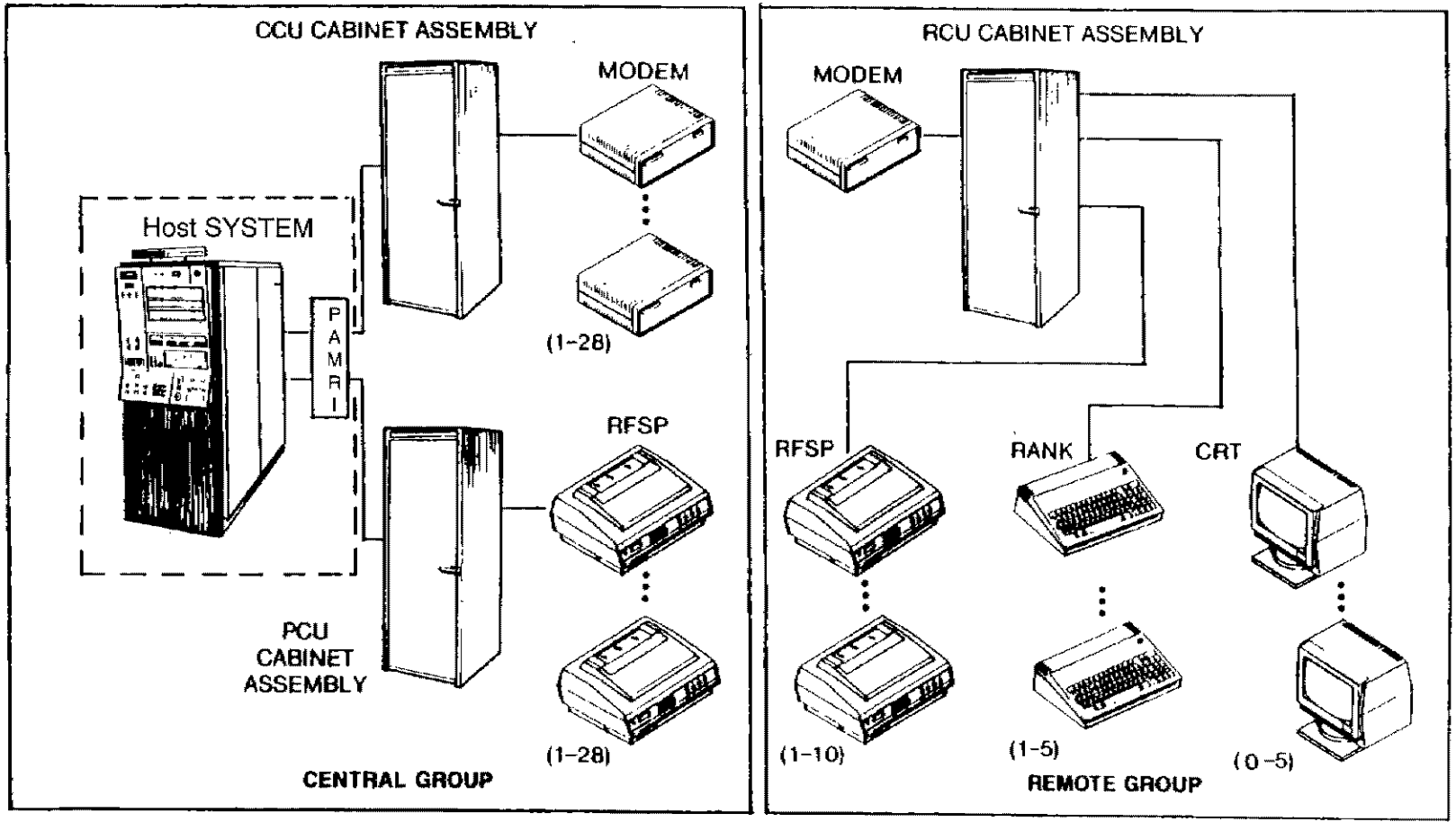


FIGURE 1-1. RELATIONSHIP BETWEEN CONTROL AND PERIPHERAL ELEMENTS

Data received at the RCU cabinet assembly is channeled through BCs to a peripheral RFSP or CRT element for display. Controllers at the remote sites may send data to or request data from the Host through a RANK.

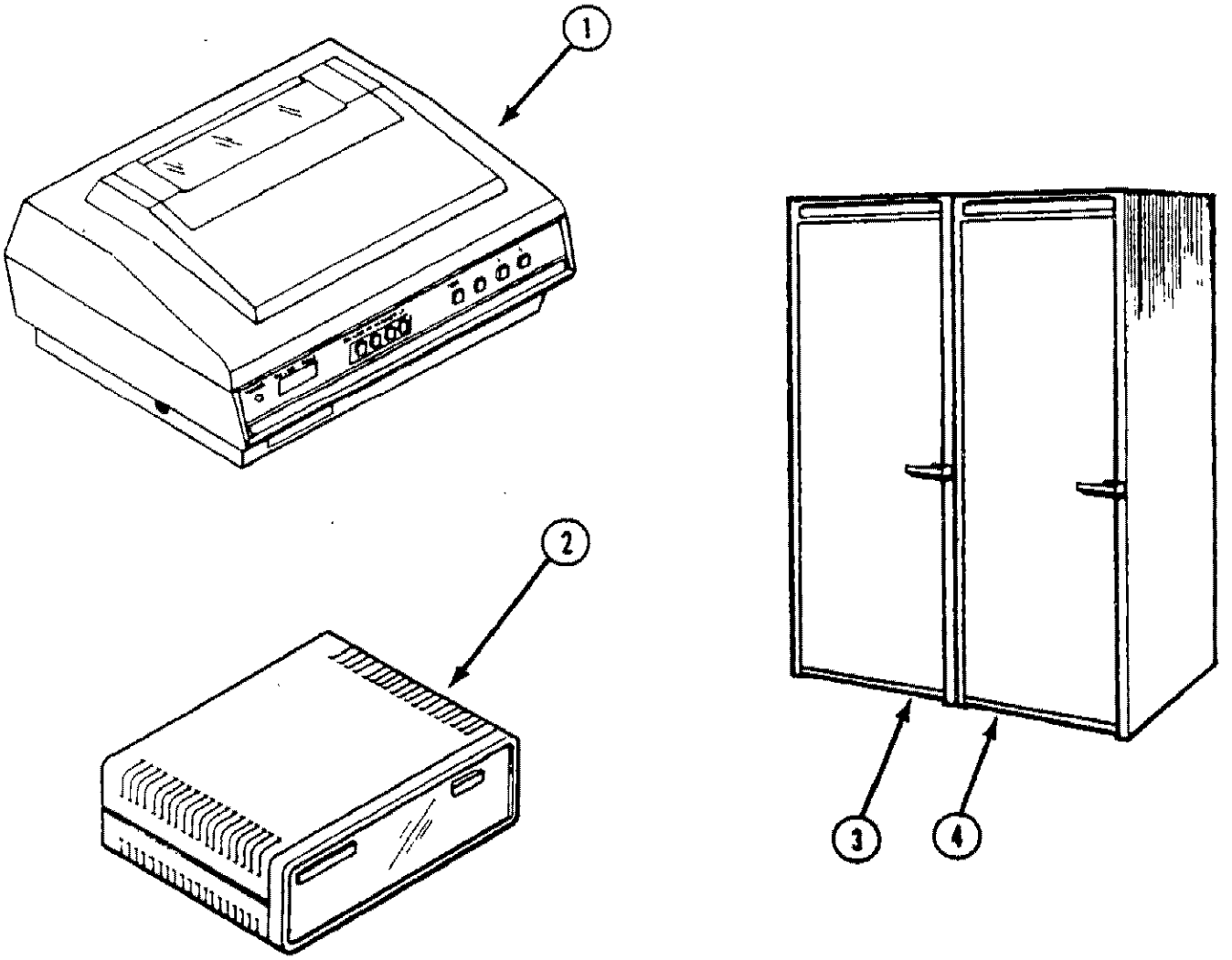
PCU cabinet assemblies at the ARTCC drive up to 28 RFSP peripheral elements located in the ARTCC. A PCU/PCU cabinet assembly can communicate with up to 56 RFSP peripheral units.

Control elements for the FDIO system are supplied in seven cabinet configurations as shown in the FDIO Family Tree (see front matter). Each configuration is housed in a single cabinet assembly. Configurations used in the ARTCC locations are: CCU/CCU, PCU/PCU, CCU/PCU, CCU, and PCU. Configurations used in the ATCT remote sites are: RCU and RCU Expanded. The RCU Expanded configuration contains an additional BC card cage assembly for communicating with additional FDIO peripherals.

Typical makeup of a central group includes any CCU and PCU configuration communicating with the Host. CCU cabinet assemblies will use one modem per remote site communication. PCU cabinet assemblies communicate with ARTCC printer peripheral elements. These printers are the only FDIO peripheral elements to be included with ARTCC operations. Figure 1-2 shows an example of typical control cabinet assemblies (CCU and PCU) and peripheral elements located at an ARTCC.

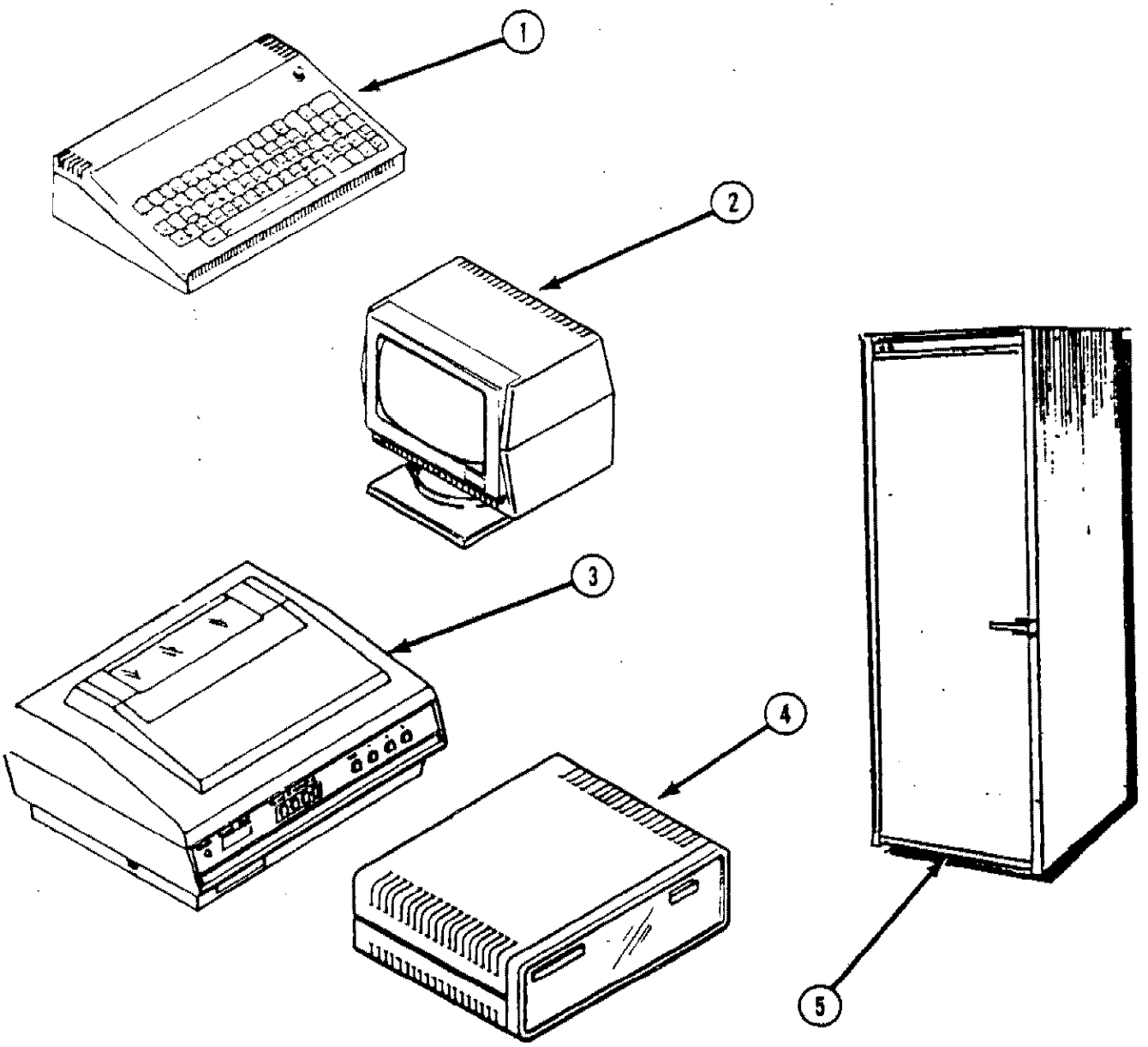
Typical makeup of a remote group will include at least one RCU configuration, 1 to 10 RFSP peripheral elements, 1 to 5 RANK peripheral elements, and 0 to 5 CRT peripheral elements.

Only 14 peripheral elements are allowed with the standard RCU cabinet assembly with the requirement in the contract to have a spare slot and a maintenance slot. The expanded RCU will enable operation of up to the maximum amount of 20 peripherals called out in the contract (10 RFSPs, 5 CRTs, and 5 RANKs). Figure 1-3 shows an example of a typical RCU cabinet assembly and peripheral elements located at an ATCT remote site.



1 — RFSP
2 — MODEM
3 — PCU CABINET ASSEMBLY
4 — CCU CABINET ASSEMBLY

FIGURE 1-2. ARTCC TYPICAL EQUIPMENT TYPES



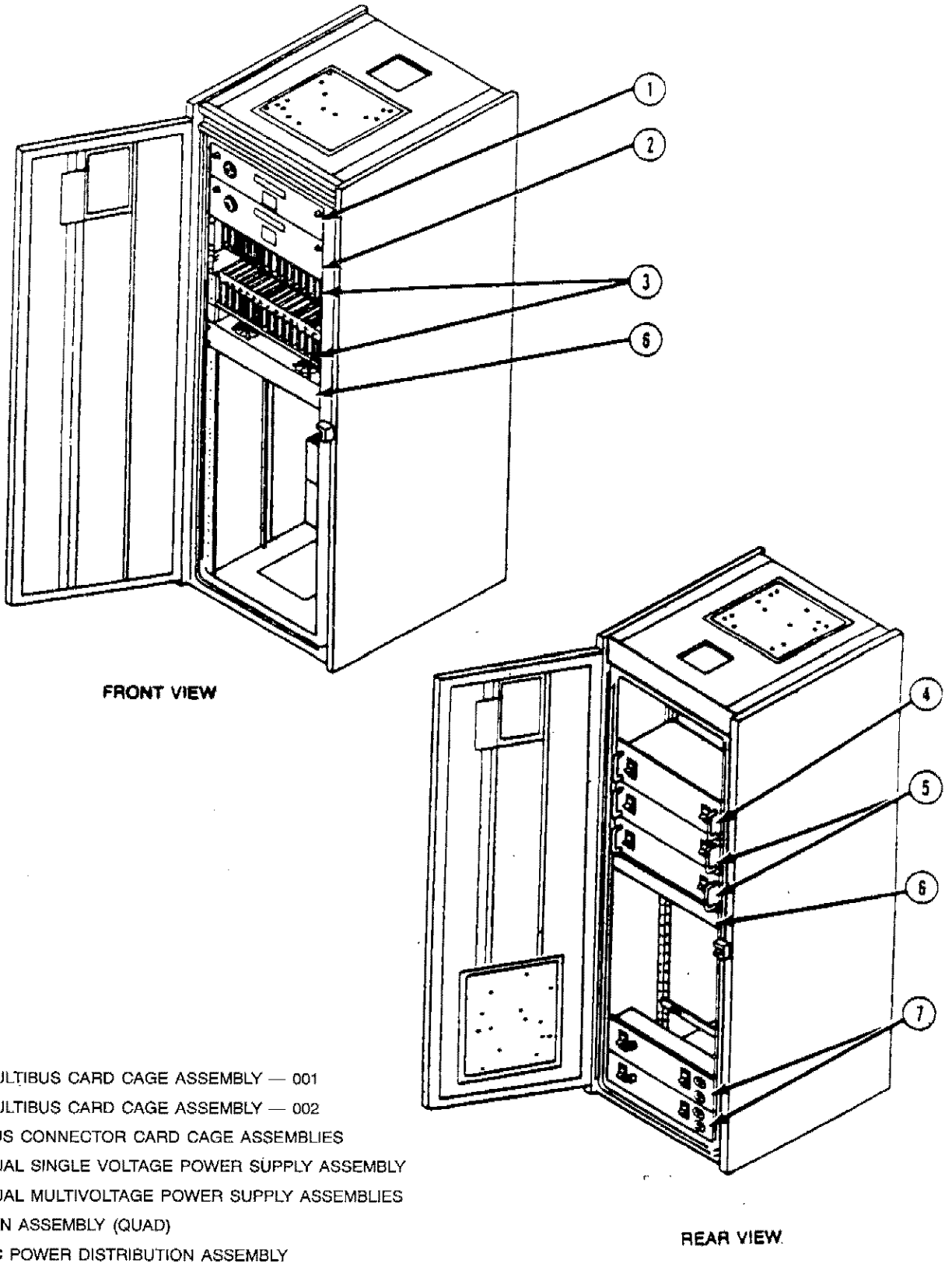
1 — RANK
2 — CRT
3 — RFSP
4 — MODEM
5 — RCU CABINET ASSEMBLY

FIGURE 1-3. ATCT REMOTE SITE TYPICAL EQUIPMENT TYPES

1.3.1 Cabinet Assembly Configuration

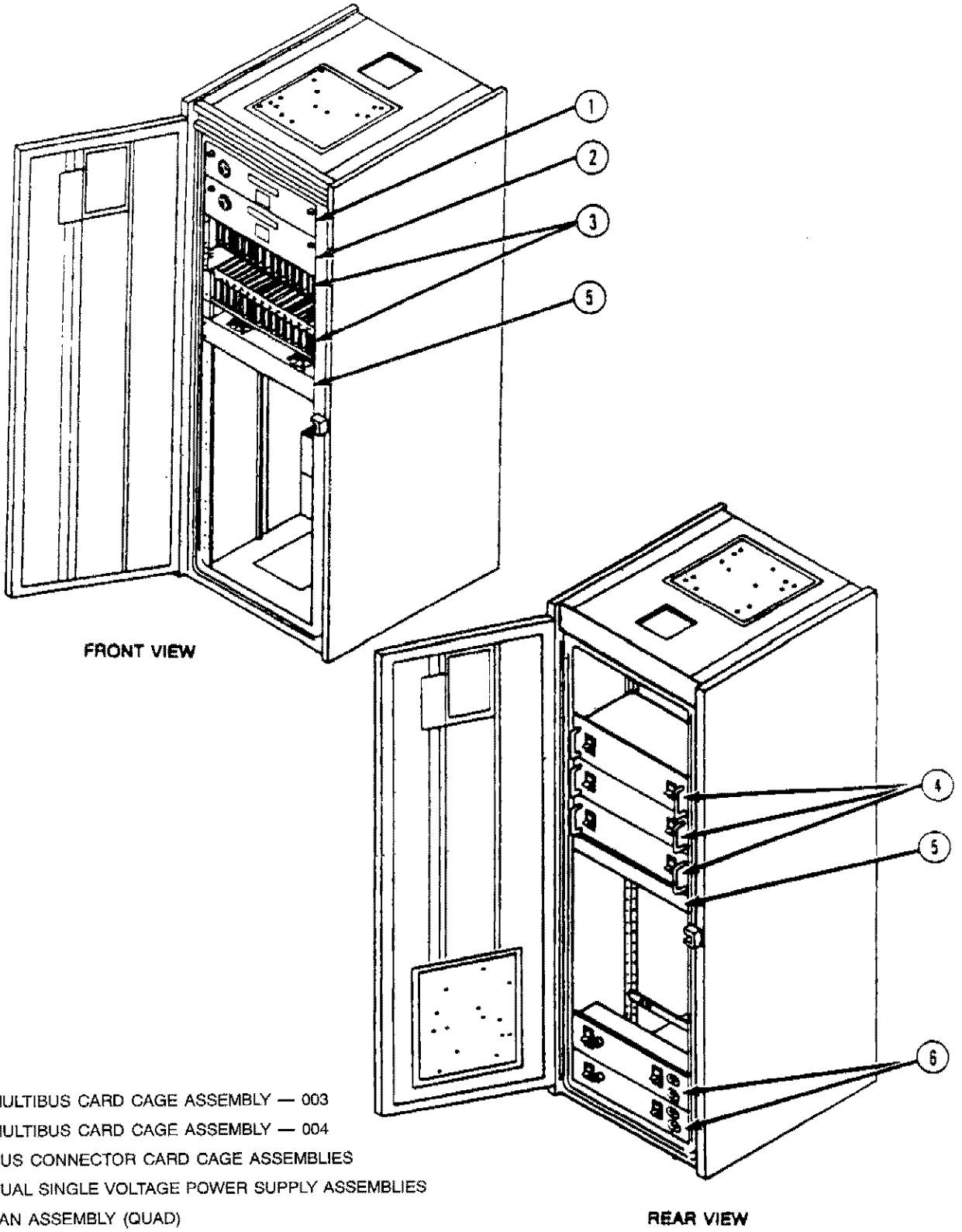
FDIO hardware and firmware modules were designed to be universally functional in any of the seven configurations. This approach simplifies maintenance and configuration management of the system. The control cabinet assembly configurations are described and illustrated as follows:

a.	CCU Cabinet Configuration	Contains two CCU Multibus assemblies, two BC card cage assemblies, one dual single voltage power supply assembly, two dual multivoltage power supply assemblies, two quad fan assemblies, and two ac power distribution assemblies (figure 1-4).
b.	PCU Cabinet Configuration	Contains two PCU Multibus assemblies, two BC card cage assemblies, three dual single voltage power supply assemblies, two quad fan assemblies, and two ac power distribution assemblies (figure 1-5).
c.	RCU Cabinet Configuration	Contains one RCU Multibus assembly, one BC card cage assembly, one single multivoltage power supply assembly, one single single voltage power supply assembly, one dual fan assembly, and one ac power distribution assembly (figure 1-6).
d.	CCU/CCU Cabinet Configuration	Contains four CCU Multibus assemblies, four BC card cage assemblies, two dual single voltage power supply assemblies, four dual multivoltage power supply assemblies, two quad fan assemblies, and two ac power distribution assemblies (figure 1-7).
e.	PCU/PCU Cabinet Configuration	Contains four PCU Multibus assemblies, four BC card cage assemblies, six dual single voltage power supply assemblies, two quad fan assemblies, and two ac power distribution assemblies (figure 1-8).
f.	CCU/PCU Cabinet Configuration	Contains four Multibus assemblies (two CCU and two PCU), four BC card rack assemblies, four dual single voltage power supply assemblies, two dual multivoltage power supply assemblies, two quad fan assemblies, and two ac power distribution assemblies (figure 1-9).
g.	RCU, Expanded Cabinet Configuration	Contains one Multibus assembly, two BC card rack assemblies, one single multivoltage power supply assembly, one dual single voltage power supply assembly, one dual fan assembly, and one ac power distribution assembly (figure 1-10).



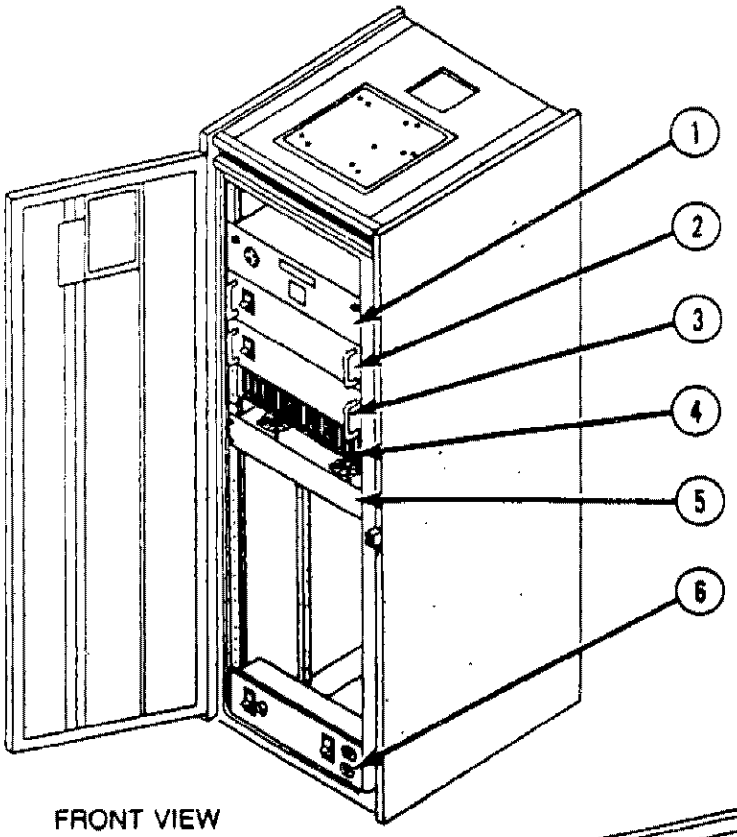
1. MULTIBUS CARD CAGE ASSEMBLY — 001
2. MULTIBUS CARD CAGE ASSEMBLY — 002
3. BUS CONNECTOR CARD CAGE ASSEMBLIES
4. DUAL SINGLE VOLTAGE POWER SUPPLY ASSEMBLY
5. DUAL MULTIVOLTAGE POWER SUPPLY ASSEMBLIES
6. FAN ASSEMBLY (QUAD)
7. AC POWER DISTRIBUTION ASSEMBLY

FIGURE 1-4. CCU CABINET CONFIGURATION

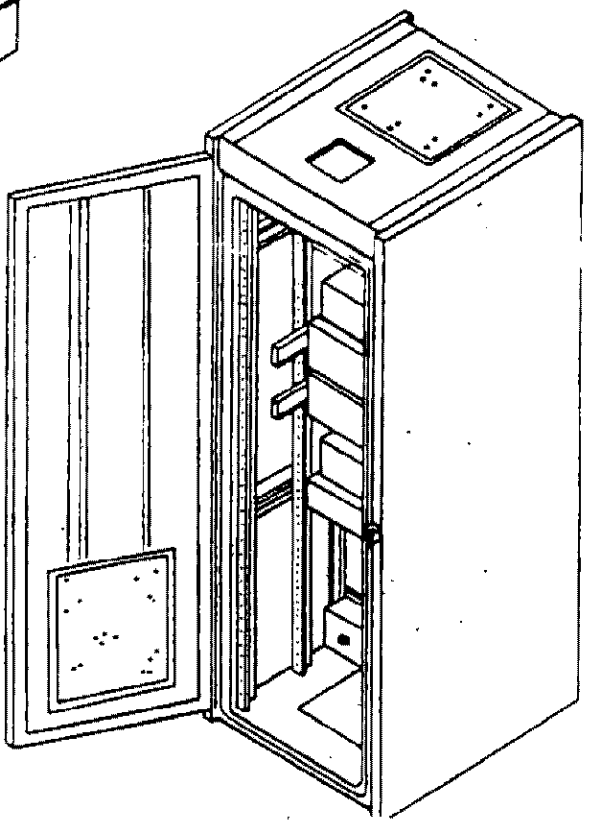


1. MULTIBUS CARD CAGE ASSEMBLY — 003
2. MULTIBUS CARD CAGE ASSEMBLY — 004
3. BUS CONNECTOR CARD CAGE ASSEMBLIES
4. DUAL SINGLE VOLTAGE POWER SUPPLY ASSEMBLIES
5. FAN ASSEMBLY (QUAD)
6. AC POWER DISTRIBUTION ASSEMBLIES

FIGURE 1-5. PCU CABINET CONFIGURATION



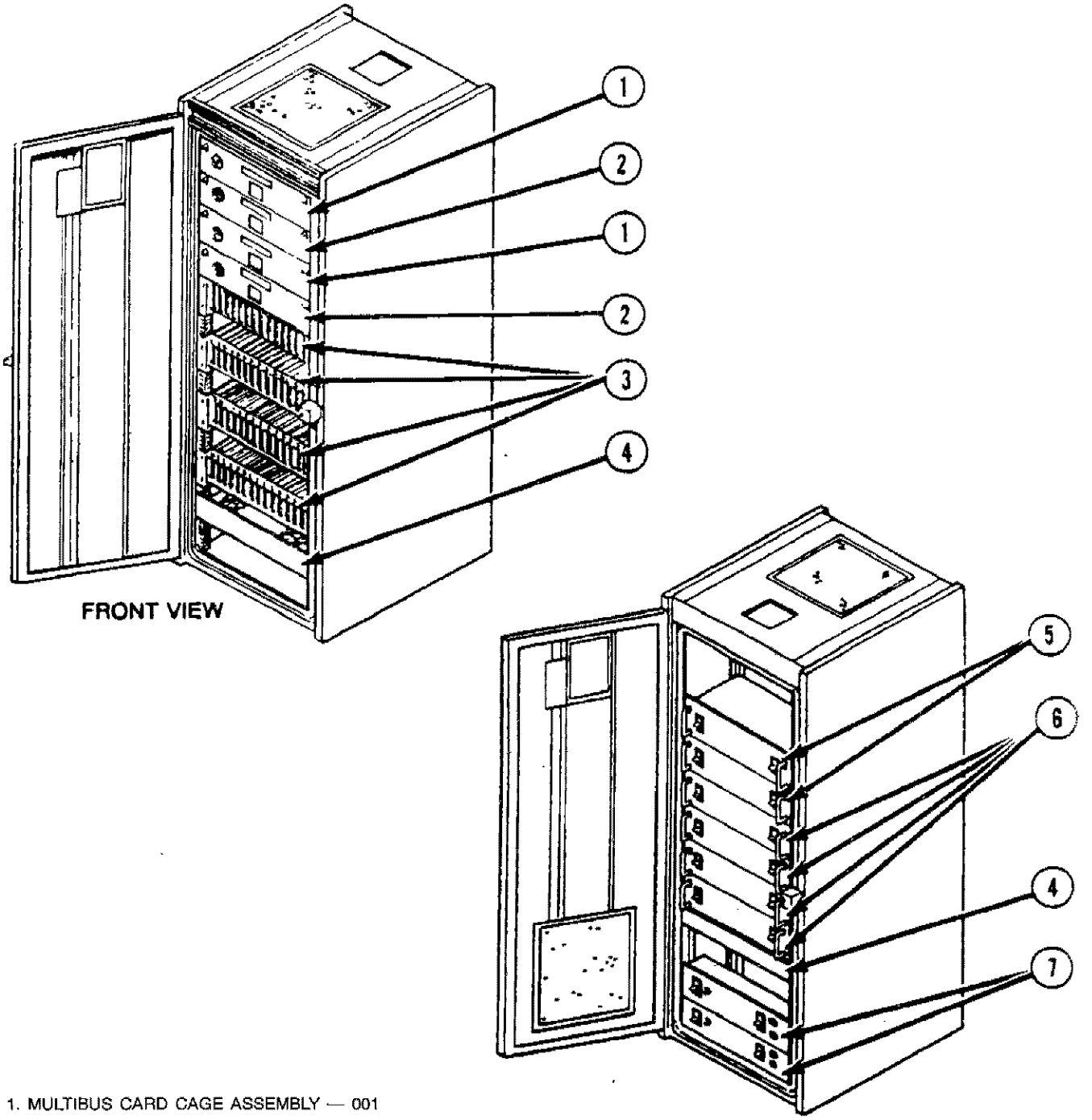
FRONT VIEW



REAR VIEW

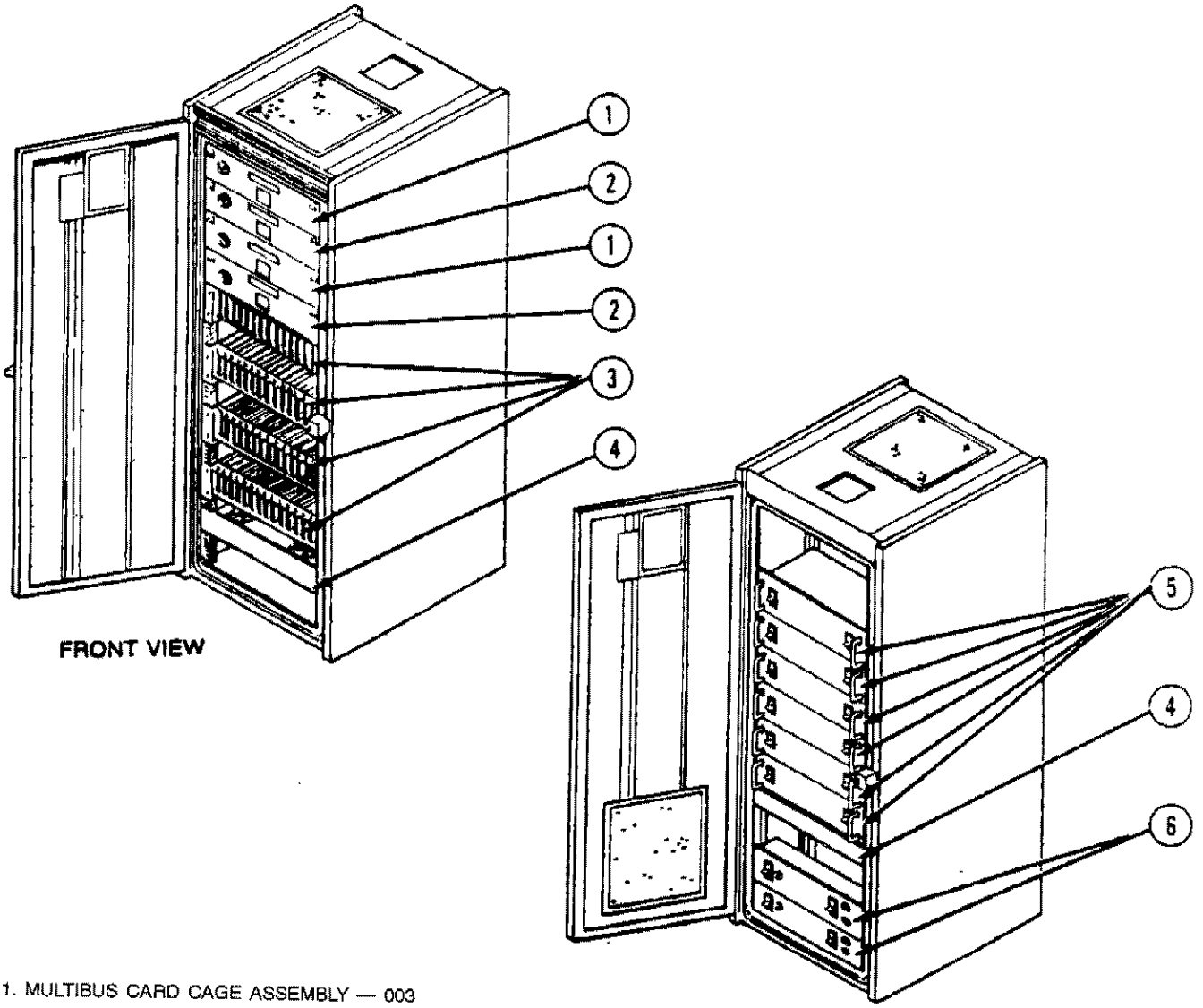
1. MULTIBUS CARD CAGE ASSEMBLY — 005
2. SINGLE MULTIVOLTAGE POWER SUPPLY ASSEMBLY
3. SINGLE SINGLE VOLTAGE POWER SUPPLY ASSEMBLY
4. BUS CONNECTOR CARD CAGE ASSEMBLY
5. FAN ASSEMBLY (DUAL)
6. AC POWER DISTRIBUTION ASSEMBLY

FIGURE 1-6. RCU CABINET CONFIGURATION



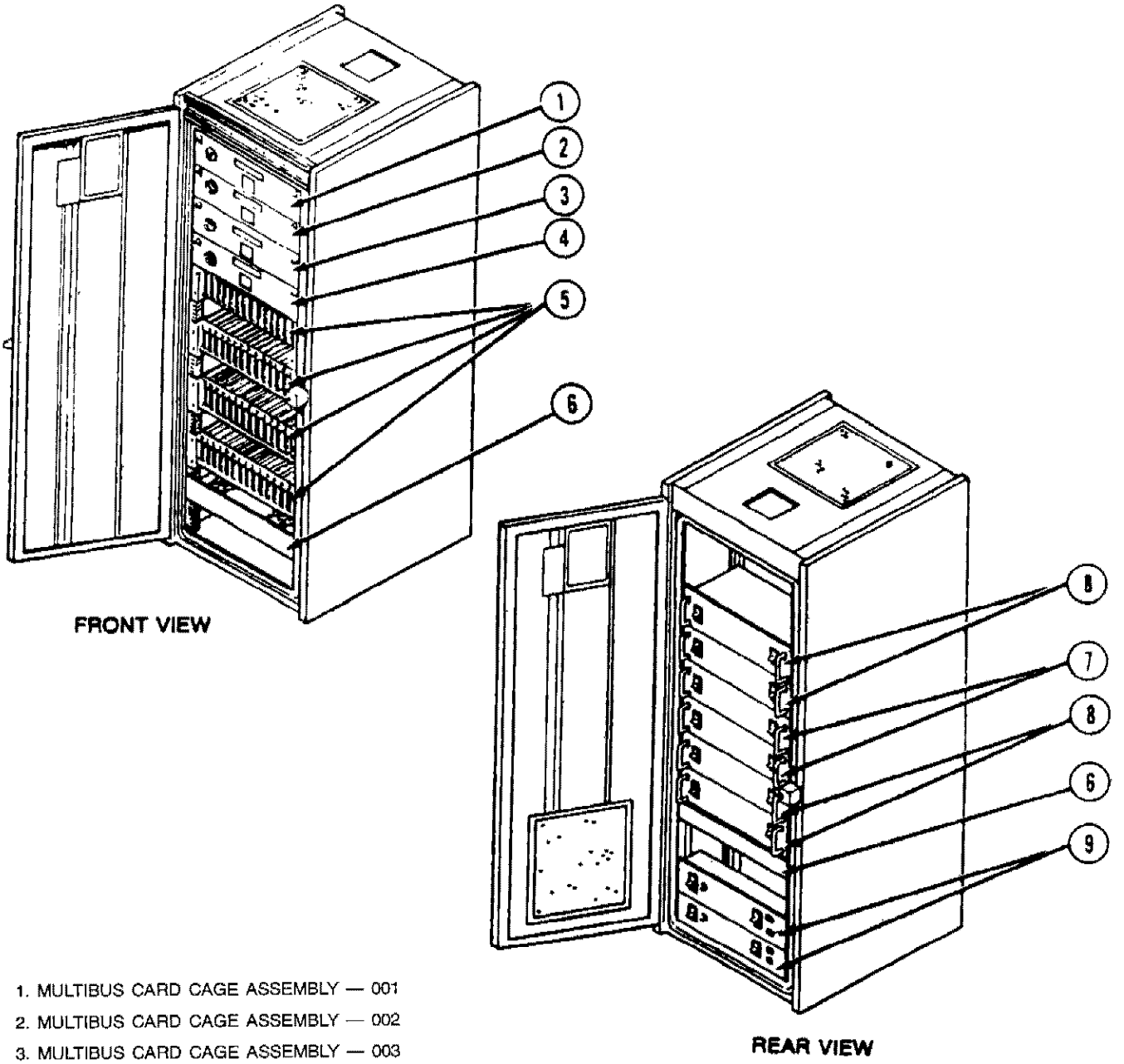
1. MULTIBUS CARD CAGE ASSEMBLY — 001
2. MULTIBUS CARD CAGE ASSEMBLY — 002
3. BUS CONNECTOR CARD CAGE ASSEMBLIES
4. FAN ASSEMBLY (QUAD)
5. DUAL SINGLE VOLTAGE POWER SUPPLY ASSEMBLIES
6. DUAL MULTIVOLTAGE POWER SUPPLY ASSEMBLIES
7. AC POWER DISTRIBUTION ASSEMBLIES

FIGURE 1-7. CCU/CCU CABINET CONFIGURATION



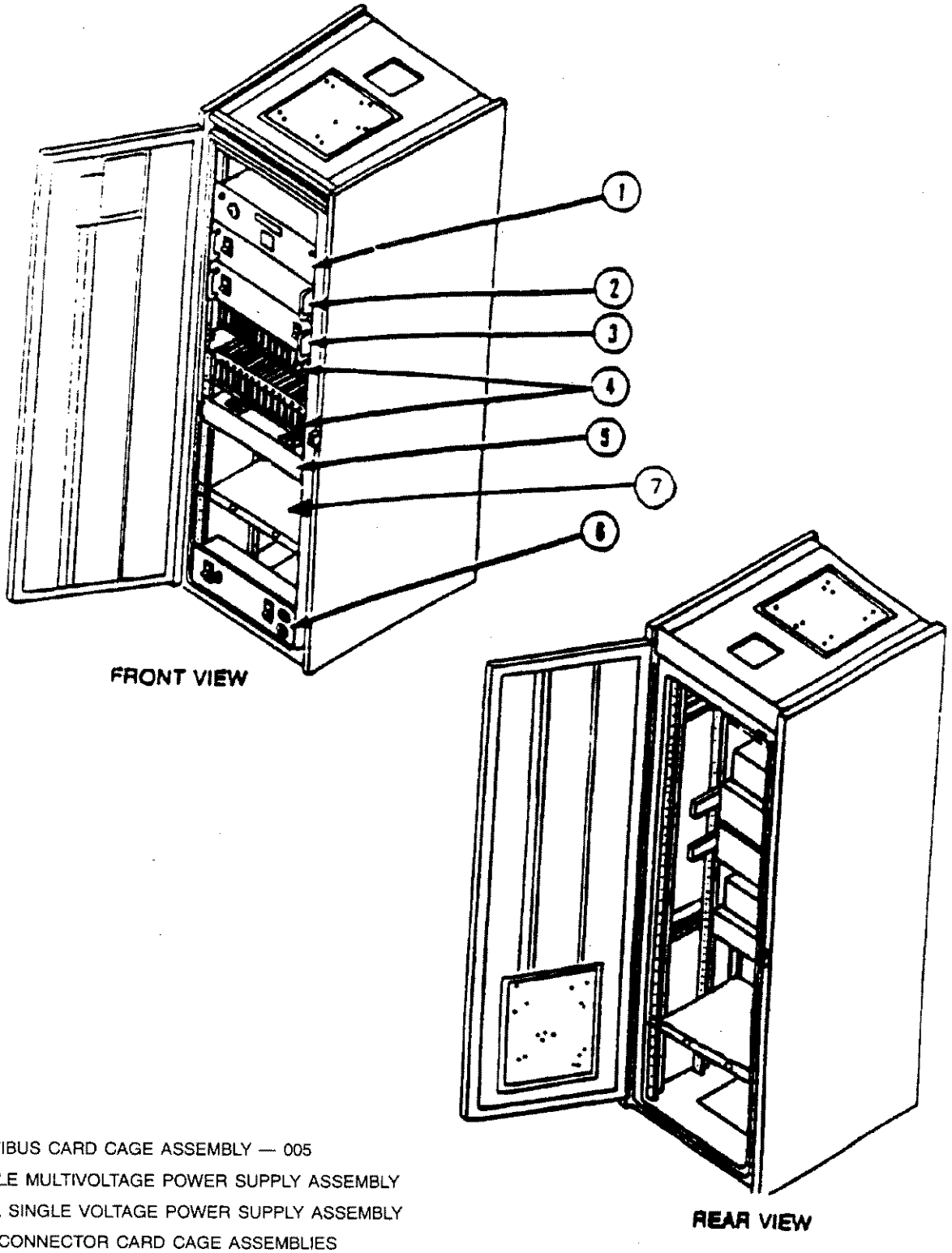
1. MULTIBUS CARD CAGE ASSEMBLY — 003
2. MULTIBUS CARD CAGE ASSEMBLY — 004
3. BUS CONNECTOR CARD CAGE ASSEMBLIES
4. FAN ASSEMBLY (QUAD)
5. DUAL SINGLE VOLTAGE POWER SUPPLY ASSEMBLIES
6. AC POWER DISTRIBUTION ASSEMBLIES

FIGURE 1-8. PCU/PCU CABINET CONFIGURATION



1. MULTIBUS CARD CAGE ASSEMBLY — 001
2. MULTIBUS CARD CAGE ASSEMBLY — 002
3. MULTIBUS CARD CAGE ASSEMBLY — 003
4. MULTIBUS CARD CAGE ASSEMBLY — 004
5. BUS CONNECTOR CARD CAGE ASSEMBLIES
6. FAN ASSEMBLY (QUAD)
7. DUAL MULTIVOLTAGE POWER SUPPLY ASSEMBLIES
8. DUAL SINGLE VOLTAGE POWER SUPPLY ASSEMBLIES
9. AC POWER DISTRIBUTION ASSEMBLIES

FIGURE 1-9. CCU/PCU CABINET CONFIGURATION



1. MULTIBUS CARD CAGE ASSEMBLY — 005
2. SINGLE MULTIVOLTAGE POWER SUPPLY ASSEMBLY
3. DUAL SINGLE VOLTAGE POWER SUPPLY ASSEMBLY
4. BUS CONNECTOR CARD CAGE ASSEMBLIES
5. FAN ASSEMBLY (DUAL)
6. AC POWER DISTRIBUTION ASSEMBLY
7. SHELF

FIGURE 1-10. RCU EXPANDED CABINET CONFIGURATION

1.3.2 Peripheral Control Elements

Peripheral control elements are described as follows and illustrated in figures 1-11 through 1-18.

a. RFSP — Provides printout of flight strip messages at ARTCC and ATCT sites; prints pertinent flight data, prints composed FDIO messages, or logs error messages. The RFSP peripheral element may be one of three types.

1. Original FDIO printer manufactured by Wespercorp (FA 10095/2) illustrated in figure 1-11.
2. Printer manufactured by Data Products (FA 10095/11) and is illustrated in figure 1-12.
3. Printer manufactured by IER (FA 10095/14) and is illustrated in figure 1-13.

Throughout this manual the three printers will be referenced as RFSPs unless differences warrant specifying the printers separately. In such cases the printers will be referenced by an FA number.

b. RANK — Provides operator interface for Host FDIO message entry at ATCT sites (figures 1-14 and 1-15).

c. CRT — Provides display area for messages that have been printed on a printer; provides composition and editing area for FDIO messages. Located at ATCT. The CRT peripheral element may be one of three types:

1. Original FDIO CRT (FA 10095/4) is illustrated in figure 1-16.
2. CRT (FA 10095/12) is illustrated in figure 1-17.
3. CRT (FA 10095/18) is illustrated in figure 1-17A.

Throughout this manual all three will be referenced as CRTs unless differences warrant specifying the CRTs separately. In such cases the CRTs will be referenced by an FA number.

d. MODEM — GFE used to provide communication between ARTCC CCUs and ATCT RCUs (figure 1-18).

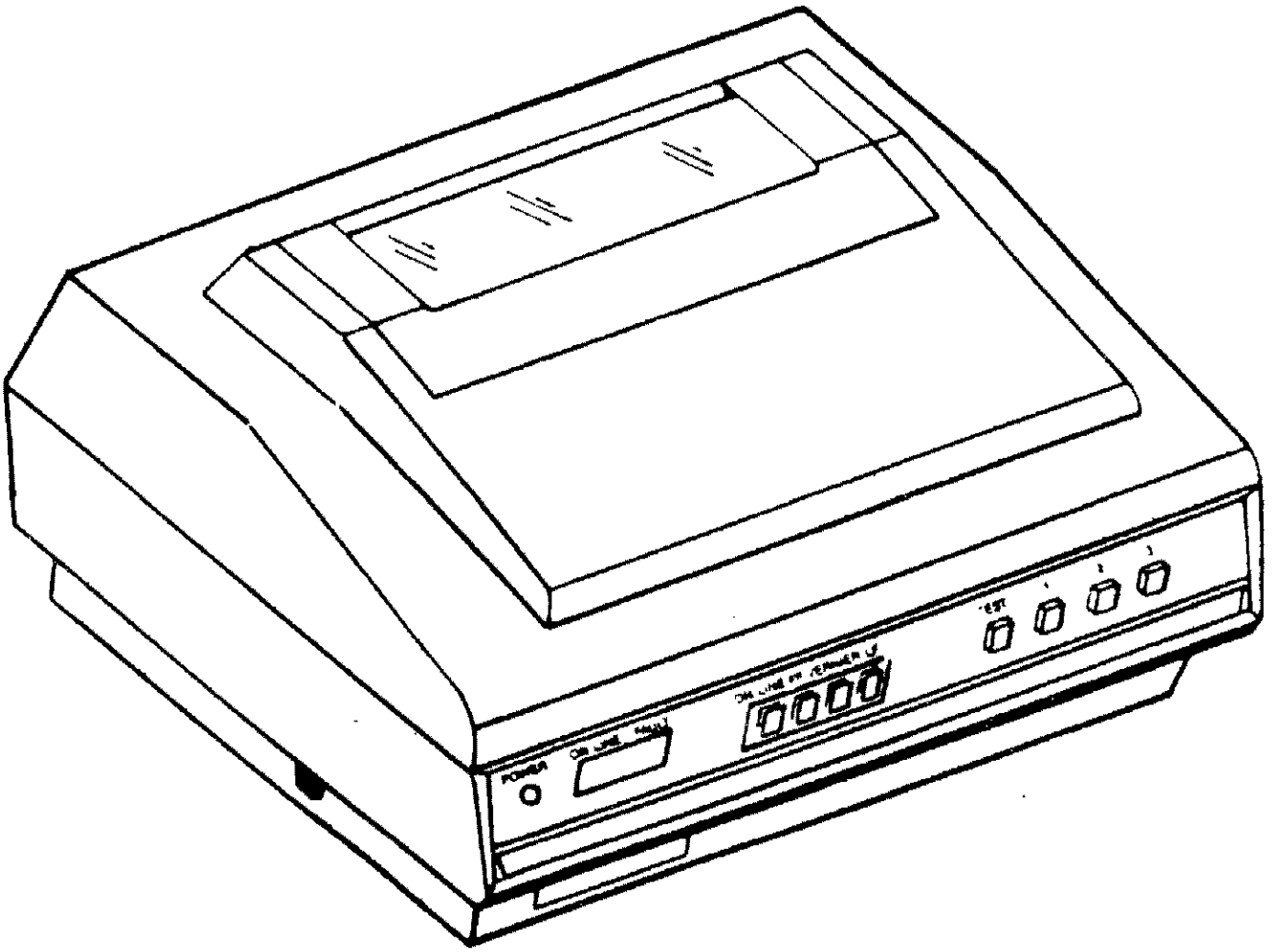


FIGURE 1-11. RFSP PERIPHERAL ELEMENT

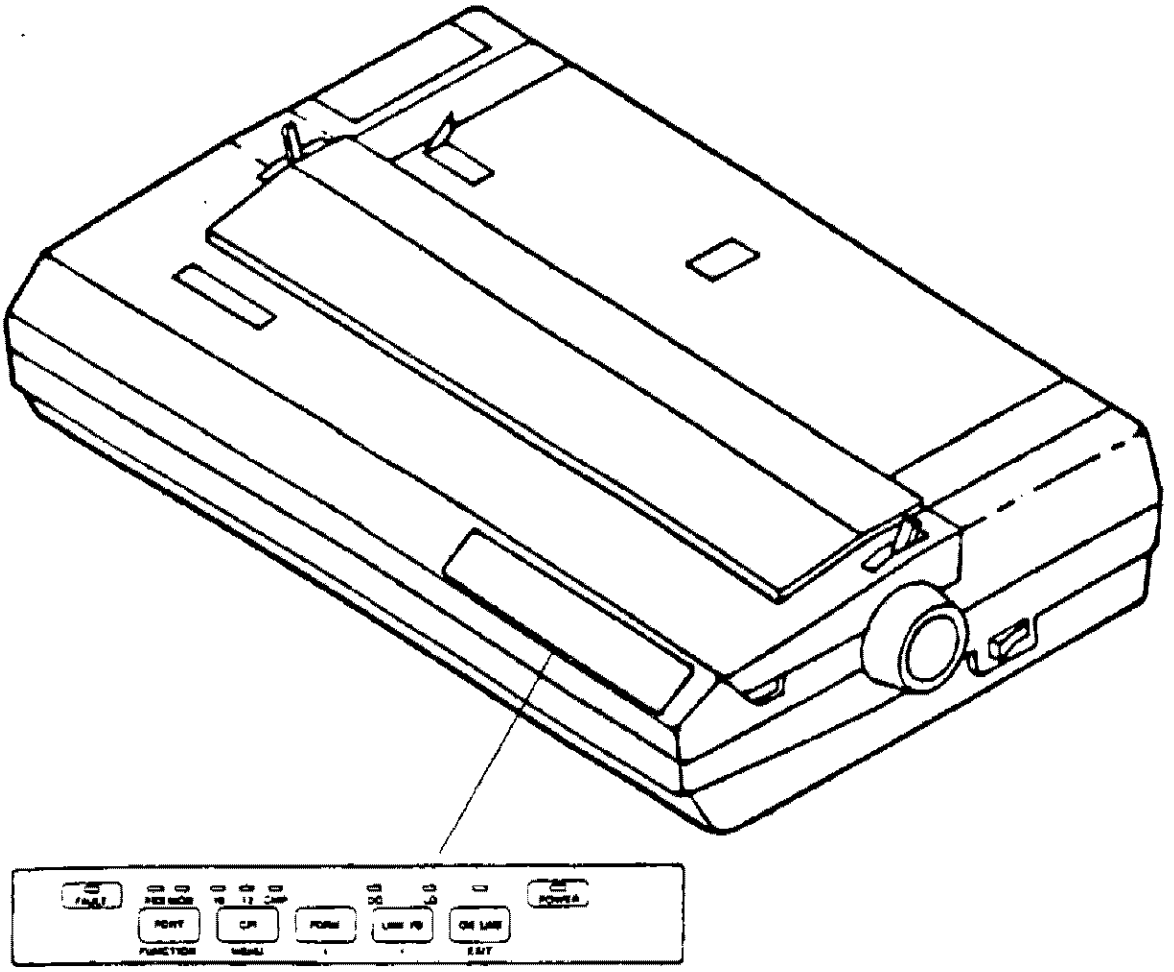


FIGURE 1-12. RFSP (FA 10095/11) PERIPHERAL ELEMENT

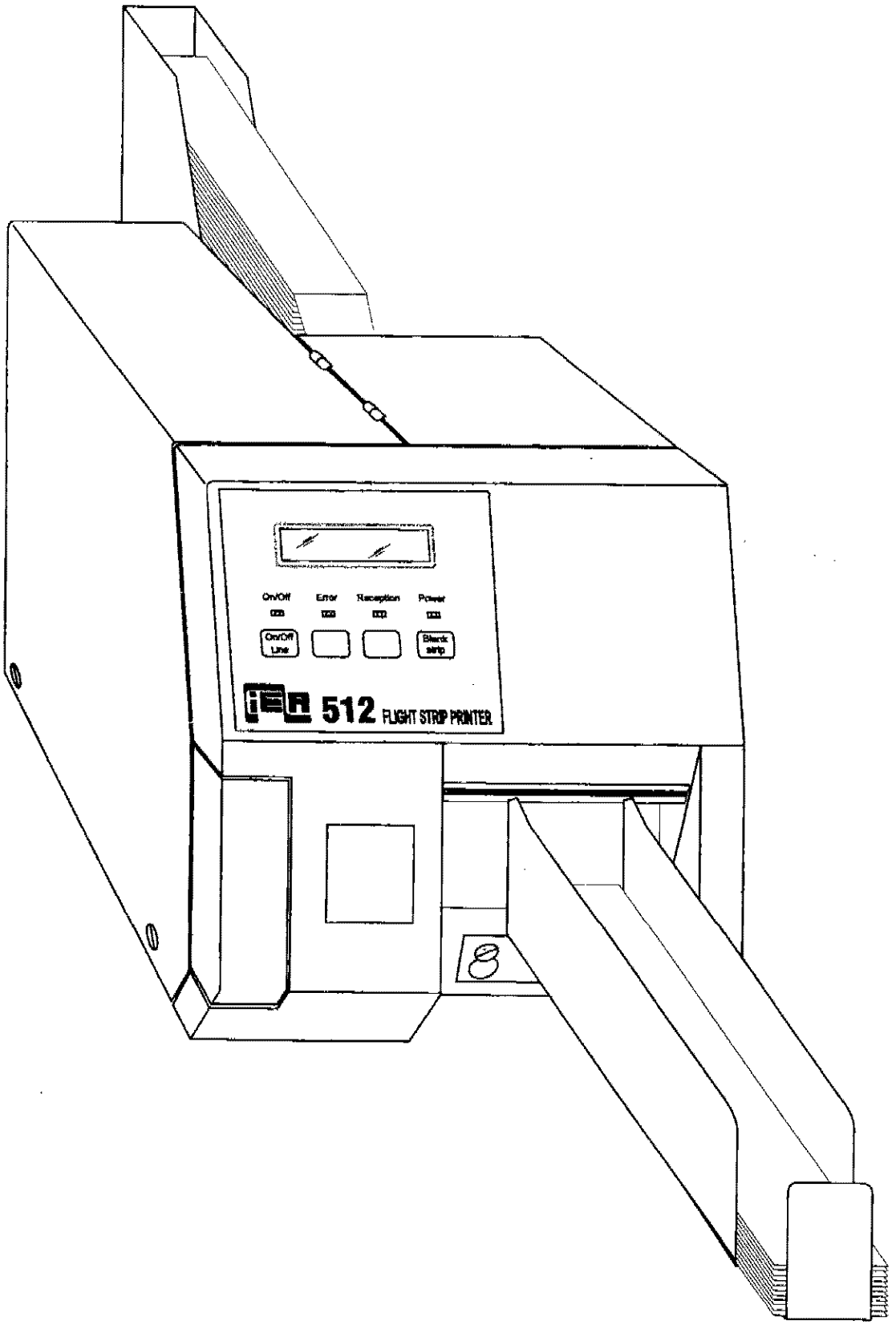


FIGURE 1-13. RFSP (FA 10095/14) PERIPHERAL ELEMENT

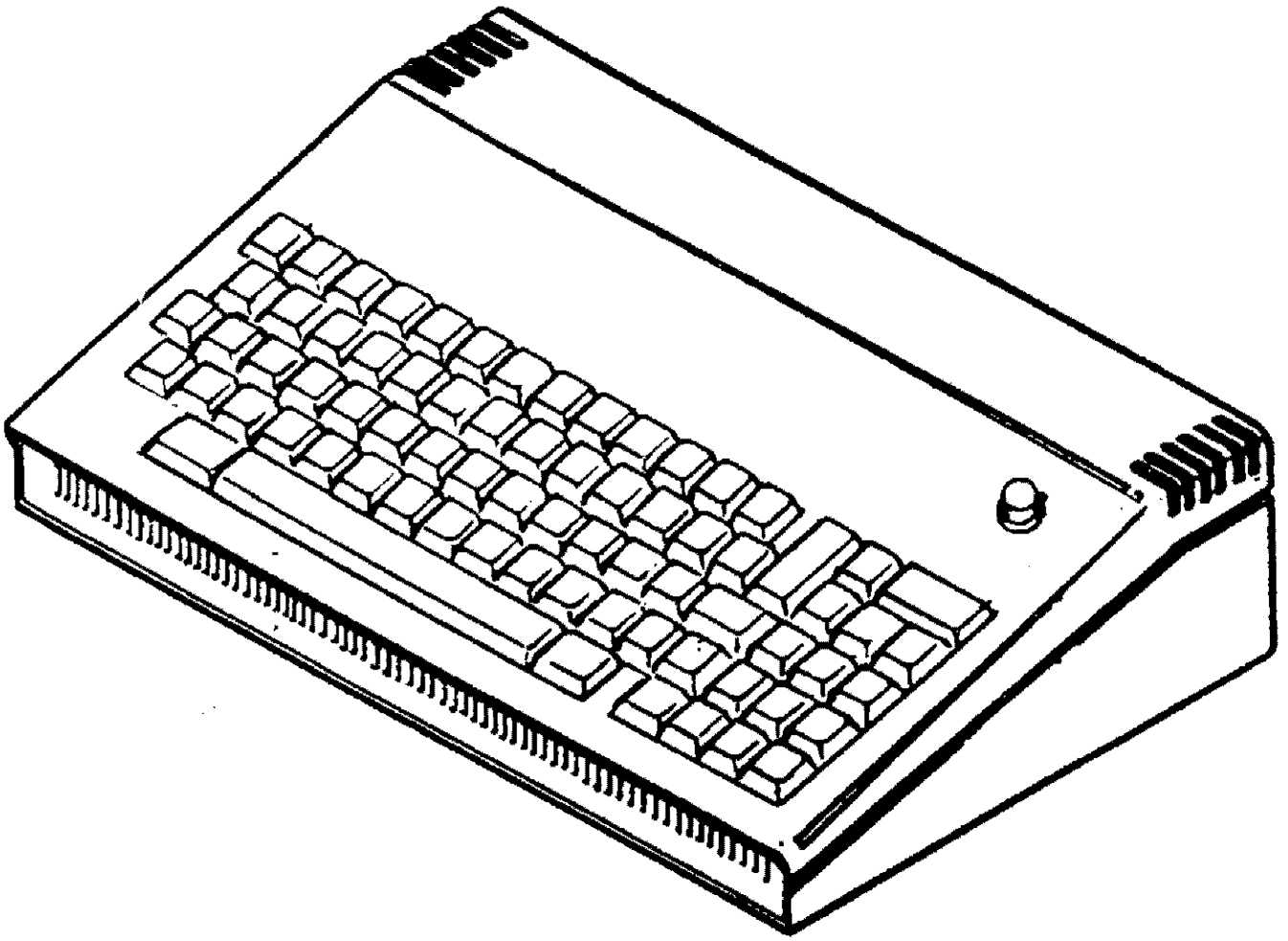


FIGURE 1-14. RANK (FA 10095/3) PERIPHERAL ELEMENT

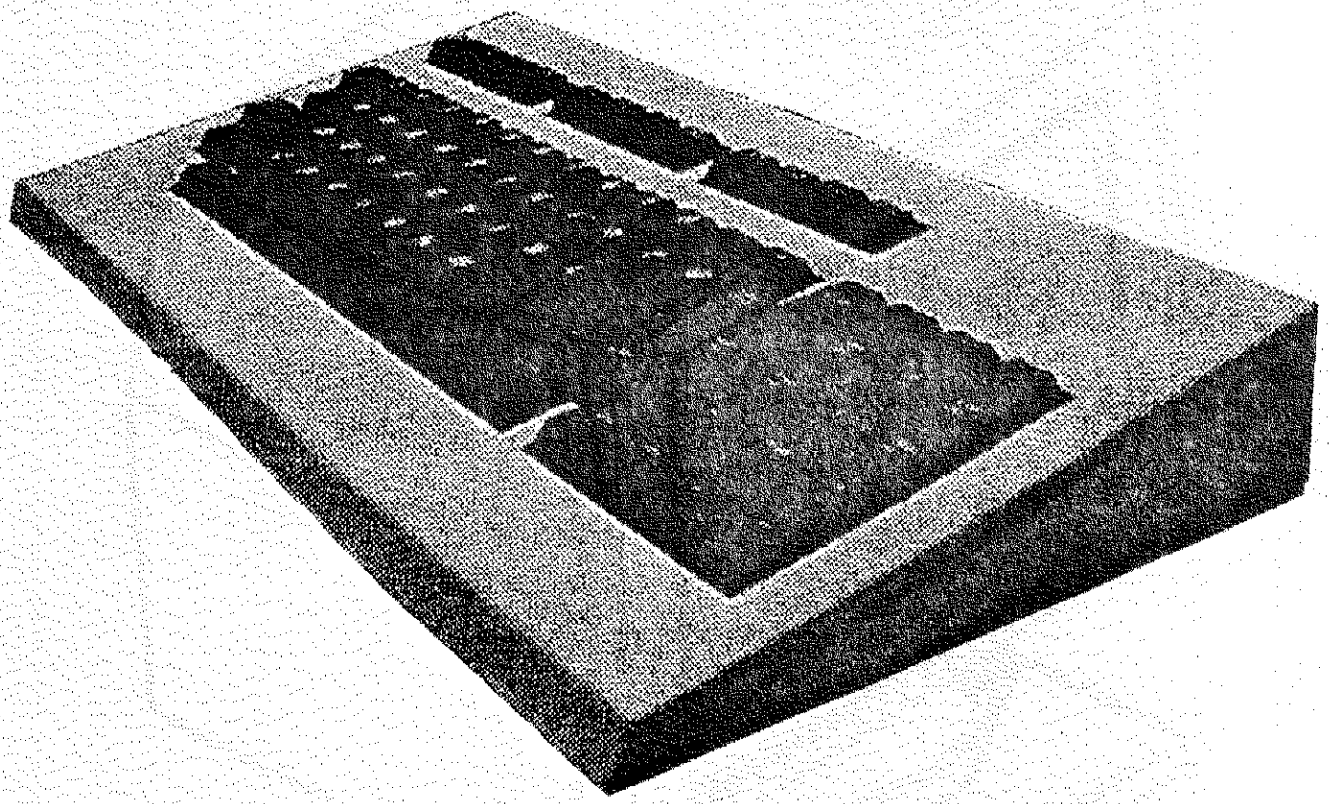


FIGURE 1-15. RANK (FA 10095/17) PERIPHERAL ELEMENT

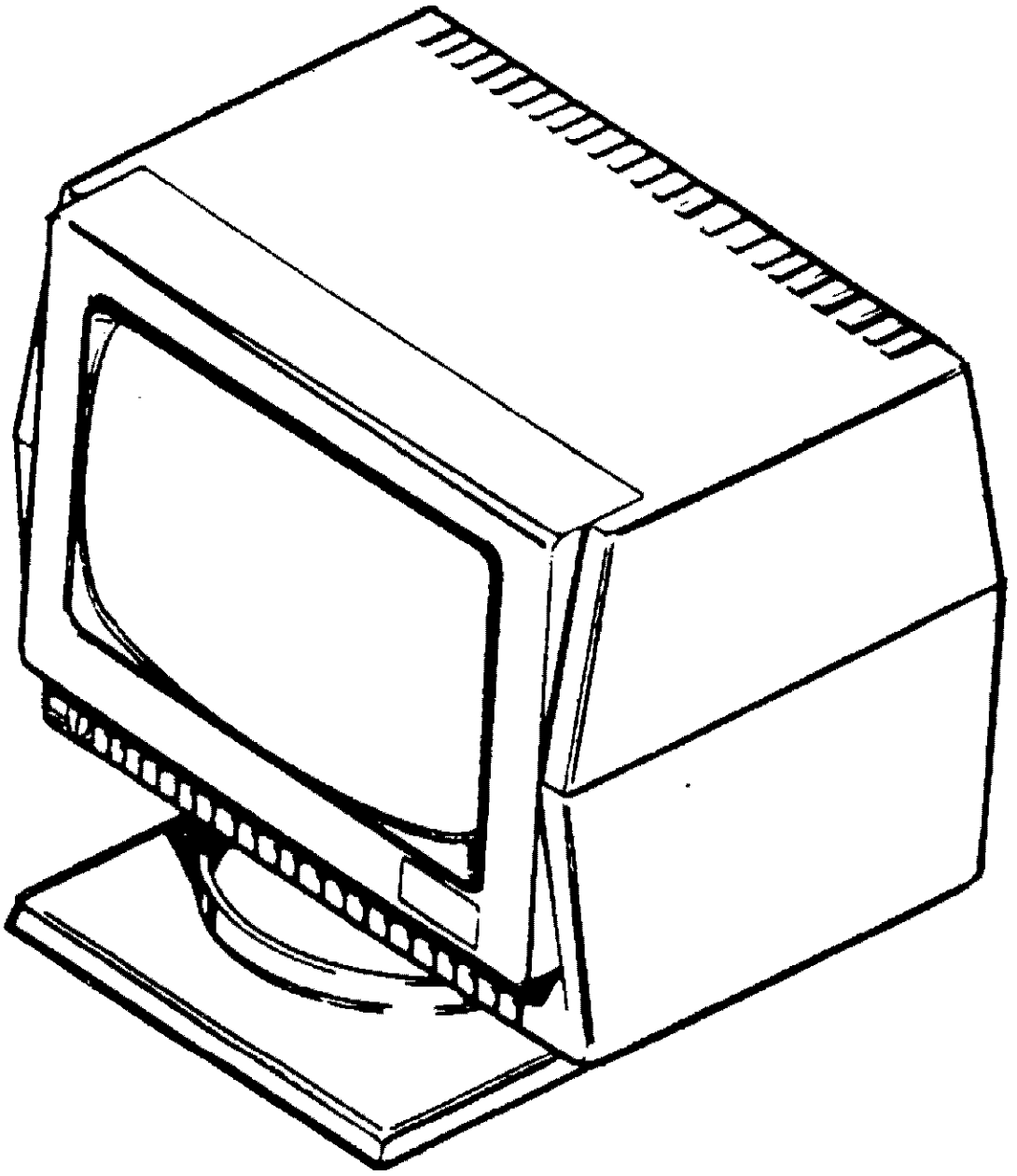


FIGURE 1-16. CRT (FA 10095/4) PERIPHERAL ELEMENT

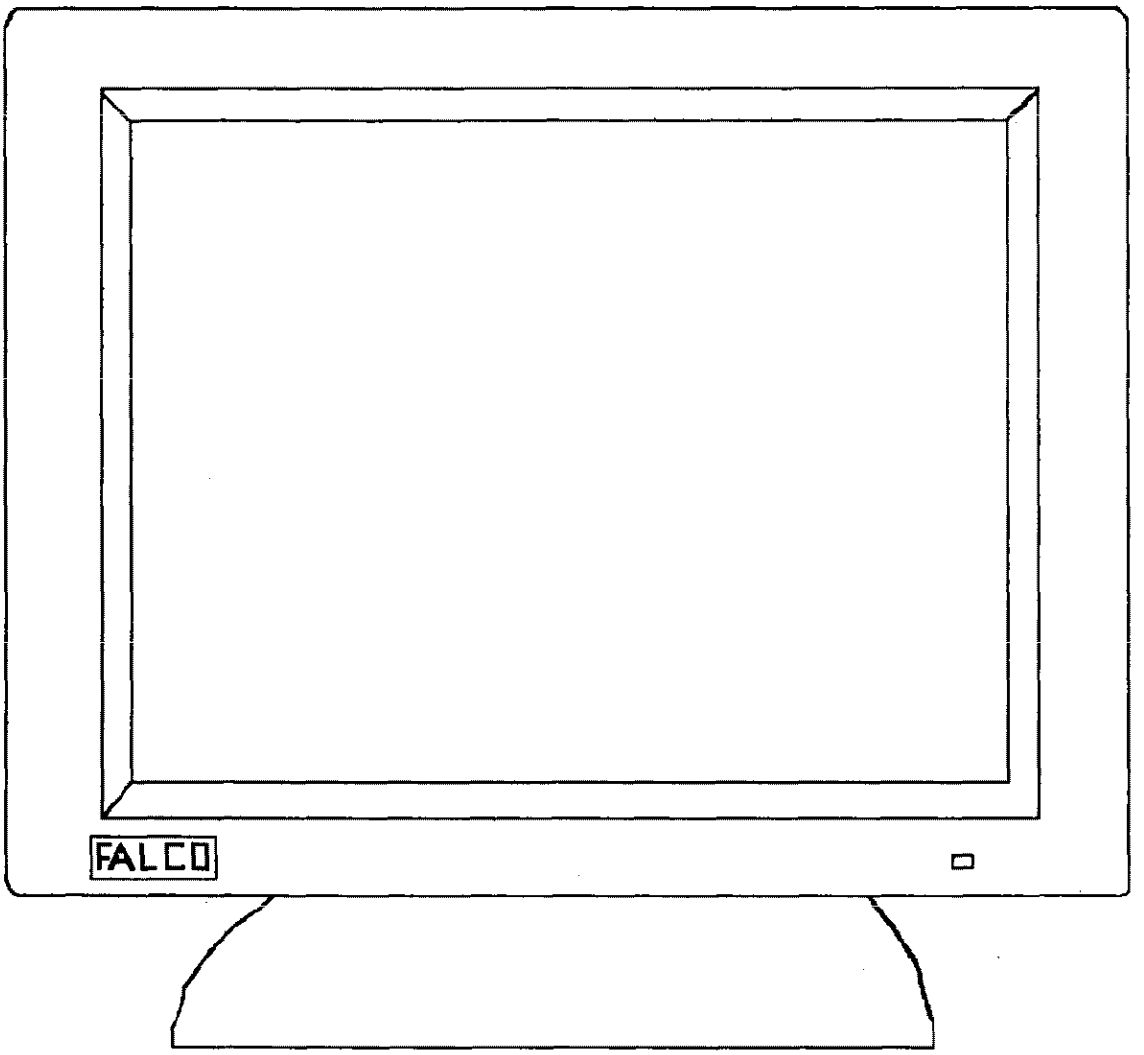


FIGURE 1-17. CRT (FA 10095/12) PERIPHERAL ELEMENT

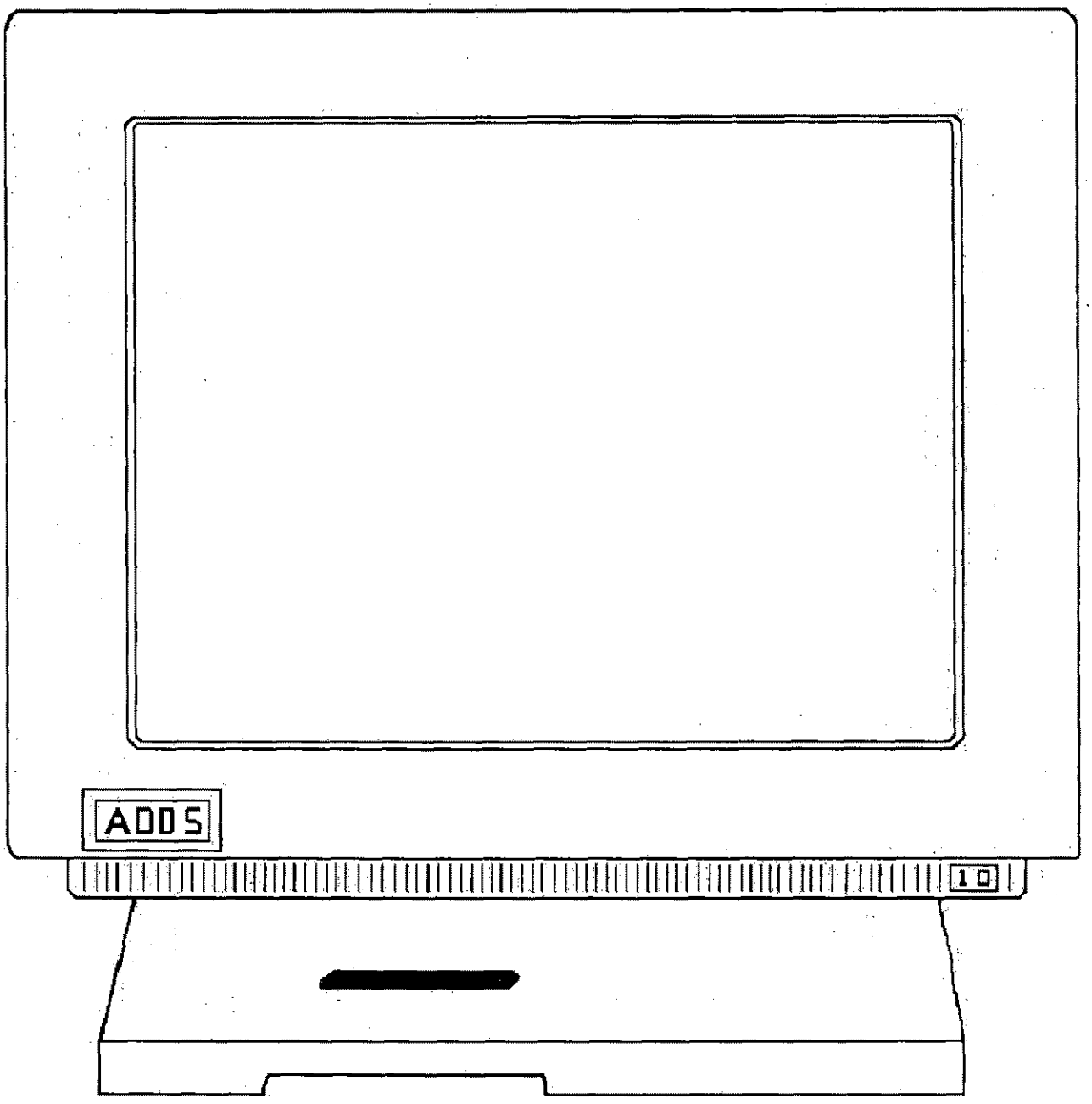


FIGURE 1-17A. CRT (FA 10095/18) PERIPHERAL ELEMENT

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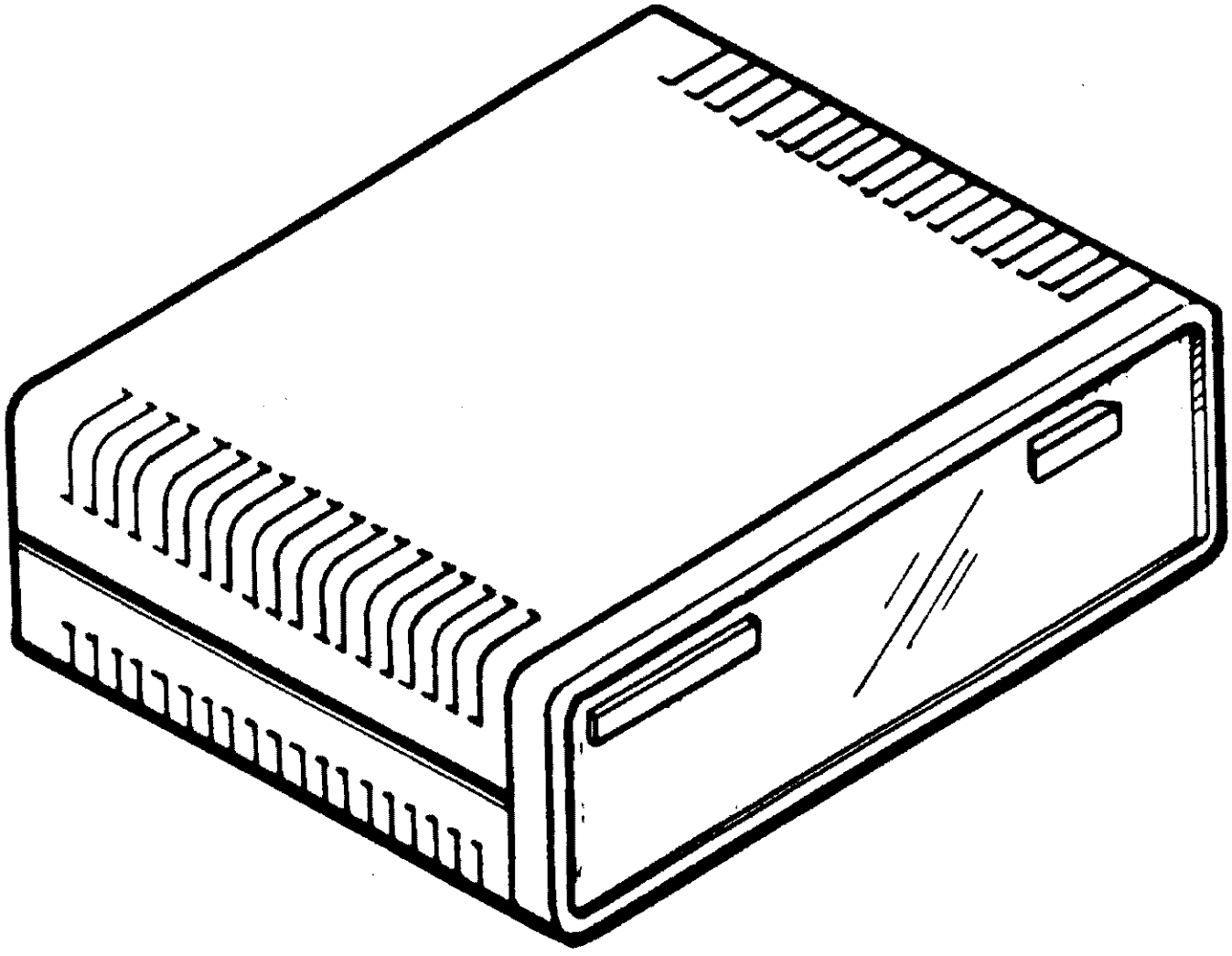


FIGURE 1-18. MODEM PERIPHERAL ELEMENT (FURNISHED BY CUSTOMER)

Table 1-2 lists the maximum number and types of equipment communicating with each control cabinet configuration.

TABLE 1-2. SYSTEM PERIPHERALS

Control Cabinet Configuration	Communicates With	Maximum Number
CCU/CCU	RCUs (through modems)	56
PCU/PCU	RFSPs	56
CCU/PCU	RCUs (through modems)	28
	RFSPs	28
CCU	RCUs (through modems)	28
PCU	RFSPs	28
RCU *	CCU (through modem)	1
	RFSPs	10
	RANKs	5
	CRTs	5
RCU Expanded	CCU (through modem)	1
	RFSPs	10
	RANKs	5
	CRTs	5

*Any combination that includes at least one RFSP and one RANK is allowed; total peripheral elements total 14, with the requirement of the contract to have a spare slot and a slot for the maintenance channel.

1.3.3 BC Cards

BC cards control message flow between the control elements and peripherals. Each BC card cage assembly can hold up to 16 BC cards. The PCU has one card slot reserved for a maintenance port and one spare. The RCU has one card slot reserved for a maintenance port. At time of installation, peripheral units are verified to be in operating order at the maintenance port before being cable connected to the system. All BC card cage assemblies contain spare ports (not addressed). Table 1-3 illustrates the breakdown of the BC card cage assemblies by control unit.

1.3.4 Equipment Redundancy

FDIO control elements located at the ARTCC (CCUs and PCUs) are designed such that if any single failure occurs, the system will continue to operate. In order to satisfy this design criterion, each CCU and PCU cabinet assembly configuration contains two identical sets of equipment. One set of equipment is active (primary); the other is semi-active (secondary). The two sets of equipment contain hardware and firmware which monitor each other's performance, detect operating problems, and, if necessary, automatically bring failed equipment offline and switch the semi-active equipment online.

Three firmware tasks (Fail-Safe (FS), Fail-Safe Electronics (FSE), and Intercomputer Link (ICL)) in the CCU and PCU configurations satisfy the requirement to provide redundancy. The fail safe electronics

consists of an independent microcomputer system which monitors system performance, controls the intercomputer link, and executes the primary-secondary switch.

Each FDIO system will be installed by the contractor. All equipment will be thoroughly checked out and certified operational before the system is brought online.

TABLE 1-3. BC CARD CAGE ASSEMBLY BREAKDOWN

Control Unit	Available Ports (addressed)	Maintenance Address
CCU	28	N/A
PCU	28	29
RCU Expanded	20	21
RCU	14	21

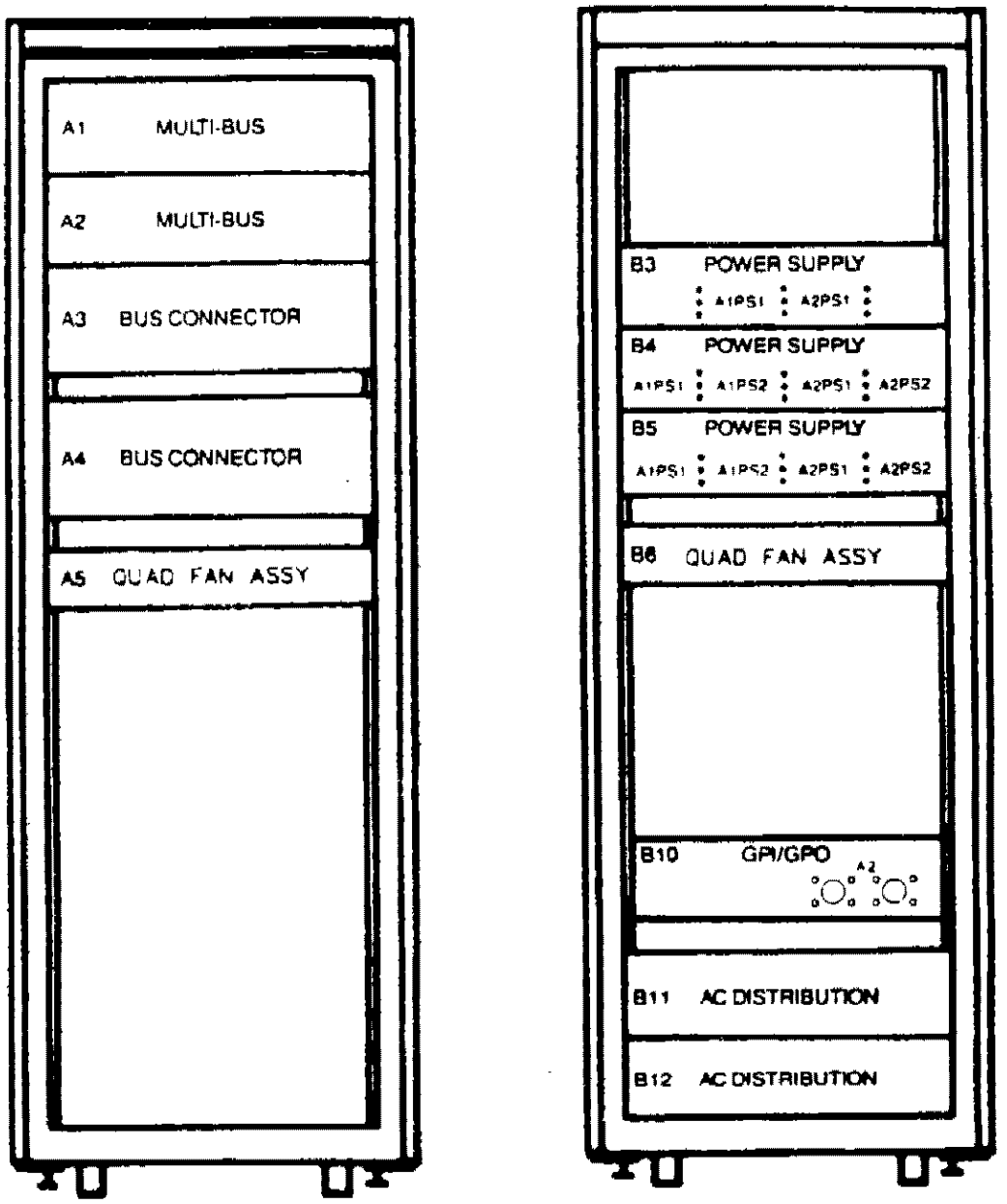
1.3.5 Cabinet Assembly Makeup

All assemblies of the control cabinets, regardless of the configuration, are mounted in a 6-foot equipment cabinet equipped with 19-inch rails. The rails conform to the Electronics Industry Association (EIA) specification RS-310-C. The number of assemblies contained in the cabinet are determined by the configuration required at each particular site.

Component reference designations within the cabinet assembly are outlined in the FDIO Family Tree in the front matter and shown in figures 1-19 through 1-25.

Each type of assembly found in the control cabinets is described and illustrated in the following paragraphs and figures.

1.3.5.1 Multibus Card Cage Assembly. The Multibus assembly is the heart of each cabinet configuration. The CCU and PCU receive messages directly from the Host (the RCU receives messages from the CCU via modem). Messages are transmitted to their peripheral element destination through BCs. The message source and destination for each control element is shown in table 1-4.



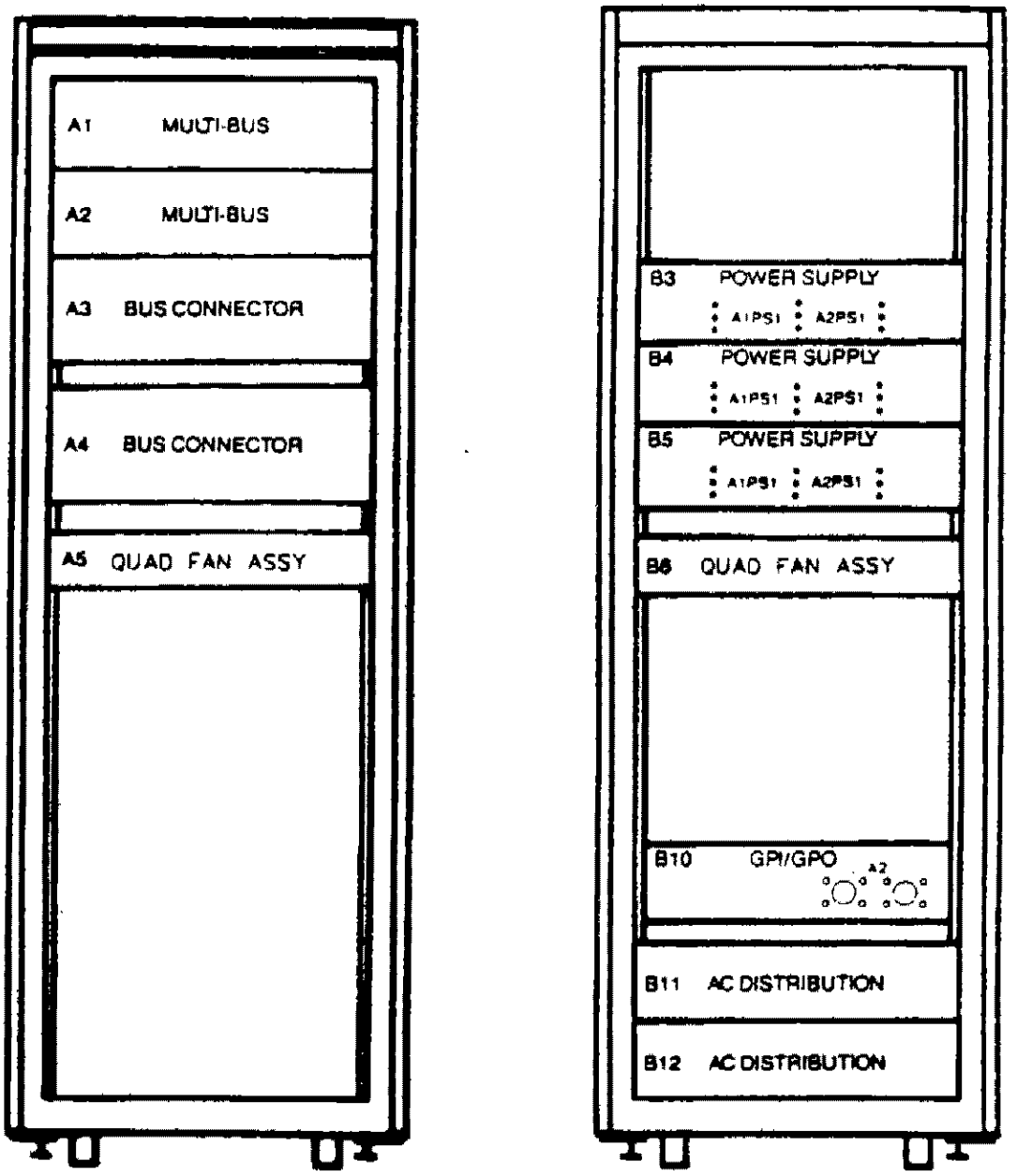
B3A1PS1 SUPPLIES A1

B3A2PS1 SUPPLIES A2

B4 SUPPLIES A3

B5 SUPPLIES A4

FIGURE 1-19. CCU CABINET ASSEMBLY COMPONENT REFERENCE DESIGNATIONS



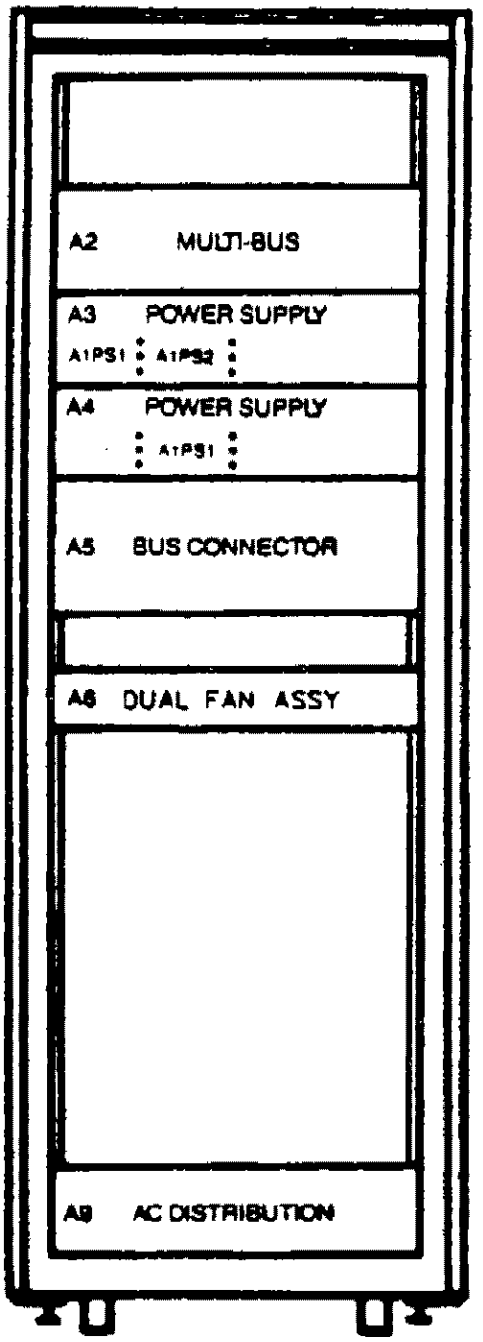
B3A1PS1 SUPPLIES A1

B3A2PS1 SUPPLIES A2

B4 SUPPLIES A3

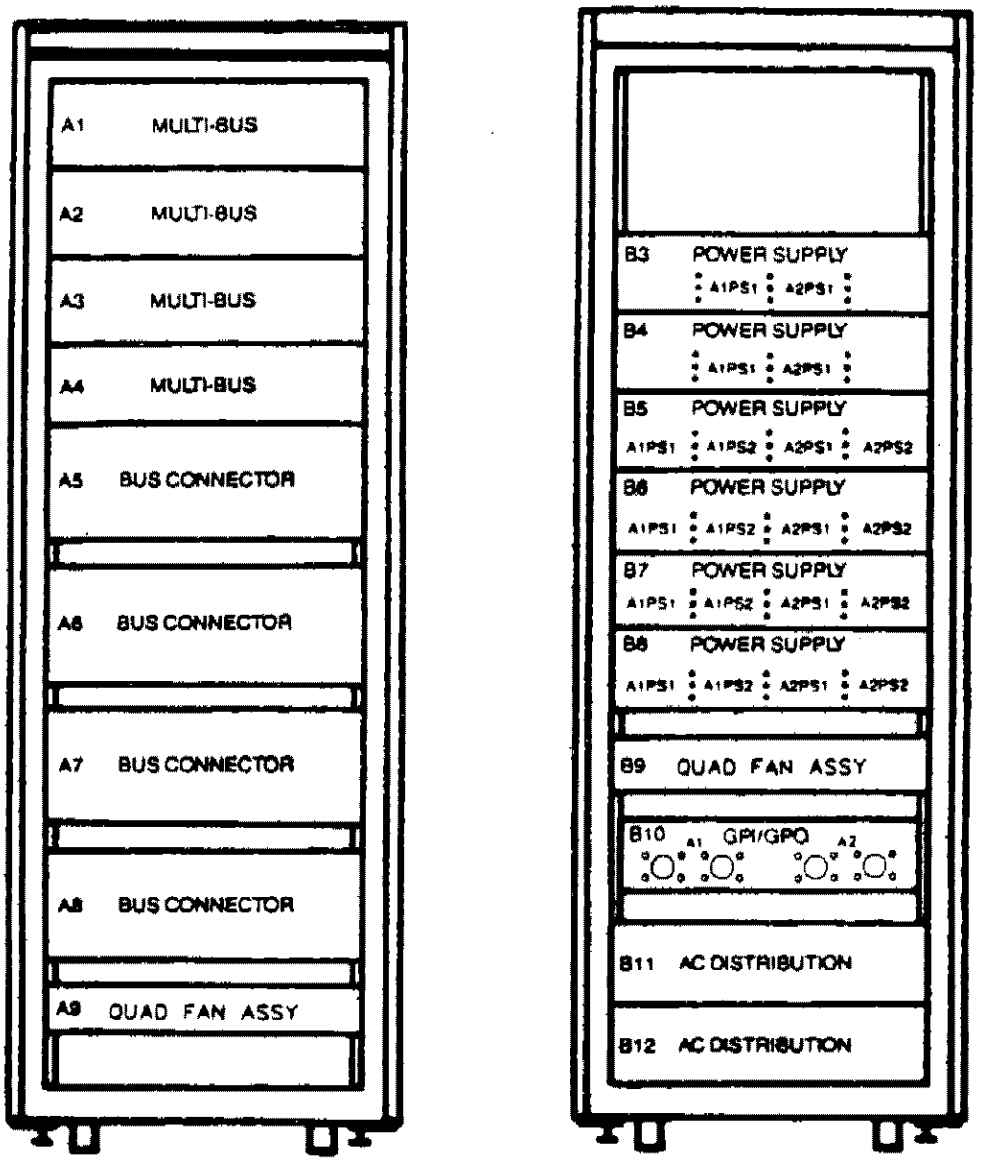
B5 SUPPLIES A4

FIGURE 1-20. PCU CABINET ASSEMBLY COMPONENT REFERENCE DESIGNATIONS



A3 SUPPLIES A2
A4 SUPPLIES A5

FIGURE 1-21. RCU CABINET ASSEMBLY COMPONENT REFERENCE DESIGNATIONS

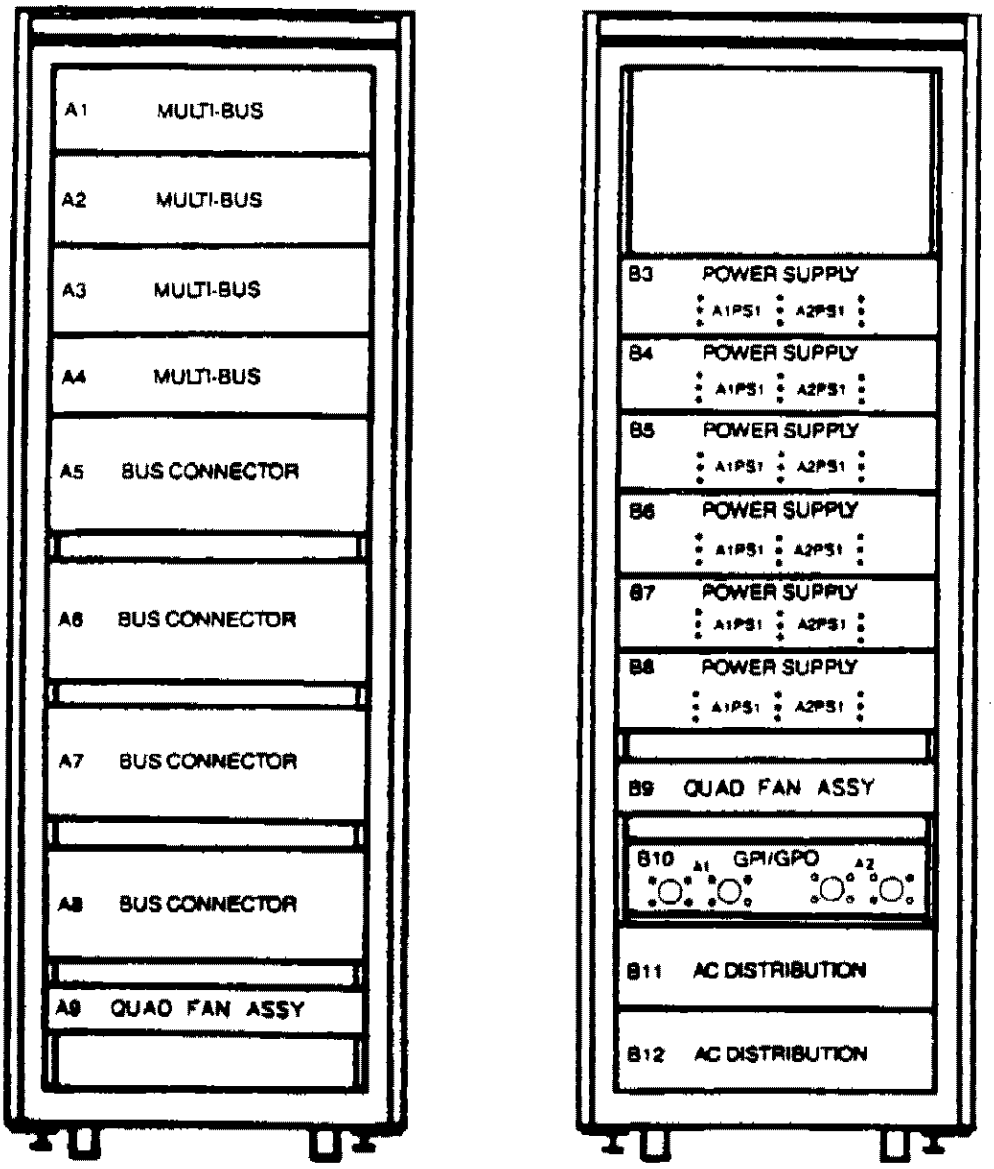


FRONT

REAR

B3A1PS1 SUPPLIES A1
B3A2PS1 SUPPLIES A2
B4A1PS1 SUPPLIES A3
B4A2PS1 SUPPLIES A4
B5 SUPPLIES A5
B6 SUPPLIES A6
B7 SUPPLIES A7
B8 SUPPLIES A8

FIGURE 1-22. CCU/CCU CABINET ASSEMBLY COMPONENT REFERENCE DESIGNATIONS

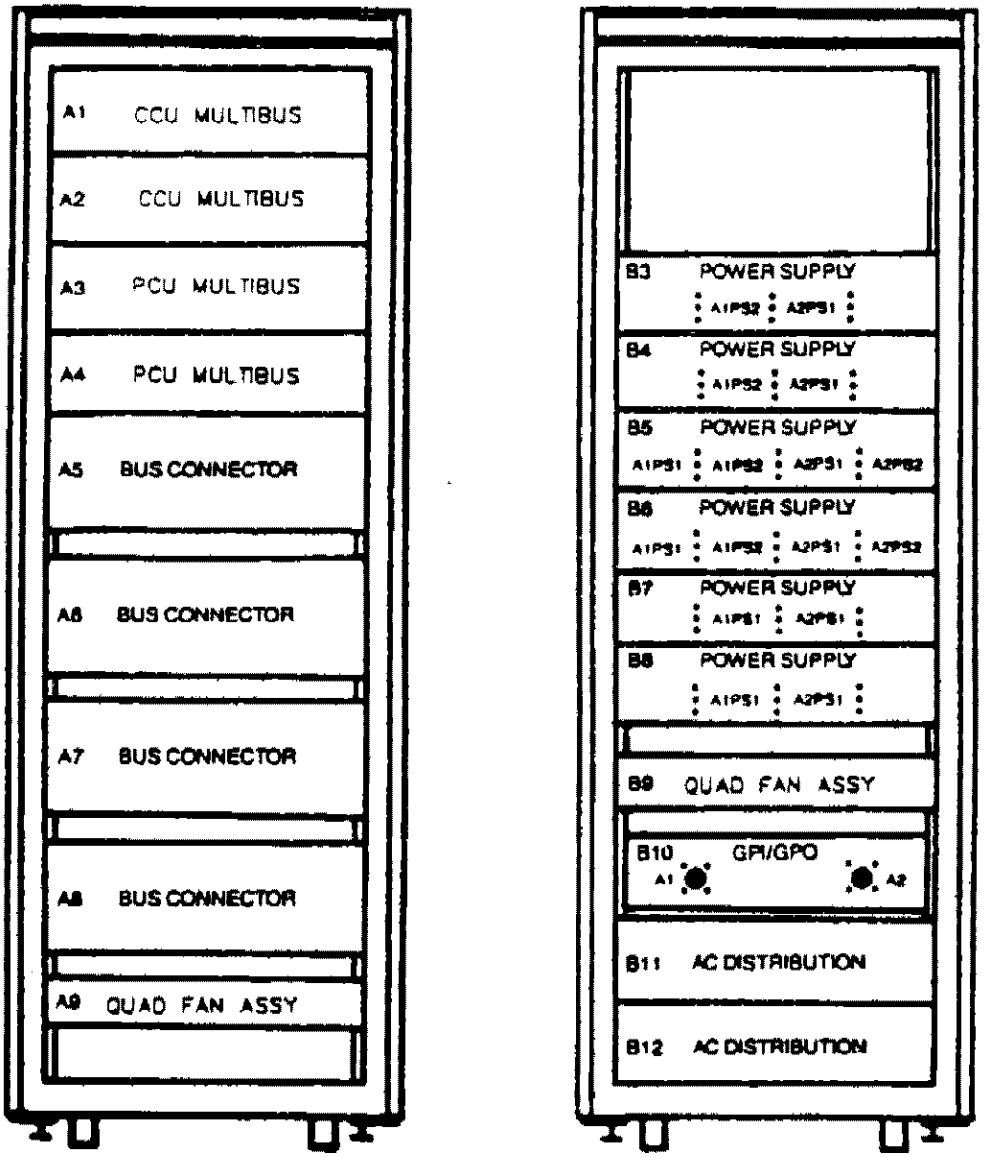


FRONT

B3A1PS1 SUPPLIES A1
B3A2PS1 SUPPLIES A2
B4A1PS1 SUPPLIES A3
B4A2PS1 SUPPLIES A4
B5 SUPPLIES A5
B6 SUPPLIES A6
B7 SUPPLIES A7
B8 SUPPLIES A8

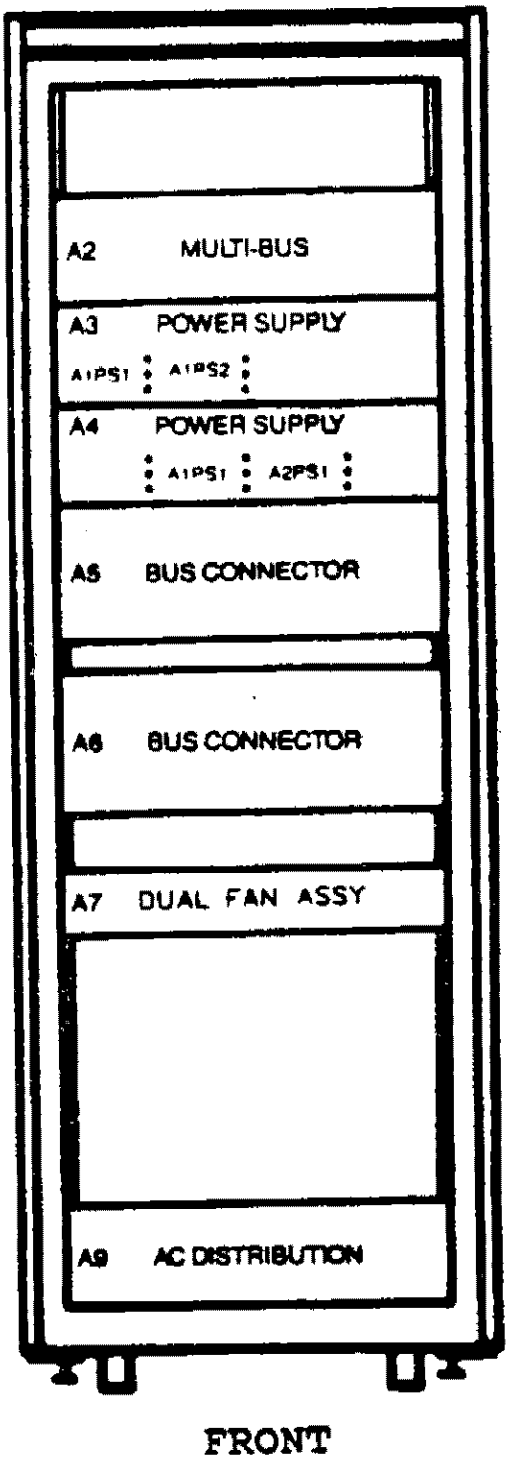
REAR

FIGURE 1-23. PCU/PCU CABINET ASSEMBLY COMPONENT REFERENCE DESIGNATIONS



B3A1PS1 SUPPLIES A1
B3A2PS1 SUPPLIES A2
B4A1PS1 SUPPLIES A3
B4A2PS1 SUPPLIES A4
B5 SUPPLIES A5
B6 SUPPLIES A6
B7 SUPPLIES A7
B8 SUPPLIES A8

FIGURE 1-24. CCU/PCU CABINET ASSEMBLY COMPONENT REFERENCE DESIGNATIONS



A3 SUPPLIES A2
A4A1PS1 SUPPLIES A5
A4A2PS1 SUPPLIES A6

FIGURE 1-25. RCU EXPANDED CABINET ASSEMBLY COMPONENT REFERENCE DESIGNATIONS

TABLE 1-4. MESSAGE SOURCE AND DESTINATION

	MESSAGE	
Control Element	Source	Destination
CCU	Host	Modem
PCU	Host	RFSP
RCU	Host via CCU & Modems	RFSP or CRT

The Multibus assemblies are listed and illustrated in figure 1-26. Refer to table 1-1 for the type and quantity of Multibus assemblies required for each control cabinet configuration.

1.3.5.2 BC Card Cage Assembly. The BC card cage assembly consists of the card cage, up to 16 BC cards and a BC backplane board. In the CCU cabinet assemblies, BC boards provide a communications link between the Multibus assemblies and the modems for sending or receiving data to or from the associated remote site. In the PCU and RCU cabinet assemblies, BC boards provide a communication link between Multibus assemblies and associated peripheral elements. The PCU BCs interface with RFSP peripheral elements and the RCU BCs interface with RFSP, CRT, and RANK peripheral elements. The BC card rack assembly is illustrated in figure 1-27.

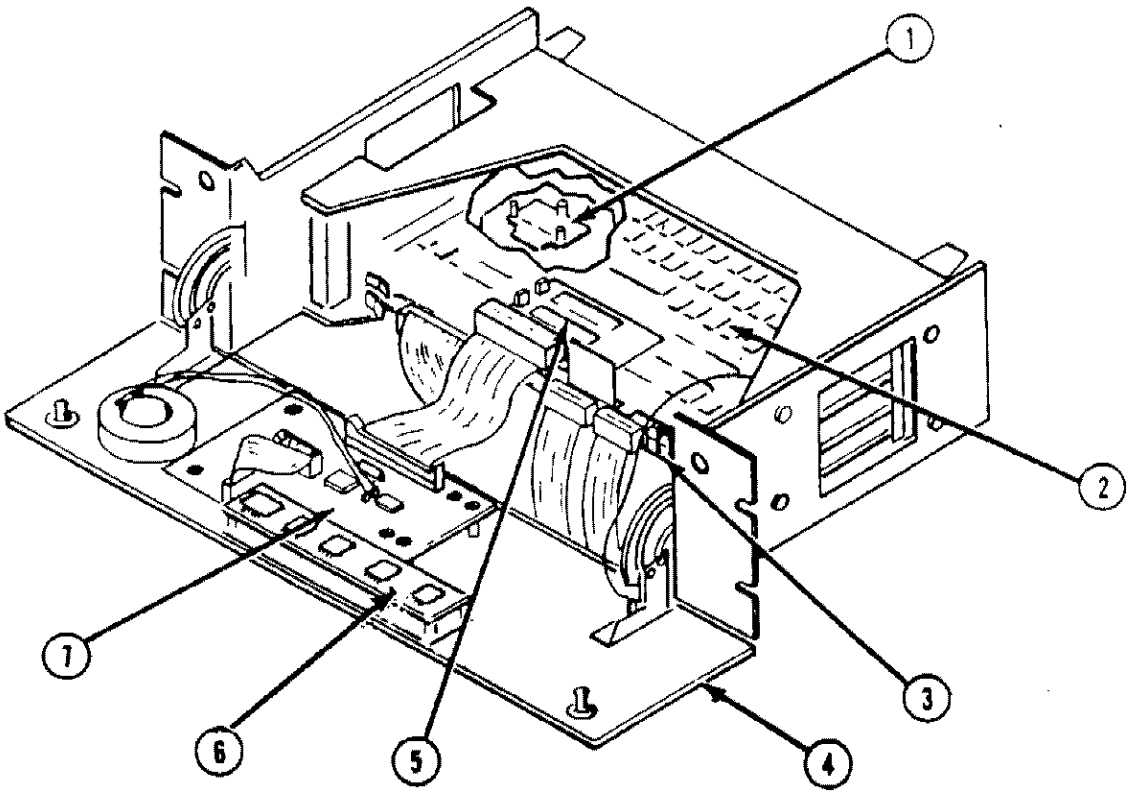
1.3.5.3 Power Supply Assemblies. The power supply assembly configurations are:

a. Single single voltage power supply assemblies contain one 5 Volts direct current (V dc) 12 Ampere (A) power supply and one circuit breaker (figure 1- 28).

b. Dual single voltage power supply assemblies contain two 5 V dc 12 A power supplies and two circuit breakers (figure 1-29).

c. Single multivoltage power supply assembly contain one 5 V dc 12 A power supply, and one ±12 V dc 1.7 A power supply, and one circuit breaker switch (figure 1-30).

d. Dual multivoltage power supply assemblies contain two 5 V dc 12 A power supplies, two ±12 V dc 1.7 A power supplies, and two circuit breaker switches (figure 1-31).



1. TERMINATOR
2. CPU (88/45)
3. UTILITY BOARD (PSU OR CCU)
   16 K RAM MEMORY BOARD (RCU)
4. FRONT PANEL ASSY
5. FRONT PANEL INTERFACE BOARD
6. LCD PANEL
7. FRONT PANEL CONTROL BOARD

MULTIBUS ASSEMBLY -001
- CCU CPU (88/45)
- UTILITY BOARD
- TERMINATOR BOARD
- FRONT PANEL ASSEMBLY

MULTIBUS ASSEMBLY -002
- CCU CPU (88/45)
- UTILITY BOARD
- FRONT PANEL ASSEMBLY

MULTIBUS ASSEMBLY -003
- PCU CPU (88/45)
- UTILITY BOARD
- TERMINATOR BOARD
- FRONT PANEL ASSEMBLY

MULTIBUS ASSEMBLY -004
- CCU CPU (88/45)
- UTILITY BOARD
- FRONT PANEL ASSEMBLY

MULTIBUS ASSEMBLY -005
- RCU CPU (88/45)
- 16 K RAM MEMORY BD
- FRONT PANEL ASSEMBLY

FIGURE 1-26. MULTIBUS CARD CAGE ASSEMBLIES -001 THROUGH -005

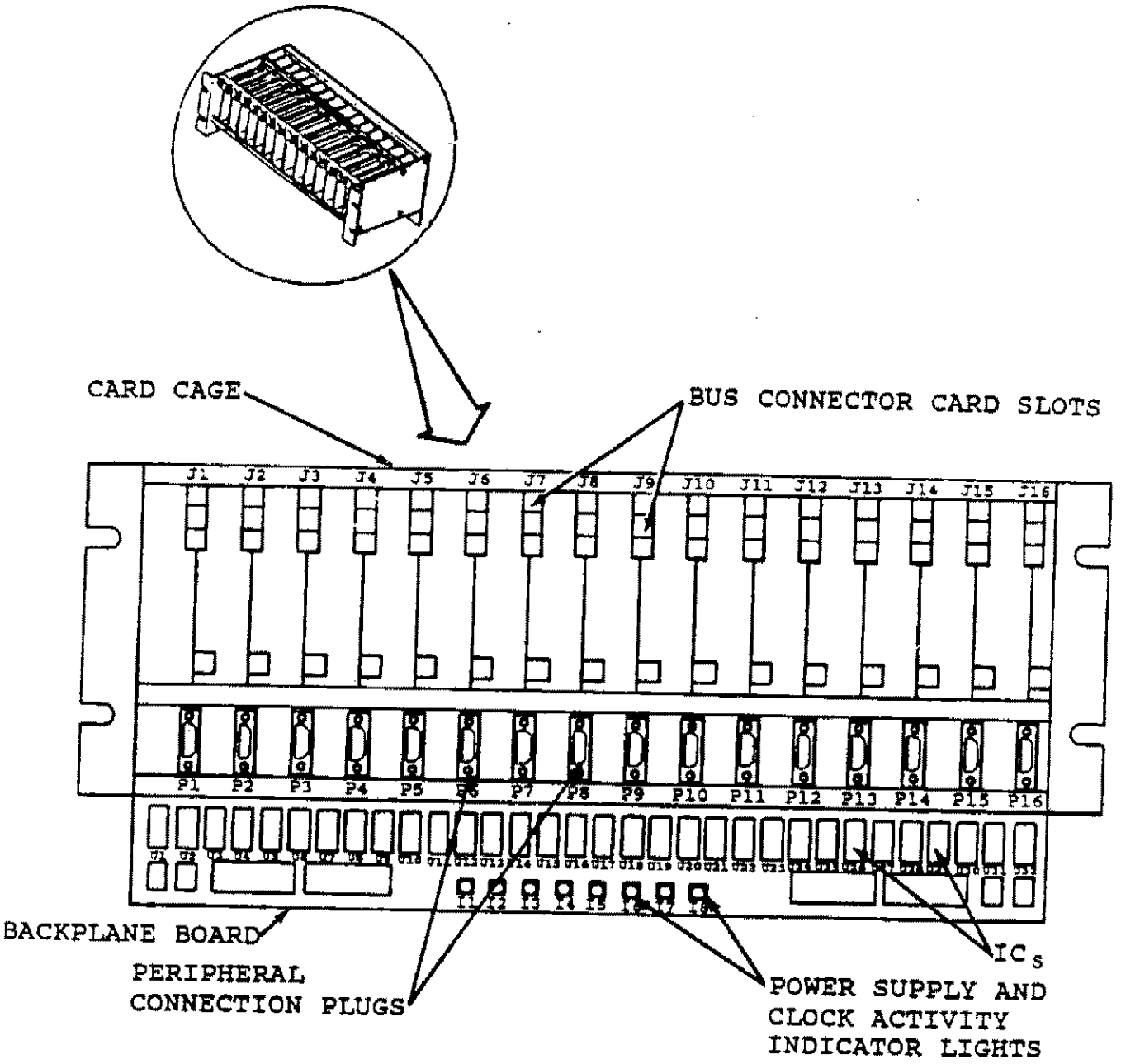
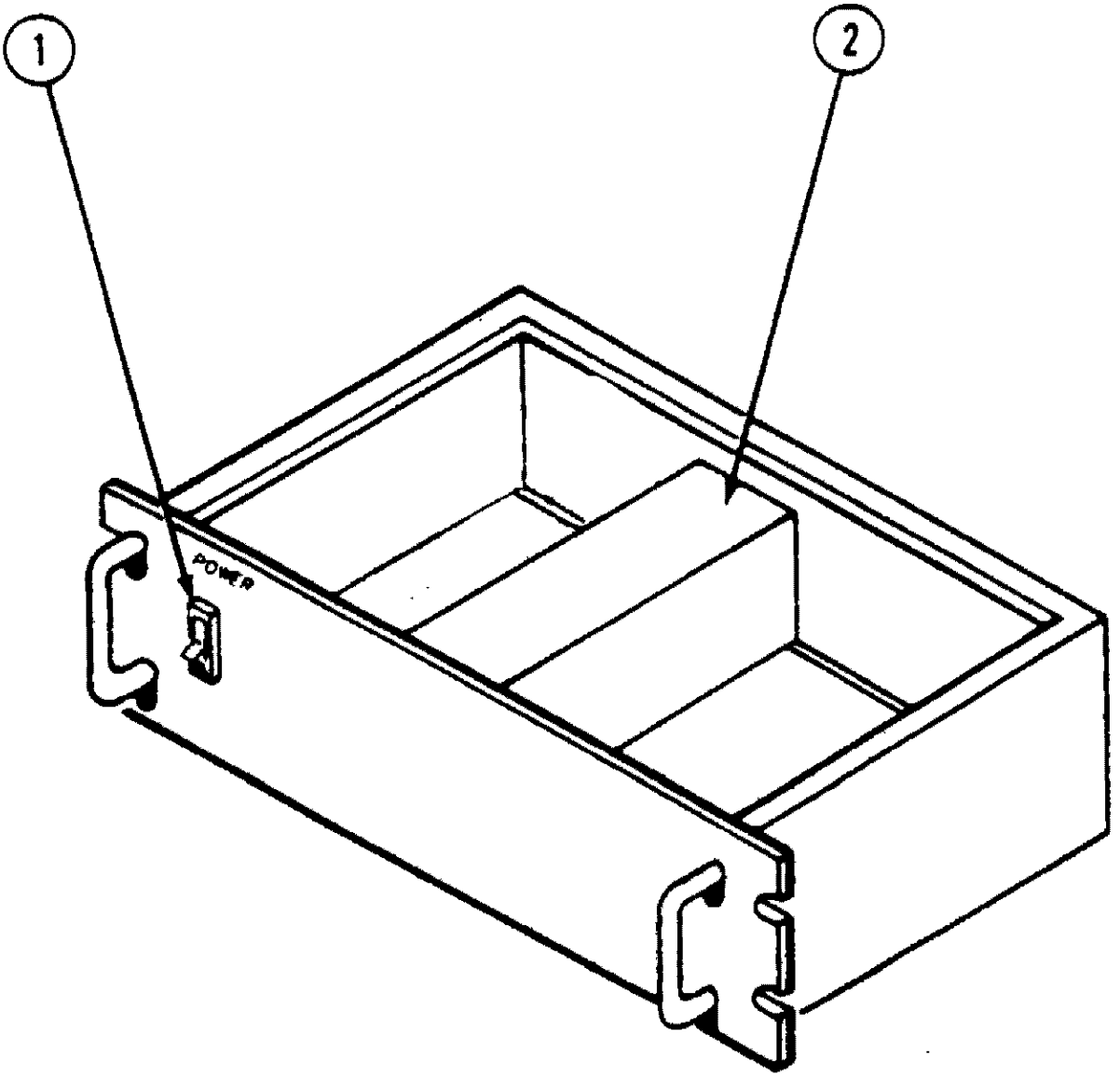
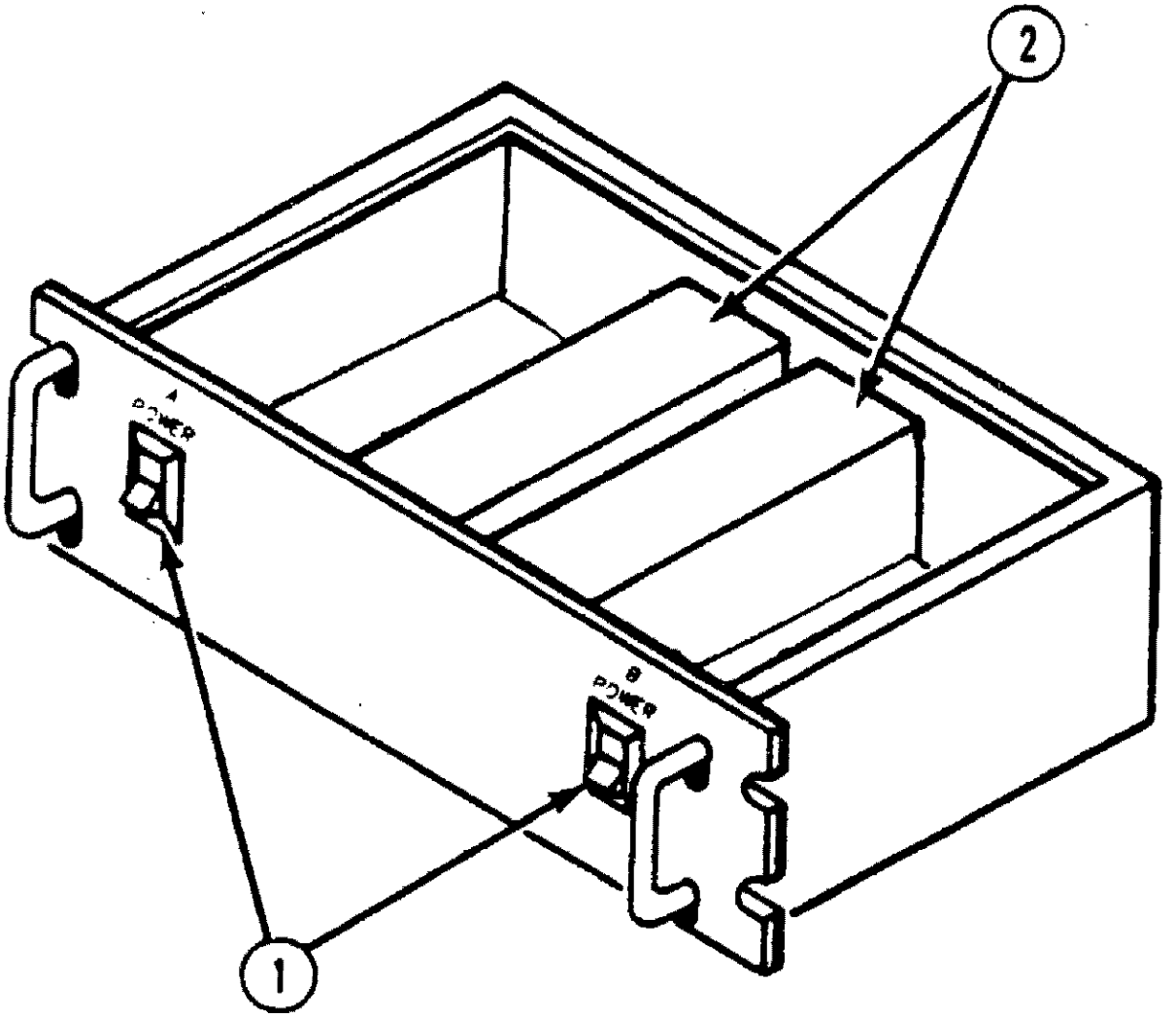


FIGURE 1-27. BC CARD CAGE ASSEMBLY



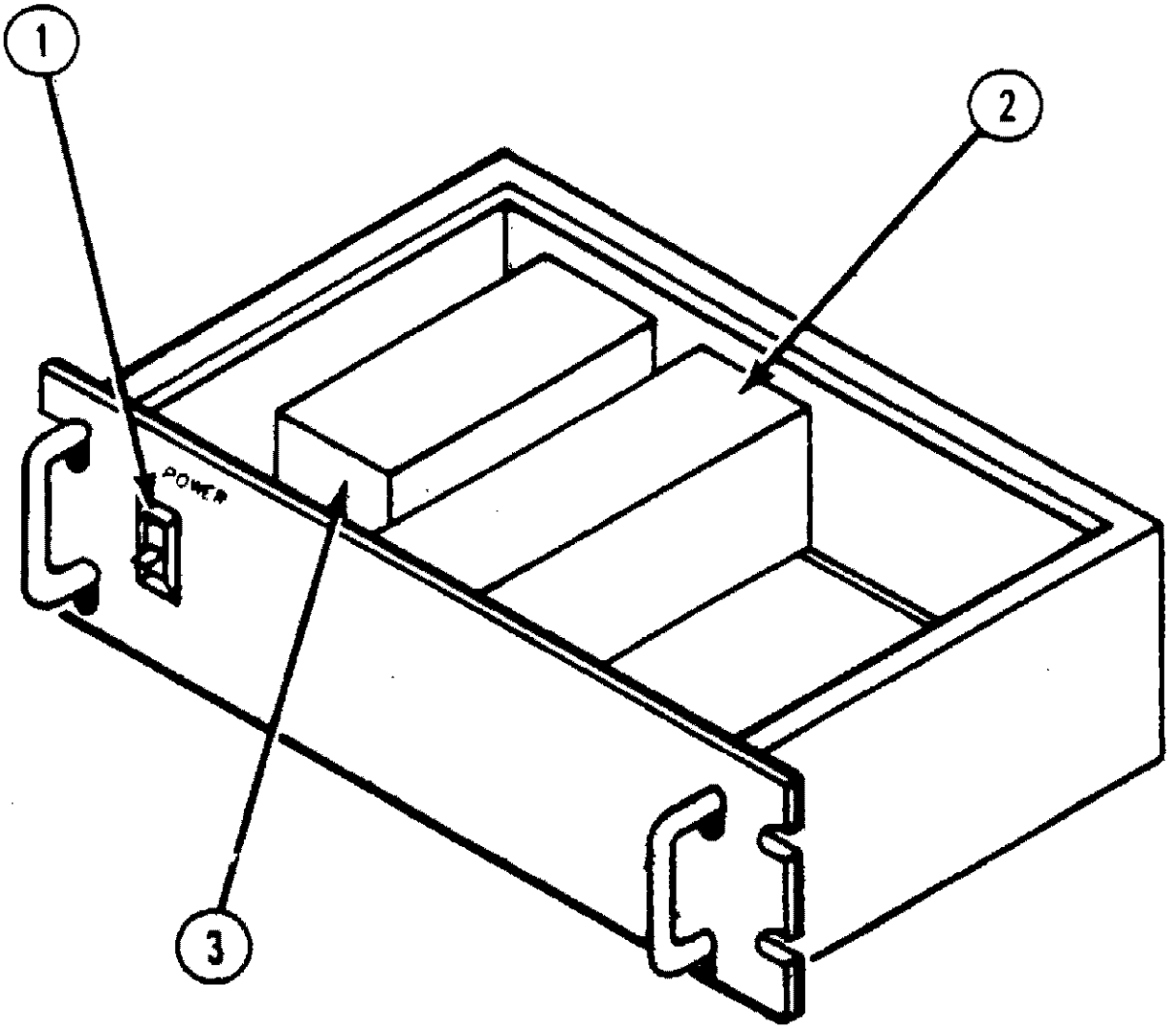
1. A1CB1 2 AMP CIRCUIT BREAKER
2. A1PS1 5 V POWER SUPPLY ASSEMBLY

FIGURE 1-28. SINGLE SINGLE VOLTAGE POWER SUPPLY ASSEMBLY



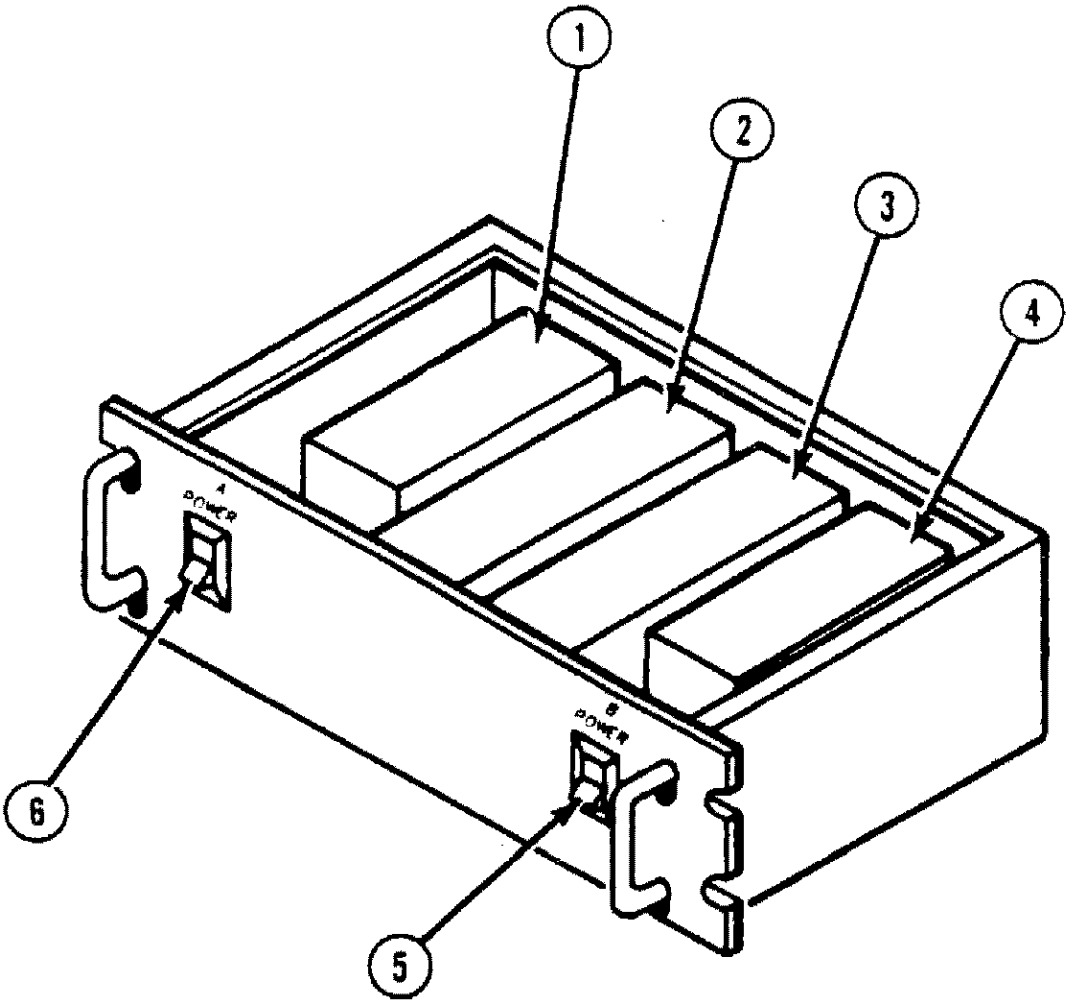
1. A1CB1/A2CB2 2 AMP CIRCUIT BREAKER
2. A1PS1/A2PS2 5 V dc POWER SUPPLY ASSEMBLIES

FIGURE 1-29. DUAL SINGLE VOLTAGE POWER SUPPLY ASSEMBLY



1. A1CB1 2 AMP CIRCUIT BREAKER
2. A1PS2 5 V dc POWER SUPPLY ASSEMBLY
3. A1PS1 ±12 V dc POWER SUPPLY ASSEMBLY

FIGURE 1-30. SINGLE MULTIVOLTAGE POWER SUPPLY ASSEMBLY



1. A1PS1 ±12 V dc POWER SUPPLY ASSEMBLY
2. A1PS2 5 V dc POWER SUPPLY ASSEMBLY
3. A2PS1 5 V dc POWER SUPPLY ASSEMBLY
4. A2PS2 ±12 V dc POWER SUPPLY ASSEMBLY
5. A2CB1 2 AMP CIRCUIT BREAKER
6. A1CB1 2 AMP CIRCUIT BREAKER

FIGURE 1-31. DUAL MULTIVOLTAGE POWER SUPPLY ASSEMBLY

1.3.5.4 AC Power Distribution Assembly. The ac power distribution assembly distributes incoming ac power to the dc power supplies and fan assemblies in the cabinet. The ac power distribution assembly is illustrated in figure 1-32.

1.3.5.5 Fan Assemblies. Fan assemblies provide air circulation for convective cooling of the cabinet assemblies. The CCU/CCU, PCU/PCU, CCU/PCU, CCU, and PCU cabinet assemblies contain two quad fan assemblies, one each in the front section and back section of the cabinet. The RCU and RCU Expanded cabinet assemblies have one dual fan assembly each, located in the front section of the cabinet. The quad fan housing assembly uses two separate power sources. Each power source feeds two of the four fans: if, for any reason, a power source is lost, the other two fans continue to provide air circulation inside the cabinet assembly. Fans in the dual fan housing assembly are supplied by one source of power input.

CAUTION

Front and rear cabinet doors should be opened only for brief intervals in order to maintain proper air circulation in the cabinet assemblies. Failure to comply may damage FDIO equipment.

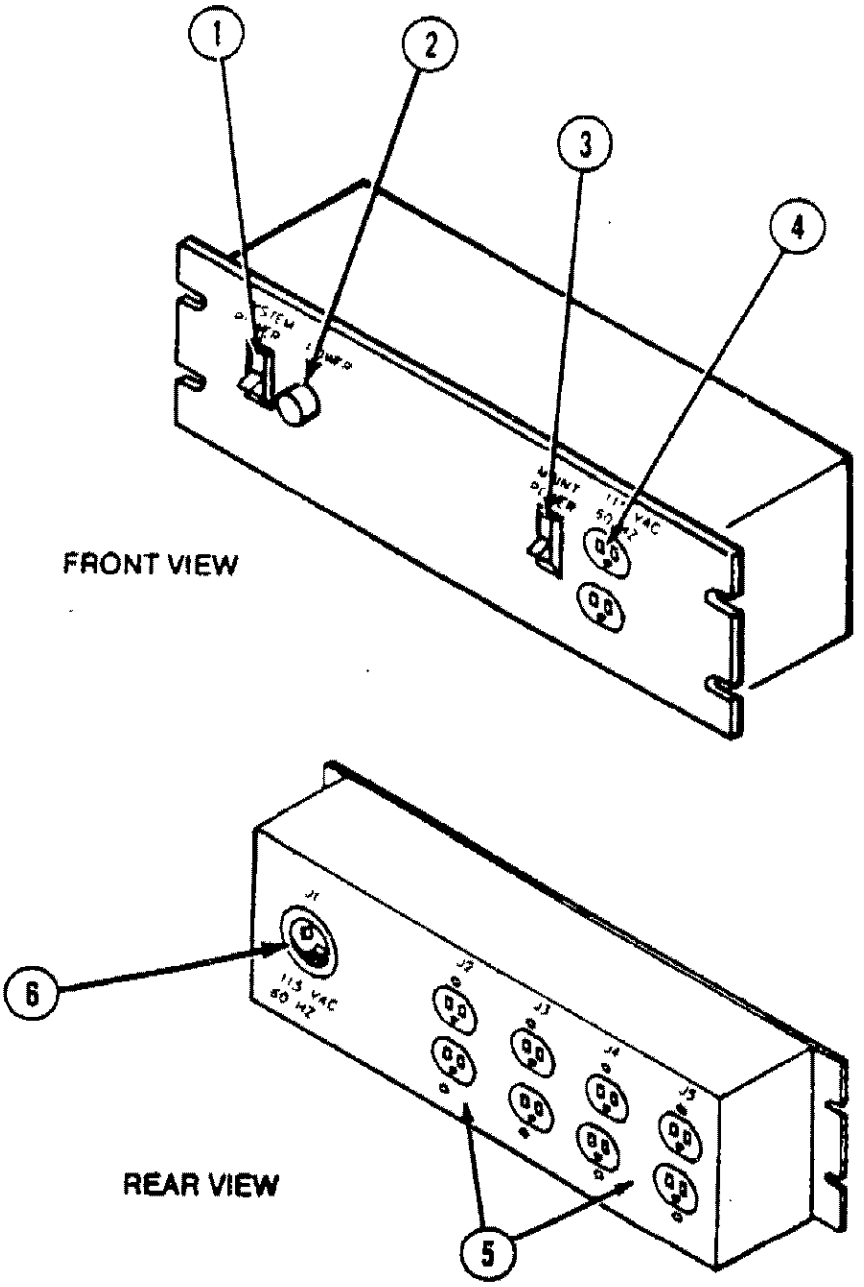
Fan assemblies are illustrated in figure 1-33.

1.3.6 Capabilities and Limitations

FDIO equipment provides an efficient means for data communication between central locations and remote sites. The CCU interfaces the Host and RCUs via RS-232-C and a telephone modem link. With the FDIO system, controllers at the remote sites may enter data into the Host or request data through the en route FDIO message formats.

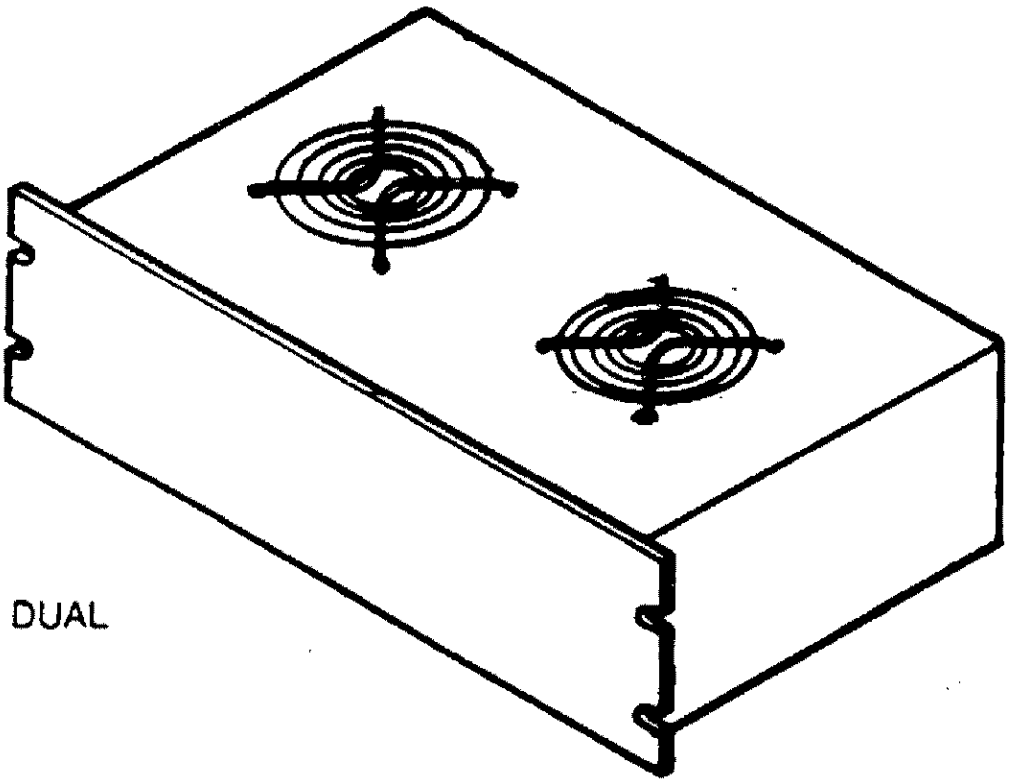
Each RCU interfaces up to: 5 RANKs, 5 CRTs, and 10 RFSPs (maximum combination of 14 peripherals with contract requirements to have a spare slot and a slot for the maintenance channel BC card) with the Host via the CCU and a modem link. RCU Expanded units will handle the full complement of these peripherals.

Each PCU interfaces the Host with up to 28 RFSPs plus one maintenance channel.



1. CB1	15 AMP CIRCUIT BREAKER (SYSTEM)
2. L1	LAMP (SYSTEM PWR ON INDICATOR)
3. CB2	15 AMP CIRCUIT BREAKER (MAINT)
4.	DUPLEX RECEPTACLE (MAINT)
5. J2 THRU J4	DUPLEX RECEPTACLE (SYSTEM)
6. J1	MAIN POWER RECEPTACLE

FIGURE 1-32. AC POWER DISTRIBUTION ASSEMBLY



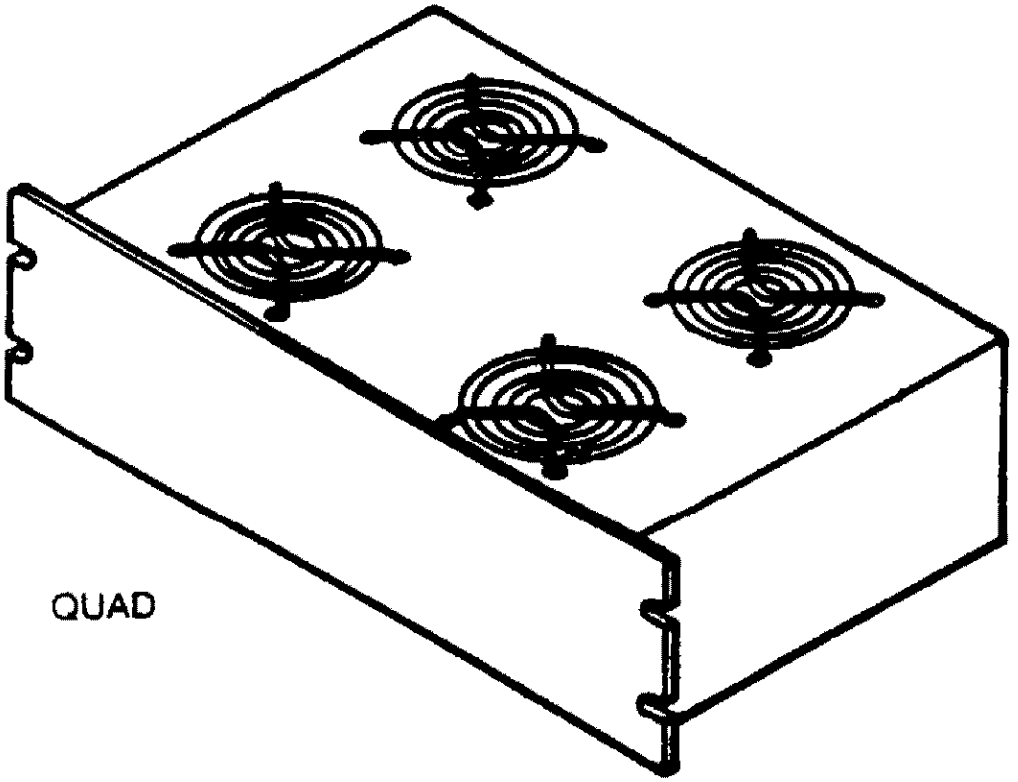


FIGURE 1-33. QUAD AND DUAL FAN HOUSING ASSEMBLIES

1.3.7 Equipment Interface

The following paragraphs provide information on the FDIO equipment interface requirements.

1.3.7.1 Computer Interface. Each PCU or CCU cabinet assembly interfaces with the Host via the GPI and GPO adapters. The computer interface provides the means of transferring messages between the Host and the CCU or PCU cabinet assemblies. The RCU does not require a computer interface.

The GPI portion of the computer interface carries messages from the PCU or CCU cabinet assembly to the Host. The GPO portion of the computer interface carries messages from the Host to the PCU or CCU cabinet assembly.

The computer interface has the following characteristics:

- Format — bit parallel, byte serial
- Parity — 1 bit
- Electrical Interface — IBM
- Data code — Extended Binary Coded Decimal Information Code (EBCDIC)

1.3.7.2 Local Area Network (LAN) Interface. The LAN interface provides communication between the Multibus card cage assembly and the BC boards. PCU and CCU cabinet assemblies use redundant LAN interfaces. The RCU cabinet assembly uses a single LAN interface. The LAN interface has the following characteristics:

- Format — bit serial (8 bits data, no parity), synchronous, full duplex
- Mode — Synchronous Data Link Communication (SDLC) loop
- Protocol — Advanced Data Communication Control Procedures (ADCCP)
- Transfer rate — 19.2 K baud
- Telecommunications Interface — RS-422
- Data code — American Standard for Computer Information Interchange (ASCII)

1.3.7.3 Peripheral Interface. The peripheral interface provides the means of transferring messages between a BC board and a CRT, RANK, or RFSP. The peripheral interface has the following characteristics:

- Format — bit serial (8 bits data, 1 bit parity), asynchronous, full duplex
- Framing — 1 start bit, 1 stop bit
- Transfer rate — 2400 baud
- Telecommunications Interface — RS-422
- Data code — ASCII

1.3.7.4 Modem Interface. The modem interface provides the means of transferring messages between a modem and the control cabinet assembly (BC board or CPU board). The CPU board interfaces the RCU modems and the BC board interfaces the CCU modems. The modem interface has the following characteristics:

- Format — bit serial (8 bits data, 1 bit parity), synchronous, full duplex
- Protocol — ADCCP
- Transfer rate — 2400 baud
- Telecommunications Interface — RS-232
- Data code — ASCII

1.3.7.5 ICL Interface. The ICL interface provides the means of transferring data between redundant CCU and PCU Multibus card cage assemblies. The ICL interface has the following characteristics:

- Format — bit serial (8 bits data, 1 bit parity), synchronous, full duplex
- Framing — 1 start bit, 1 stop bit
- Transfer rate — 19.2 K baud
- Electrical Interface — Transistor-Transistor Logic (TTL)
- Data code — Binary

1.4 EQUIPMENT SPECIFICATION DATA

Equipment specification data including nameplate data, functional characteristics, external power requirements, rated output, and environmental characteristics are outlined in table 1-5.

TABLE 1-5. EQUIPMENT SPECIFICATION DATA

Item	Description
Nameplate Data*	
Equipment title	FDIO SYSTEM
Type	FA10095
Serial number	XXX
Contract number	DTFA01-84-C-00002
Contractor's name	Wespercorp-FSG, Inc.
Contractor's address	14511 New Myford Road, Tustin, CA 92680

*See figure 1-34 for nameplate example.

TABLE 1-5. EQUIPMENT SPECIFICATION DATA (Continued)

Item	Description
Functional Characteristics	
Power	115 V ac
Modes of Operation	CCU, PCU, RCU — Main, Reconfiguration, and Diagnostic CCU and PCU — Primary or Secondary
Signal Output	GPO/GPI — bit parallel, byte serial transmission for CCU and PCU All other communication lines — bit serial (lines to modems are RS-232 and lines to all other peripherals are RS-422)

External Power Requirements

Cabinet Configuration	Maximum Current (Amp)	Voltage	Watts	Power Factor	Surge Current (Amp)
CCU	1.62	115 V ac	138	0.78	12.0
PCU	1.45	115 V ac	130	0.78	12.0
RCU	0.77	115 V ac	69	0.79	8.0
CCU/CCU	3.24	115 V ac	238	0.78	24.0
PCU/PCU	2.90	115 V ac	216	0.80	24.0
CCU/PCU	3.07	115 V ac	227	0.79	24.0
RCU Exp.	0.76	115 V ac	69	0.79	10.0
RFSP (1)	0.11	115 V ac	7.2	-0.60	1.0
RFSP (2)	0.24	120 V ac	12	-0.43	5.0
RFSP (5)	0.26	120 V ac	17.1	0.55	3.0
RANK (6)	0.11	115 V ac	9.8	0.80	0.7
RANK (7)	2.40	115 V ac	48.0	0.80	3.5
CRT (3)	0.14	115 V ac	10.0	-0.60	1.0
CRT (4)	0.61	115 V ac	40.0	-0.57	7.2
CRT (8)	2.00	115 V ac	46.0	-0.51	50.0

Rated Output of Power Supplies: +12 V @ 1.7 A
+5 V @ 12 A

Environmental Characteristics

Ambient Temperature	50° to 100° Fahrenheit	
Relative Humidity	20% to 80% noncondensing	
Heat Dissipation	CCU/CCU	— 274.4 Watts
	PCU/PCU	— 258.4 Watts
	CCU/PCU	— 266.4 Watts
	CCU	— 137.2 Watts
	PCU	— 129.2 Watts
	RCU	— 68.1 Watts
	RFSP (1)	— 7.185 Watts

TABLE 1-5. EQUIPMENT SPECIFICATION DATA

Item	Description
	RFSP (2) — 12 Watts
	RFSP (5) — 17.1 Watts
	RANK (6) — 9.838 Watts
	RANK (7) — 48 Watts
	CRT (3) — 10.02 Watts
	CRT (4) — 40 Watts

NOTE

1. RFSP is the original FDIO printer FA 10095/2
2. RFSP is printer FA 10095/11
3. CRT is the original FDIO video display FA 10095/4
4. CRT is video display FA 10095/12
5. RFSP is IER thermal printer FA 10095/14
6. RANK is FA 10095/3
7. RANK is Touchstone Keyboard FA 10095/17
8. CRT is video display FA 10095/18

FIGURE 1-34. FDIO SYSTEM NAMEPLATE EXAMPLE

1.5 EQUIPMENT AND ACCESSORIES SUPPLIED

Control cabinet configurations and peripheral elements supplied for the FDIO system are listed in table 1-6. Crated dimensions and weight have been omitted because they are not applicable. FDIO equipment will be delivered by padded van and will be protected with a cardboard cover.

TABLE 1-6. EQUIPMENT SUPPLIED (AMERICAN MEASUREMENT)

Qty*	Nomenclature	FAA Number	Dimensions in inches (each)	Weight in pounds (each)	Volume in cubic feet (each)
4	CCU/CCU Cabinet Configuration	FA 10095 uncrated:	h — 70 3/4 w — 24 d — 28 13/16	700-750	28
23	PCU/PCU Cabinet Configuration	FA 10095 uncrated:	h — 70 3/4 w — 24 d - 28 13/16	700-750	28
4	CCU/PCU Cabinet Configuration	FA 10095 uncrated:	h — 70 3/4 w — 24 d - 28 13/16	700-750	28
20	CCU Cabinet Configuration	FA 10095 uncrated:	h — 70 3/4 w — 24 d — 28 13/16	400-425	28
4	PCU Cabinet Configuration	FA 10095 uncrated:	h — 70 3/4 w — 24 d — 28 13/16	400-425	28
476	RCU Cabinet Configuration	FA 10095 uncrated:	h — 70 3/4 w — 24 d — 28 13/16	400-425	28
2	RCU Expanded Cabinet Configuration	FA 10095 uncrated:	h — 70 3/4 w — 24 d — 28 13/16	400-425	28

TABLE 1-6. EQUIPMENT SUPPLIED (AMERICAN MEASUREMENT) (Continued)

Qty*	Nomenclature	FAA Number	Dimensions in inches (each)	Weight in pounds (each)	Volume in cubic feet (each)
837	RANK	FA 10095/3			
		uncrated:	h — 3.25 w — 14.50 d — 10.25	25	0.283
100	RANK	FA 10095/17			
		uncrated:	h — 2.75 w — 14.00 d — 8.00	10	0.18
690	CRT	FA 10095/4			
		uncrated:	h — 14.50 w — 14.25 d — 14.25	25	1.71
825	CRT	FA 10095/12			
		uncrated:	h — 10.50 w — 12.25 d — 13.00	18	0.968
2000	CRT	FA 10095/18			
		uncrated:	h —13.04 w — 12.50 d — 13.00	29	1.226
2618	RFSP	FA 10095/2			
		uncrated:	h — 7.00 w — 17.00 d — 13.25	35	0.896
2625	RFSP	FA 10095/11			
		uncrated:	h — 5.20 w — 17.40 d — 14.30	21	0.749
800	RFSP	FA 10095/14			
		uncrated:	h — 9.06 w — 8.03 d — 18.11	17.6	0.762

1.6 DOCUMENTATION SUPPLIED

Documentation pertinent to FDIO system hardware maintenance and operation is listed in table 1-7.

TABLE 1-7. DOCUMENTATION SUPPLIED

Qty	Nomenclature	Document Number
21	Hardware Design Data	FAA — TI 6130.6
21	System Design Data	FAA — CLIN-51.a
4	Flight Data Input/Output (FDIO) PCB Fault Isolation Test Procedures (September 25, 1986)	FAA — CLIN-54.1.C1
21	FDIO Printer (RFSP) FA 10095/2 Operators Manual Rev. C (December 1986)	M2501010
21	FDIO Printer (RFSP) FA 10095/2 Technical Manual Rev. B (December 1986)	M2501010T
21	FDIO Printer (RFSP) FA 10095/2 Illustrated Parts Manual Rev. B (December 1986)	M2501010I
21	FDIO Printer (RFSP) FA 10095/2 P-Card Reference Manual Rev. B (December 1986)	M2501010P
2625	RFSP (FA 10095/11) Model 9034/9044 Operating Guide Edition B (October 1988)	291814-001
10	RFSP (FA 10095/11) Technical and Illustrated Parts Manual	
800	RFSP IER 512 Printer (FA 10095/14) User Guide Ref. Rev. Level 2, 12/13/96	N07102A
1	RFSP (FA 10095/14) Illustrated Parts Catalog Ref. Edition 1, 11/1996	N07133A
21	FDIO CRT (FA 10095/4) Operator and Technical Manual (September 1985) Part One — Operator/Programmer Information Part Two — Technical Information	None
10	CRT (FA 10095/12) Programmers Manual Revision A	210089-100
10	CRT (FA 10095/12) Technical Manual	

TABLE 1-7. DOCUMENTATION SUPPLIED (Continued)

Qty	Nomenclature	Document Number
825	CRT (FA 10095/12) Quick Setup Guide	
21	iSBC 88/45 Advanced Data Communications Processor Board Hardware Reference Manual	143824-003

1.7 EQUIPMENT REQUIRED BUT NOT SUPPLIED

FSG, Inc. will supply all equipment needed for the FDIO operation except the Host computer and modems required for data transmittal. All modem units will be furnished by the customer for this application.

2.0 TECHNICAL DESCRIPTION

2.1 SIMPLIFIED THEORY OF OPERATION

The FDIO electronic hardware system consists of the following five assemblies and peripherals:

4. Host interface
5. Multibus cardcage assembly
6. Front panel assembly
7. LAN assembly
8. RFSP, CRT, and RANK

Each assembly consists of several units that are replaceable by a site maintenance technician.

2.1.1 Host Interface

The Host interface consists of the following five units as shown in figures 11-1 and 11-2 (1):

1. GPI PAMRI interface cable assembly
2. GPO PAMRI interface cable assembly
3. GPI/GPO interface board
4. GPI/GPO interface cable assembly
5. Terminator board

NOTE

This interface is common to the CCU and PCU and is not found in an RCU.

The purpose of the Host interface is to provide the electrical communication interface between the Host computer system and the CCU or PCU.

The CCU and PCU receive messages from the Host PAMRI adapter via the GPO PAMRI interface cable and send messages via the GPI PAMRI interface cable. These cables are connected to the Host PAMRI and to the GPI/GPO interface board located in the bottom portion of the control cabinet. The connection is made via circular bayonet type connectors. The GPI/GPO interface board sends and receives GPI and GPO interface signals and routes them to the GPI or GPO interface cable.

The GPI/GPO interface cable routes GPI and GPO interface signals through the cabinet to the Multibus cardcage assembly where it connects to the primary and secondary control unit utility boards. The cable also routes the GPI/GPO interface signals to the GPI/GPO terminator board located on the top Multibus assembly, where the signals are electrically terminated.

2.1.1.1 Power Distribution. The Host interface requires no external power because it contains no active elements. It acts only as a conduit for the GPI/GPO interface signals.

2.1.1.2 Inputs. The CCU and PCU receive messages from the Host in bit parallel, byte serial fashion, via the GPO PAMRI interface cable. This cable contains eight data lines, a parity line, and handshake and status lines. Table 2-1 describes the active GPO interface signals.

GPI messages entering the Host interface from the Multibus cardcage assembly first the pass through the utility board of the primary CCU or PCU.

TABLE 2-1. GPO INTERFACE SIGNAL DEFINITION

Interface Signal Names	Input [I] Output [O]	Function (note 1)
		DATA LINES
GPO DATA0	[I]	Most significant data bit
GPO DATA1	[I]	
GPO DATA2	[I]	
GPO DATA3	[I]	(Data is in 8-bit NAS format)
GPO DATA4	[I]	
GPO DATA5	[I]	
GPO DATA6	[I]	
GPO DATA7	[I]	Least significant data bit
GPO PARITY	[I]	Parity bit added to data bits
		HANDSHAKE LINES
ADAPTER SELECT	[I]	NAS is ready to communicate via GPO
GPOIOREQ	[O]	CCU or PCU is ready to receive a character
GPO ADAPTER RESPONSE	[I]	Character available from Host
GPO EOM	[I]	End of Message (EOM)
DEVICE INOP	[O]	CCU or PCU is available to receive data from the Host (note 2)
		DEVICE STATUS LINES
DSL3	[O]	Device Status Line 3 (CCU or PCU has received a parity error)

TABLE 2-1. GPO INTERFACE SIGNAL DEFINITION (Continued)

Interface Signal Names	Input [I] Output [O]	Function (note 1)
DSL5	[O]	Device Status Line 5 (CCU or PCU internal receive buffer has overflowed)
DSL6	[O]	Device Status Line 6 (CCU or PCU requests that the Host resend the message)

NOTE

1. All interface signals are active when they are high.
2. The device inoperative line is active (high) when FDIO is operative (i.e. available to receive data from the Host).

2.1.1.3 Outputs. The GPO messages and handshake signals received from the Host are output to the Multibus cardcage assembly via the utility board for processing by the FDIO system firmware and hardware.

The CCU and PCU send messages to the Host in bit parallel, byte serial fashion, via the GPI PAMRI interface cable. This cable contains eight data lines, a parity line, and handshake and control lines. Table 2-2 describes the active GPI interface signals.

TABLE 2-2. GPI INTERFACE SIGNAL DEFINITION

Interface Signal Names	Input [I] Output [O]	Function (note 1)
		DATA LINES
GPI DATA0	[O]	Most significant data bit
GPI DATA1	[O]	
GPI DATA2	[O]	
GPI DATA3	[O]	(Data is in 8-bit NAS format)
GPI DATA4	[O]	
GPI DATA5	[O]	
GPI DATA6	[O]	
GPI DATA7	[O]	Least significant data bit
GPI PARITY	[O]	Parity bit added to data bits

TABLE 2-2. GPI INTERFACE SIGNAL DEFINITION (Continued)

Interface Signal Names	Input [I] Output [O]	Function (note 1)
		HANDSHAKE LINES
GPIIOREQ	[O]	Request by CCU or PCU to send a character
GPI ADAPTER RESPONSE	[I]	Acknowledgment of the character by the Host
GPI EOM	[O]	EOM
		DEVICE CONTROL LINES
DCL1	[I]	Device Control Line 1 (Host is ready to accept)
DCL3	[I]	Device Control Line 3 (Host received parity error)
DCL4	[I]	Device Control Line 4 (Force control unit switch, note 2.)

NOTE

1. All interface signals are active when they are high.
2. A control unit switch occurs if DCL1, DCL3 and DCL4 are all active at the same time.

2.1.1.4 Theory of Operation

2.1.1.4.1 GPI PAMRI Interface Cable Assembly. This cable connects the Host PAMRI to the FDIO system. The cable terminates at the PAMRI by a 24-pin serpentine connector and at the FDIO by a 24-pin round bayonet type connector. Strain reliefs at each end contribute to the mechanical and electrical integrity of the cable. The cable itself contains fifteen separate coaxial shielded lines. The active GPI signal is transmitted through the central conductor with the outer shield being connected at each end to electrical ground.

2.1.1.4.2 GPO PAMRI Interface Cable Assembly. This cable connects the Host PAMRI to the FDIO system. The cable terminates at the PAMRI by a 24-pin serpentine connector and at the FDIO by a 24-pin round bayonet type connector. Strain reliefs at each end contribute to the mechanical and electrical integrity of the cable. The cable itself contains eighteen separate coaxial shielded lines. The active GPO signal is transmitted through the central conductor with the outer shield being connected at each end to electrical ground.

2.1.1.4.3 GPI/GPO Interface Board. This board provides the transition medium between the GPI and GPO PAMRI interface cables connected to the Host PAMRI and the internal GPI/GPO cable that routes the GPI or GPO signals within FDIO. GPI or GPO signals enter the GPI/GPO interface board via the 24-pin round bayonet connectors (J1 and J2) and exit via the 40-pin edge connector (J3).

2.1.1.4.4 GPI/GPO Interface Cable Assembly. This cable routes the GPI or GPO signals within the FDIO cabinet and consists of a 40-pin ribbon cable using mass-termination Insulation Displacement Connection (IDC) technology. The cable distributes the signals to the Multibus cardcage assemblies (utility boards) of the primary and secondary PCUs and CCUs. Connector P4 connects to the GPI/GPO interface board in the bottom of the control unit cabinet. Connector P3 connects to J3 of the utility board in the lower control unit position, and connector P2 connects to J3 of the utility board in the upper control unit position. Connector P1 of the cable connects to P1 of the terminator board.

2.1.1.4.5 Terminator Board. The terminator board electronically terminates all active GPI and GPO signals by connecting a 100 Ohm resistor between the signal and ground. This ensures proper transmission line characteristics to minimize unwanted signal noise, ringing, and other spurious signals.

2.1.2 Multibus Cardcage Assembly

The Multibus cardcage assembly differs for the CCU, PCU, and RCU.

2.1.2.1 CCU and PCU Multibus Cardcage Assembly. The CCU and PCU consist of primary and secondary control units. Each control unit contains a Multibus cardcage assembly. Communication occurs between the primary and secondary control units via the FSE and ICL cables. The primary and secondary CCU and PCU Multibus cardcage assembly consists of the following seven units as shown in figures 11-1 and 11-2 (2):

1. Multibus backplane
2. iSBC 88/45 processor board
3. Utility board
4. Front panel interface board
5. LAN interface adapter board
6. FSE cable
7. ICL cable

The Multibus backplane electrically connects the iSBC 88/45 processor board and the utility board, and distributes power. The iSBC 88/45 processor board contains the microprocessor, system program, data memory, and support circuitry. The utility board contains the interface to the Host interface, expansion data memory, and the redundant control unit logic. The front panel interface board provides the communication link with the front panel assembly. The LAN interface adapter board provides the transition for the signals from the iSBC 88/45 processor board to the LAN assembly. The FSE and ICL cables are the hardware link between the primary and secondary control units.

GPI and GPO signals between the Host interface and the utility board travel through J3 on the utility board. The utility board contains the hardware and firmware for the handshake protocol with the Host. Messages from the Host are received character by character via the GPO interface and are stored in system Random Access Memory (RAM). When the entire message is received and buffered, it is decoded and processed. Text messages received by a control unit are processed and sent to the LAN assembly for distribution to the various peripheral devices. Messages that are not text messages cause internal operations to be performed.

Responses and acknowledgments received by the control unit from the various peripheral devices are sent via the LAN assembly and are processed in the Multibus cardcage assembly. If the message

is being sent to the Host, hardware and firmware on the utility board performs the handshake protocol and transmits the message byte by byte to the Host via the Host interface.

Error messages and operator prompt messages for display on the front panel are transmitted to the front panel assembly via the front panel interface board attached to the iSBC 88/45 processor board. Front panel keyboard entries are sensed by hardware on the front panel interface board and made available to the system firmware on the iSBC 88/45 processor board.

Communication between the primary and secondary control units occurs through hardware on the utility board and the FSE and ICL cables.

2.1.2.2 RCU Multibus Cardcage Assembly. The RCU is not redundant and contains only one Multibus cardcage assembly. There is no utility board in the RCU because the RCU does not communicate with the Host interface. The RCU Multibus cardcage assembly consists of the following five units as shown in figure 11-3 and 11-4 (2):

1. Multibus backplane
2. iSBC 88/45 processor board
3. Front panel interface board
4. 16 K RCU memory expansion board
5. LAN interface adapter board

The Multibus backplane electrically connects the iSBC 88/45 processor board and the 16 K RCU memory expansion board, and distributes power. The iSBC 88/45 processor board contains the microprocessor, system program, data memory, and support circuitry. The front panel interface board provides the communication link with the front panel assembly. The 16 K RCU memory expansion board increases the amount of buffer memory for the RCU. The LAN interface adapter board transitions the signals from the iSBC 88/45 processor board to the LAN assembly.

Messages or responses transmitted over the modem link between the CCU and RCU modem interface (connector J2 on the iSBC 88/45 processor board) are conveyed via J2 on the plate connector interface. These messages are received bit serially using ADCCP protocol. The modem serial interface in the iSBC 88/45 processor board receives the message and stores it in RAM. After the entire message is received and buffered, it is decoded and processed. Text messages in the RCU are processed and sent to the LAN assembly for distribution to the RFSP and CRT peripheral devices. Messages that are not text messages cause internal operations to be performed.

Messages received from RFSP, CRT, or RANK are sent to the LAN assembly and processed in the Multibus cardcage assembly. If the message is sent to the CCU or to the Host via the CCU, the message is transmitted over the serial modem interface.

Error messages and operator prompt messages for display on the front panel are transmitted to the front panel assembly via the front panel interface board attached to the iSBC 88/45 processor board. Front panel keyboard entries are sensed by hardware on the front panel interface board and made available to the system firmware on the iSBC 88/45 processor board.

2.1.2.3 Power Distribution. Power is distributed to the Multibus cardcage assembly through the Multibus backplane. The CCU and PCU require +5 V dc (see figures 11-1 and 11-2). The RCU and the RCU expanded require +5 V dc and ±12 V dc (see figures 11-3 and 11-4). Each redundant

CCU or PCU Multibus cardcage receives power from a separate power supply via connectors J6 and J8 and a power cable. The RCU has only a single power supply assembly. The Multibus backplane distributes the power to the iSBC 88/45 board and the utility board (CCU or PCU), or 16 K RCU memory expansion board. Power for the front panel interface board is obtained from the iSBC 88/45 processor board.

2.1.2.4 Inputs. Inputs to the Multibus cardcage assembly are from one of six sources described below:

	SOURCE	DESCRIPTION
1.	Host interface (CCU or PCU):	GPO messages received from the Host enter the Multibus cardcage assembly via J3 on the utility board. See table 2-3.
2.	CCU messages (RCU):	Messages received from the CCU via the modem enter the Multibus cardcage assembly via J2 on the iSBC 88/45 board. See table 2-4.
3.	LAN assembly:	Messages received from the LAN assembly enter the Multibus cardcage assembly via J1 on the LAN interface adapter board. See table 2-5.
4.	Front panel assembly:	Keypad entries from the front panel enter the Multibus cardcage assembly via J1 on the front panel interface board. See table 2-6.
5.	FSE cable:	Discrete signals sent by the redundant control unit enter the Multibus cardcage assembly via J1 on the utility board. See table 2-7.
6.	ICL cable:	Serial messages sent by the redundant control unit enter the Multibus cardcage assembly via J2 on the utility board. See table 2-8.

2.1.2.5 Outputs. Outputs from the Multibus cardcage assembly are sent to one of six destinations described below:

	DESTINATION	DESCRIPTION
1.	Host interface (CCU or PCU):	GPI messages to be sent to the Host exit the Multibus cardcage assembly via J3 on the utility board. See table 2-3.
2.	CCU messages (RCU):	Messages to be sent to the CCU via the modem exit the Multibus cardcage assembly via J2 on the iSBC 88/45 board. See table 2-4.
3.	LAN assembly:	Messages for the LAN assembly exit the Multibus cardcage assembly via J1 on the LAN interface adapter board. See table 2-5.
4.	Front panel assembly:	Messages to be displayed on the control unit front panel display exit the Multibus cardcage assembly via J1 on the front panel interface board. See table 2-6.
5.	FSE cable:	Discrete signals to be sent to the redundant control unit exit the Multibus cardcage assembly via J1 on the utility board. See table 2-7.
6.	ICL cable:	Serial messages to be sent to the redundant control unit exit the Multibus cardcage assembly via J2 on the utility board. See table 2-8.

TABLE 2-3. GPI/GPO INTERFACE CABLE SIGNAL DEFINITIONS

Interface Signal Names	Input [I] Output [O]	Function (note 1)
		GPI DATA LINES
GPI DATA0	[O]	Most significant data bit
GPI DATA1	[O]	
GPI DATA2	[O]	
GPI DATA3	[O]	(Data is in 8-bit NAS format)
GPI DATA4	[O]	
GPI DATA5	[O]	
GPI DATA6	[O]	
GPI DATA7	[O]	Least significant data bit
GPI PARITY	[O]	Parity bit added to data bits
		GPO DATA LINES
GPO DATA0	[I]	Most significant data bit
GPO DATA1	[I]	
GPO DATA2	[I]	
GPO DATA3	[I]	(Data is in 8-bit NAS format)
GPO DATA4	[I]	
GPO DATA5	[I]	
GPO DATA6	[I]	
GPO DATA7	[I]	Least significant data bit
GPO PARITY	[I]	Parity bit added to data bits
		GPI HANDSHAKE LINES
GPIIOREQ	[O]	Request by CCU or PCU to send a character
GPI ADAPTER RESPONSE	[I]	Acknowledgment of the character by the Host
GPI EOM	[O]	EOM

TABLE 2-3. GPI/GPO INTERFACE CABLE SIGNAL DEFINITIONS (Continued)

Interface Signal Names	Input [I] Output [O]	Function (note 1)
		GPO HANDSHAKE LINES
ADAPTER SELECT	[I]	NAS is ready to communicate via GPO
GPOIOREQ	[O]	CCU or PCU is ready to receive a character
GPO ADAPTER RESPONSE	[I]	Character available from Host
GPO EOM	[I]	EOM
DEVICE INOP	[O]	CCU or PCU is available to receive data from the Host (note 2)
		GPI DEVICE CONTROL LINES
DCL1	[I]	Device Control Line 1 (Host is ready to accept)
DCL3	[I]	Device Control Line 3 (Host received parity error)
DCL4	[I]	Device Control Line 4 (Force control unit switch, note 3.)
		GPO DEVICE STATUS LINES
DSL3	[O]	Device Status Line 3 (CCU or PCU has received a parity)
DSL5	[O]	Device Status Line 5 (CCU or PCU receive buffer has overflowed)
DSL6	[O]	Device Status Line 6 (CCU or PCU requests that the Host resend the message)

NOTE

1. All interface signals are active when they are high.
2. The device inoperative line is active (high) when FDIO is operative (i.e., available to receive data from the Host).
3. A control unit switch occurs if DCL1, DCL3, and DCL4 are all active at the same time.

TABLE 2-4. MODEM INTERFACE SIGNAL DEFINITION

Interface Signal Names	Input [I] Output [O]	Function
		SERIAL DATA LINES
TXD	[O]	RS-232 transmit data line
TXC	[O]	RS-232 transmit clock line
RXD	[I]	RS-232 receive data line
RXC	[I]	RS-232 receive clock line
		GROUND LINES
SIG GND		RS-232 ground reference

TABLE 2-5. LAN INTERFACE SIGNAL DEFINITION

Interface Signal Names	Input [I] Output [O]	Function
		SERIAL DATA LINES
+ TXD	[O]	RS-422 serial transmit
-TXD	[O]	RS-422 serial transmit
+ RXD	[I]	RS-422 serial receive
-RXD	[I]	RS-422 serial receive
		CLOCK LINES
+ TXC	[O]	RS-422 transmit clock line
-TXC	[O]	RS-422 transmit clock line
+ RXC	[I]	RS-422 receive clock line
-RXC	[I]	RS-422 receive clock line
		GROUND LINES
GND		RS-422 ground reference

TABLE 2-6. FRONT PANEL INTERFACE SIGNAL DEFINITION

Interface Signal Names	Input [I] Output [O]	Function
		LIQUID CRYSTAL DISPLAY (LCD) DATA LINES
LCD display data bits		
PA7	[O]	Display DATA7 Most Significant Bit (MSB)
PA6	[O]	Display DATA6
PA5	[O]	Display DATA5
PA4	[O]	Display DATA4
PA3	[O]	Display DATA3
PA2	[O]	Display DATA2
PA1	[O]	Display DATA1
PA0	[O]	Display DATA0 Least Significant Bit (LSB)
		LCD CONTROL LINES
PC2	[O]	LCD Data Enable (DEN) line
PC1	[O]	LCD Data Read/Write (DRW) select line
PC0	[O]	LCD Data Read/Select (DRS) line
		ALARM LINE
PC3	[O]	Alarm line
		KEYBOARD LINES
RL7	[I]	Column 7 return line
RL6	[I]	Column 6 return line
RL5	[I]	Column 5 return line
RL4	[I]	Column 4 return line
RL3	[I]	Column 3 return line
RL2	[I]	Column 2 return line
RL1	[I]	Column 1 return line
RL0	[I]	Column 0 return line
SL3	[O]	Select row 3 line
SL2	[O]	Select row 2 line
SL1	[O]	Select row 1 line
SL0	[O]	Select row 0 line

TABLE 2-6. FRONT PANEL INTERFACE SIGNAL DEFINITION (Continued)

Interface Signal Names	Input [I] Output [O]	Function
SHFT	[I]	Shift input (not used)
CTRL	[I]	Control input (not used)

TABLE 2-7. FSE CABLE DEFINITION

Interface Signal Names	Input [I] Output [O]	Function
		CONTROL LINES
WDOUT/	(O)	Watchdog timer output pulse to redundant control unit
WDOUT ECHO/	(I)	Watchdog timer output pulse echo from redundant control unit
WDIN/	(I)	Watchdog timer input pulse from redundant control unit
WDIN ECHO/	(O)	Watchdog timer input pulse echo to redundant control unit
XRELCMDIN/	(I)	Request from redundant control unit to release the transmitter
XRELCMDOUT/	(O)	Request to redundant control unit to release the transmitter
XMTRAVAIL	(I/O)	Signal common to both control units indicating the transmitter is available
FSECABLE/	(I/O)	Indicates presence of FSE cable
		GROUND LINES
GND		FSE ground reference

NOTE

/ = negative active low

TABLE 2-8. ICL SIGNAL CABLE DEFINITION

Interface Signal Names	Input [I] Output [O]	Function
		SERIAL DATA LINES
TXDA	[O]	Serial transmit channel A
TXDB	[O]	Serial transmit channel B
RXDA	[I]	Serial receive channel A
RXDB	[I]	Serial receive channel B
		CONTROL LINES
IORQOUT	[O]	I/O REQUEST signal to redundant control unit
IORQIN	[I]	I/O REQUEST signal from redundant control unit
ICLCABLE/	[I]	Indicates presence of ICL cable
		GROUND LINES
GND		ICL ground reference

2.1.2.6 Theory of Operation

2.1.2.6.1 Multibus Backplane. The Multibus backplane is part of the Multibus cardcage that can accommodate up to four expansion boards. The Multibus backplane is an 86-pin bus containing address, data, control, and interrupt lines that allow Multibus compatible boards to communicate with each other and share resources.

In the CCU and PCU, the iSBC 88/45 processor board and the utility board are installed in the cardcage. The iSBC 88/45 processor board is the central processing unit and the utility board is an expansion board containing extra data memory and specialized I/O circuits that are managed by the iSBC 88/45 processor board. In the RCU, the iSBC 88/45 processor board and the 16 K RCU memory expansion board are installed in the Multibus cardcage.

2.1.2.6.2 iSBC 88/45 Processor Board. The iSBC 88/45 processor board is a Multibus compatible board that plugs into the Multibus backplane at location J1. The iSBC 88/45 is the central processing unit for the control unit and contains the 8088 microprocessor, system Erasable Programmable Read-Only Memory (EPROM), and 16 Kb of system RAM. The iSBC 88/45 processor board contains support functions such as the interrupt control circuitry, Direct Memory Access (DMA) logic, and several serial I/O interfaces.

The iSBC 88/45 board is configured for the FDIO system. The major circuits of the iSBC 88/45 board are described below:

CIRCUITS	DESCRIPTION
1. Central processor unit (CPU):	An 8088 microprocessor chip is the foundation of the CPU which executes the instructions contained in program memory to perform the FDIO operations.

CIRCUITS	DESCRIPTION
2. 64 Kb of program memory:	64 Kb of EPROM are available for program memory.
3. 16 Kb of data memory (RAM):	RAM is used to store program variables, buffer FDIO messages and support the stack space required by the firmware. The DMA buffer used to transmit andreceive LAN messages resides in this RAM.
4. Serial LAN interface:	The LAN interface is a serial communications controller using an 8273 Large Scale Integration (LSI) micro-chip. The interface is controlled by the CPU and provides parallel to serial and serial to parallel conversion of the FDIO messages so they can be transmitted and received over the LAN interface. The LAN interface is an SDLC loop configured and uses ADCCP protocol. The LAN interface signals are present on connector J1 to which the LAN interface board is attached.
5. DMA circuit for LAN:	The LAN transmit and receive interface operation uses DMA cycle stealing techniques to minimize the overhead on system hardware and firmware. When a character is received from the LAN by the serial communications controller, the DMA controller automatically stores the received character in RAM when the CPU is not using the memory. A character that is ready to be transmitted, is fetched from memory for output to the serial communications controller. The DMA controller automatically stores the transmitted character in RAM when the CPU is not using the memory.
6. Serial modem interface (RCU):	The modem interface is a serial communications controller using one channel of the 8274 LSI micro chip. The modem interface is controlled by the CPU and provides parallel to serial and serial to parallel conversion of the FDIO messages so they can be transmitted and received over the serial modem interface to the CCU. The modem interface uses ADCCP protocol. The modem interface signals are present on connector J2 to which the modem cable is attached in the RCU.
7. Programmable baud rate generators:	Two internal hardware timers are configured as baud rate generators and provide the 19,200 baud clock for the LAN interface and the 2400 baud clock for the modem interface.
8. Programmable interval timer:	A programmable hardware interval timer generates a clock fed to the interrupt controller to provide a real time system interrupt every 5 milliseconds.
9. System interrupt control:	A Programmable Interrupt Controller (PIC) controls the sensing and reporting of up to eight external interrupt requests to the 8088 processor. The interrupt controller can accept, mask, and arbitrate the different interrupt requests generated by the iSBC 88/45 processor board or by the utility board.

CIRCUITS	DESCRIPTION
10. iSBX expansion connector:	The I/O capability of the iSBC 88/45 processor board can be enhanced by adding a multimodule expansion board. The FDIO system uses this feature by attaching the front panel interface board to the iSBC 88/45 processor board at connector J5. The front panel interface board communicates with the iSBC 88/45 processor board over the iSBX bus which makes internal address, data, and control lines available.
11. Multibus interface:	This circuitry allows the iSBC 88/45 to access other boards connected to the multibus interface. Data, address and control lines are brought out of the iSBC 88/45 board to the Multibus backplane where they are bussed and made available to other boards plugged into the Multibus interface. Specifically, the resources on the utility board are made available to the iSBC 88/45 in the CCU or PCU, and the resources on the 16 K RCU memory expansion board are made available to the iSBC 88/45 in the RCU.

2.1.2.6.3 Utility Board. The utility board in the CCU or PCU is a Multibus compatible board that plugs into the Multibus backplane at location J4. The utility board operates slave to the iSBC 88/45 processor board in that it cannot control the Multibus interface, but can only respond to memory and I/O requests made of it. The utility board is configured for the FDIO system. The major circuits of the utility board are described below:

CIRCUITS	DESCRIPTION
1. Expansion RAM:	48 Kb of expansion RAM allow for the buffering of FDIO messages for CCU and PCU systems. This memory is contiguous with the 16 Kb of RAM on the iSBC 88/45 and starts at memory location 4000 (hex).
2. GPI interface circuitry:	The GPI interface provides the 8-bit GPI data, accepts control information, and performs the handshaking to communicate and send the byte to the Host PAMRI. The GPI circuit includes a firmware controlled loop-back feature to allow the parity checker and data output port to be verified.
3. GPO interface circuitry:	The GPO interface accepts the 8-bit GPO data, provides status information, and performs the handshaking to communicate with and receive data from the Host PAMRI. The GPO circuit includes a firmware controlled loop-back feature which allows the receive buffers, parity checker, and data input port to be verified.
4. FSE circuitry:	This circuit resides on each utility board and monitors the redundant operation of the CCU or PCU. The FSE circuitry monitors the operation of the iSBC88/45 processor board, a self-test which is done periodically to assure its own correct operation, and the operation of the redundant control unit.

CIRCUITS	DESCRIPTION
	The FSE circuitry detects any abnormality and initiates the appropriate recovery action, for example, switching off a malfunctioning primary control unit, or removing a failed secondary control unit from operation.
5. ICL circuitry:	The ICL circuitry consists of two high speed asynchronous serial channels connecting the primary and secondary control units. The primary and secondary control units communicate with each other over the ICL cable by sending messages and data over the ICL interface. ICL channel A is used to send commands and data to the redundant control unit. The receiving control unit uses channel B to respond to commands and data received from the originating control unit. The ICL circuit contains a firmware controlled loop-back feature which allows for testing of the two serial channels without needing the ICL cable or redundant control unit.

2.1.2.6.4 16 K RCU Memory Expansion Board. The 16 K RCU memory expansion board (used in RCUs only) is a Multibus compatible board that plugs into the Multibus backplane at connector J4. The 16 K memory expansion board is configured for the FDIO system to increase the amount of buffer memory available in the RCU.

2.1.2.6.5 LAN Interface Adapter Board. The LAN interface adapter board connects to J1 of the iSBC 88/45 processor board and provides a transition for the LAN interface signals on the iSBC 88/45 processor board and the LAN cable connecting to the LAN assembly. The board is shown in figure 11-20, sheet 2, and more detailed information is in paragraph 2.2.2.5.

2.1.3 Front Panel Assembly

The front panel assembly consists of the following five units as shown in figures 11-1, 11-2, 11-3, and 11-4 (3):

1. Front panel interface board
2. Front panel interface cable
3. Front panel control board
4. Display interface cable
5. LCD display module

NOTE

This assembly is common to the CCU, PCU, and RCU.

The front panel assembly allows operators to communicate with the FDIO equipment via the front panel. A 40-column LCD display panel and an audible alarm are the output media to the operator, and a 20-key keypad is the operator input mechanism to the FDIO system.

The front panel assembly is attached to the front of the Multibus assembly and is hinged to allow access to the boards within the Multibus assembly. The front panel interface cable connects the front panel assembly to the Multibus cardcage assembly.

2.1.3.1 Power Distribution. The power required to operate this assembly is supplied by the iSBC 88/45 board via the front panel interface cable.

2.1.3.2 Inputs. Operator inputs consist of keypad entries. There are two types of keypad entries: function and edit/response keys.

2.1.3.2.1 Function Keys. The FDIO function keys invoke FDIO system firmware and are listed below:

RECN	Pressing this key allows the operator to view and modify the current site configuration data of the control unit.
DIAG	Pressing this key allows the operator to initiate diagnostics.
SYS/STAT	Pressing this key allows the operator access to the system status and error logger.
PRI/SEC	Pressing this key allows the operator to initiate a control unit switch operation. This key is valid for a CCU or PCU control units only.
ACK	Pressing this key allows the operator to acknowledge and clear the message displayed on the front panel.

2.1.3.2.2 Edit/Response Keys. The remaining keys (digits, YES/GO, NO, EXIT, CLEAR, and ENTER) are used during the operator dialogue with the FDIO system, such as entering responses to menus displayed on the front panel or parameters required by different functions.

2.1.3.3 Outputs. The front panel assembly contains an audible alarm for signaling error conditions, and a 40-column LCD display module for displaying text.

2.1.3.4 Theory of Operation

2.1.3.4.1 Front Panel Interface Board. The front panel interface board is an iSBX compatible board that connects to the iSBC 88/45 processor board. The connection is made via the iSBX connector J5 on the iSBC 88/45 board. The iSBX connector supports the iSBX bus structure which is a general purpose I/O bus containing data, address, and control signals. The front panel interface board is configured for the FDIO system and contains the following major sections:

a. Electrically EPROM (EEPROM) — This circuitry consists of a 2048 byte nonvolatile EEPROM chip, and supporting address and control logic. The EEPROM stores site configuration data and system error information. Refer to 2.2.3.1.5 for more detailed information on the EEPROM.

b. Front panel control — This circuitry is the control interface between the iSBC 88/45 processor board and the front panel assembly. Two main operations are performed:

   1. Front panel display circuit — This circuit provides the bidirectional data port and control lines used to drive the 40-column LCD display on the front panel, and control the front panel audible alarm.

   2. Keyboard scan circuit — This circuit scans the front panel keypad (20 keys arranged in a 5 by 4 array). The keys are debounced, buffered internally, and made available to the firmware running on the iSBC 88/45 processor board.

2.1.3.4.2 Front Panel Interface Cable. The front panel interface cable connects J1 of the front panel interface board of the Multibus assembly and J101 of the front panel control board of the front

panel assembly and consists of a 50-pin ribbon cable using IDC technology. The cable contains the power and signal lines that drive the LCD, and the audible alarm. The cable also contains keyboard contact closure information.

2.1.3.4.3 Front Panel Control Board. The front panel control board receives the LCD, audible alarm data, and control signals through the front panel interface cable. LCD signals are routed to the LCD module via the display cable plugged into J102 of the control board. The audible alarm is activated directly from the control lines received at pins W3 and W4 of the front panel control board.

The 20-key keypad contains the key contacts arranged as a 4x8 matrix, but only five of the eight rows contain active keys. The remainder are available for future expansion. The column and row scan lines are routed to J101 for sensing by the front panel interface board.

2.1.3.4.4 Display Cable. This cable connects J102 of the front panel control board and the LCD module, and consists of a 14-pin ribbon cable using IDC technology. It contains the power and signal lines that drive the LCD and the display contrast control line.

2.1.3.4.5 LCD Module. The display module, mechanically mounted to the front panel, consists of a plastic front LCD panel capable of displaying 40 characters and is surrounded by a protective metal support. Each character is represented in a 5x7 dot matrix array. All interface and drive electronics are part of the module. Data and control lines enter the module via a 14-pin connector on the back of the module used for connecting the display cable.

2.1.4 LAN Assembly

The LAN assembly routes output messages from the FDIO control unit to the peripheral devices and accepts input messages from the peripheral devices. Peripheral devices attached to a CCU are modems which communicate with RCUs. Peripheral devices attached to a PCU are RFSPs, and peripheral devices attached to an RCU are RFSPs, CRTs, and RANKs. The configuration of the LAN assembly differs for each control unit type.

The LAN exists as a loop having a primary station located at the control unit and up to 29 BCs, and it uses the ADCCP protocol. The primary station is located on the iSBC 88/45 processor board and communicates with the BCs plugged into the BC backplane via the RS-422 LAN cable. The message transmission (ADCCP frame) from the control unit reaches the BC backplane where the signal levels are converted from RS-422 differential to single ended TTL logic levels. The transmission is then routed sequentially to each BC plugged into the backplane. Up to 16 BCs may be installed into a single BC backplane. Prior to exiting the BC backplane, the signal levels are converted back to RS-422 differential signals for transmission.

If the system requires more than 16 BCs, an additional BC backplane may be installed. The LAN extension cable links the output of the first BC backplane with the input of the second BC backplane. The output of the second (or last) BC backplane links to the control unit to complete the LAN loop.

Each BC receives the frame and examines the address field of that frame. If the frame address matches the BC address, the BC accepts and buffers the frame. Frames not addressed to the BC are passed to the next BC in the BC backplane. If the message requires an immediate response, the addressed BC waits until the entire frame has passed and appends the appropriate response frame. This response frame is also passed through all succeeding BCs. Both the original message frame and any response frames are received at the control unit primary station.

After receiving and buffering a message, the BC interprets it and, if appropriate, transmits it to the attached peripheral. For a CCU, the message is transmitted to a modem via the modem interconnect

cable using RS-232 discipline. For an RCU or PCU, the message is transmitted to the peripheral device via the peripheral interconnect cable using RS-422 discipline.

2.1.4.1 CCU LAN Assembly. The CCU LAN assembly is redundant and communicates with redundant Multibus assemblies. The CCU LAN assembly distributes messages between the CCU and up to 28 modems connected to RCUs and contains the following five replaceable units as shown in figure 11-1 (4):

1. LAN cable (two)
2. LAN extension cable (two)
3. BC backplane (two)
4. BC (up to 28)
5. Modem interconnect cable (up to 28)

2.1.4.2 PCU LAN Assembly. The PCU LAN assembly is redundant and communicates with redundant Multibus assemblies. The PCU LAN assembly distributes messages between the PCU and up to 28 RFSPs and a maintenance channel, and it contains the following five replaceable units as shown in figure 11-2 (4):

1. LAN cable (two)
2. LAN extension cable (two)
3. BC backplane (two)
4. BC (up to 29)
5. Peripheral interconnect cable (up to 29)

2.1.4.3 RCU LAN Assembly. The RCU LAN assembly communicates with a nonredundant Multibus assembly and is therefore nonredundant. The RCU LAN assembly normally distributes messages between the RCU and up to 14 peripherals. Fourteen is the maximum number of peripherals available in a standard RCU due the contractual requirement to have one spare slot and one slot for the maintenance channel BC card. The RCU LAN assembly can be expanded by adding another BC cardcage assembly to distribute messages between the expanded RCU and up to 20 peripherals. The RCU LAN assembly contains the following five replaceable units as shown in figures 11-3 and 11-4 (4):

1. LAN cable
2. LAN extension cable (expanded RCU only)
3. BC backplane (RCU-1; Expanded RCU-2)
4. BCs (maximum configuration: RCU 15; Expanded RCU-21)
5. Peripheral interconnect cables (RCU 14; Expanded RCU-20)

NOTE

An additional peripheral interconnect cable may be added to the maintenance port according to site requirement.

2.1.4.4 Power Distribution. The power to operate the LAN assembly is supplied to the BC backplane by redundant power supplies. The PCU, RCU, and RCU expanded BC backplane assemblies require only +5 V dc (see figures 11-2, 11-3, and 11-4), while the CCU BC backplane also requires ±12 V dc (see figure 11-1), which is due to the RS-232 drivers and receivers on the BC. The redundant power supplies are connected in parallel with steering diode circuitry to automatically switch to the other supply should one fail.

2.1.4.5 Inputs. Inputs to the LAN assembly may come from one of two sources:

1. Multibus assembly: Messages to be transmitted to the BCs originate at the iSBC 88/45 processor board.
2. Peripherals: Messages or responses received from the peripherals are conveyed to the BCs via the modem and peripheral interconnect cables and transmitted to the control unit.

2.1.4.6 Outputs. Outputs from the LAN assembly may be sent to one of two destinations:

1. Peripherals: Messages destined to the peripherals are transmitted from the BC via the modem or peripheral interconnect cables.
2. Multibus assembly: The primary LAN station at the iSBC 88/45 conveys messages or responses between the BCs and the control unit for processing.

2.1.4.7 Theory of Operation

2.1.4.7.1 LAN Cable. The LAN cable connects the Multibus assembly LAN interface board with the BC backplane. The cable has three ends: P1 connects to J1 of the LAN interface board and contains transmitted and received information, P2 connects to P17 or P18 of the BC backplane and contains transmit signals, P3 connects to P19 or P20 of the BC backplane and contains receive signals described in table 2-9.

TABLE 2-9. LAN INTERFACE CABLE SIGNAL DEFINITIONS

Signal Name	P1	P2	P3
+ RXD	1		1
GND	2	6	
- RXD	3		2
+ TXD	4	7	
+ RXC	5		3
- TXD	6	8	
- RXC	7		4
+ TXC	8	9	
GND	9		5
- TXC	10	10	

The LAN cable provides the physical element (a loop) required by the LAN bus. The output message originating at the LAN interface board is transmitted through the cable to P2, where it enters the BC backplane at P17 or P18. While in the backplane, the message travels to successive BCs and leaves

the BC backplane via P19 or P20. When no additional BC backplanes are connected in the series, the message is picked up at P3 of the LAN cable and routed to the control unit via the LAN cable. During this final leg of the loop transmission, the messages and any responses are considered inputs to the control unit.

If the LAN assembly is part of a redundant CCU or PCU, two LAN cables are required. One cable originates at the LAN interface board of the primary control unit, and the second from the LAN interface board of the secondary control unit. Only the primary control unit will transmit over the LAN cable. However, problems requiring the secondary control unit to assume control cause the secondary LAN cable to become active.

2.1.4.7.2 LAN Extension Cable. The LAN extension cable is used to provide increased peripheral capacity by connecting an additional BC backplane serially. The LAN extension cable connects the BC backplane output to the input of the next BC backplane. In a redundant CCU or PCU system, two LAN extension cables are required: one for the primary, and one for the secondary LAN.

2.1.4.7.3 BC Backplane. The BC backplane is the electrical interface for up to 16 BCs. The BC backplane is designed for redundant operation. The BC backplane communicates with primary and secondary LAN busses via the LAN cables. (RCU LAN BC backplanes contain, but do not use redundancy feature.) The LAN signals from the redundant LAN cables are received via connectors P17 and P18, converted from RS-422 to TTL logic levels and routed to successive BC slots. The BC decides which LAN is in use by detecting which LAN clock is active. Each LAN bus clock is active when it is controlling data flow on the LAN and the other LAN is disabled. Two red LEDs indicate which of the two clocks is active.

Since all 16 positions of the BC backplane may not contain a BC, the BC backplane contains electronics to automatically bypass an empty connector or a powered OFF BC position. If the BC backplane fails due to power loss, mechanical relays bypass the BC backplane, allowing the LAN information to be passed on to any operational BC backplanes. The failure of a BC or a BC backplane does not cause the LAN to fail.

Before exiting the BC backplane, the LAN bus signals are converted from TTL logic levels to RS-422 and then returned to the iSBC 88/45 via the LAN cable or to the expansion BC backplane via the LAN extension cable if additional BC backplanes are required.

The BC backplane is powered by redundant power supplies. Red LED indicators monitor supply lines of the redundant power supplies and provide a visual indication of the active voltage.

2.1.4.7.4 BC. The BC is a PCB that plugs into the BC backplane. The BC buffers and communicates messages between the LAN bus and the attached peripheral device.

The BC is an autonomous processor containing a microprocessor chip, supporting memory, and I/O interfaces. The major functional sections of the BC are as follows:

1.	CPU:	An 8031 microprocessor chip forms the foundation of the CPU, and contains 128 bytes of internal memory. This memory is segmented as general purpose registers, stack, scratch pad RAM, and specialty I/O registers.
2.	8 Kb of program memory (EPROM):	The program memory contains the instructions that are executed by the CPU in order to perform the FDIO operations.
3.	8 Kb of data memory (RAM):	This RAM buffers messages between the LAN and a peripheral device.

4.	Asynchronous communications controller:	This function is built into the 8031 processor and provides communication between the BC and a RANK, CRT, or RFSP. An internal baud rate generator provides the clock necessary to operate at 2400 baud.
5.	Synchronous communications controller:	This dual channel device provides the communications interface with the LAN bus (channel A) controller and the modem (channel B). The LAN channel operates at 19.2 K baud and receives its clock from the LAN bus (generated on iSBC 88/45 board). The modem channel operates at 2400 baud and receives its clock, which originates at the RCU, from the modem.
6.	Active LAN detect logic:	This logic determines which LAN bus is active by detecting the operational clock of the active LAN bus.
7.	RS-422 drivers and receivers:	Used by the asynchronous communications interface for communicating with a RANK, CRT, or RFSP.
8.	RS-232 drivers:	Used by the synchronous communications and receivers interface (channel B) for communicating with the modem.

A maximum of 16 BCs may be installed into BC backplane connectors J1 through J16. The BC backplane connects the redundant LAN bus signals and the power supply signals to P1 on the BC.

Internal circuitry monitors both LAN busses to determine which bus contains an active clock, thereby identifying the primary LAN bus. The active LAN bus signals are directed to channel A of the synchronous communications controller where the LAN frame is received one bit at a time. The BC examines the incoming frame to determine whether the frame address matches the BC address defined by the 7-position Dual Inline Package (DIP) switch. When the address matches, the frame is accepted, buffered, and processed; otherwise the frame is ignored. The BC repeats the incoming frame via the LAN bus to make it available to subsequent BCs.

The BC firmware interprets the received frame and decides whether interaction with its peripheral device is required. If the BC is connected to a modem (i.e., BCs on the CCU LAN), the entire frame is transmitted to the modem via channel B of the synchronous communications controller using the RS-232 discipline. If the BC is connected to a RANK, RFSP, or CRT, the text is stripped from the frame and transmitted to the peripheral over the asynchronous RS-422 interface.

Messages received by the BC from a peripheral device are buffered and made available for transmission to the iSBC 88/45 over the active LAN bus.

2.1.4.7.5 Modem Interconnect Cable. The modem interconnect cable plugs into P1 through P16 of the BC backplane connected to a CCU LAN. The other end of the cable connects to a government furnished modem. The cable utilizes the RS-232 signal convention and contains four active signals and a ground. See table 2-10 for a description of the signals.

TABLE 2-10. MODEM INTERCONNECT CABLE SIGNAL DEFINITION

Interface Signal Names	Input [I] Output [O]	Function
		SERIAL DATA LINES
MRX	[O]	RS-232 serial transmit data line (to modem) (RCU to BC)
MTX	[I]	RS-232 serial receive data line (from modem) (BC to RCU)
		CLOCK LINES
MTC	[I]	RS-232 transmit clock line (RCU to BC)
MRC	[O]	RS-232 receive clock line (BC to RCU)
		GROUND LINES
GND		RS-232 ground reference

2.1.4.7.6 Peripheral Interconnect Cable. The peripheral interconnect cable plugs into P1 through P16 of the BC backplane connected to a PCU or RCU LAN. The other end connects to a RANK, CRT, or RFSP. The cable uses the RS-422 signal convention and contains four active signals and a ground. See table 2-11 for description of the signals.

TABLE 2-11. PERIPHERAL INTERCONNECT CABLE SIGNAL DEFINITION

Interface Signal Names	Input [I] Output [O]	Function
		SERIAL DATA LINES
PRXP	[O]	RS-422 serial transmit data line (to peripheral)
PRXN	[O]	RS-422 serial transmit data line (to peripheral)
PTXP	[I]	RS-422 serial receive data line (from peripheral)
PTXN	[I]	RS-422 serial receive data line (from peripheral)
		GROUND LINES
GND		RS-422 ground reference

2.1.5 Peripheral Devices

Four peripheral devices are used by the FDIO system; the RANK, CRT, RFSP, and modem (see figures 11-1 through 11-4). The modem is furnished by the government and provides the electrical interface between a CCU, the telephone line, and an RCU at a remote site.

The RANK, CRT, and RFSP peripheral devices communicate with the BCs via the peripheral interconnect cable using asynchronous RS-422 protocol. The cable may reach four thousand feet in length. The information received from the BC by the peripheral device is checked for correct parity and buffered. When a valid message is received, it is printed or displayed by the peripheral device.

The BCs and peripheral devices use a handshake protocol during the message exchange that results in a positive acknowledgment from the peripheral device when the message is successfully printed or displayed. If an error occurs and the message is not successfully displayed, the error is reported to the BC and relayed back to the control unit where appropriate error recovery operations are handled.

Each peripheral device contains a status byte where its current operating environment is stored. The status byte is transmitted to the BC on request. This byte is a register that specifies the identity of the peripheral device, that is, RANK, CRT or RFSP, and indicates status, for example; peripheral on or offline, out of paper (RFSP), or a fault condition.

2.1.5.1 Power Distribution. Each peripheral device receives power from a 120 V ac 60 Hertz (Hz) external source. Internal power supplies provide the required voltages for correct operation.

2.1.5.2 Inputs. Input messages from the BC are received by a peripheral device over the peripheral interconnect cable. The RANK inputs are from its keyboard.

2.1.5.3 Outputs. The primary output media for an RFSP is a printed flight strip, and a display screen for a CRT. The RANK has a Message Waiting Light (MWL) indicator that can be turned ON and OFF by the RCU via messages received by the RANK's BC. In addition, all peripheral devices send characters to the BC as part of the communications protocol; the RANK also sends key entries to the BC via the peripheral interconnect cable.

2.1.5.4 Theory of Operation

2.1.5.4.1 RFSP. The RFSP provides a hard copy flight strip printout of FDIO messages. The RFSP is connected to the peripheral interface on a BC board of a PCU or an RCU.

a. Refer to the FDIO peripheral commercial manuals listed below for the description of the operation of the RFSP (FA 10095/2):

   FDIO Printer (RFSP) Operators Manual (April 1986)
   FDIO Printer (RFSP) Technical Manual (February 1986)
   FDIO Printer (RFSP) Illustrated Parts Manual (February 1986)
   FDIO Printer (RFSP) P-Card Reference Manual (March 1986)

b. For RFSP (FA 10095/11):

   Model 9034/9044 Operating Guide Edition B (October 1988)

c. For RFSP (FA 10095/14):

   IER 512 Printer User Guide Ref. N07102A Rev. Level 2, 12/13/96

2.1.5.4.2 CRT. The CRT provides remote site operators with a visual display of flight strip, general information, and weather messages. The CRT also provides a visual display for editing messages (entered on the assigned RANK) to send to the Host.

Each CRT is a stand alone, desktop unit connected to the peripheral interface on a BC board of an RCU. The CRT displays 25 lines and 80 columns of alphanumeric characters. The CRT also has an audible alarm for signaling error conditions.

The CRT is manufactured by FALCO Data Products, to meet FDIO system requirements.

a. Refer to the FDIO peripheral commercial manuals listed below for the description of the operation of the CRT (FA 10095/4):

FDIO CRT Operator and Technical Manual (September 1985)

Part One — Operator/Programmer Information
Part Two — Technical Information

b. For CRT (FA 10095/12):

Falco Infinity-S Programmer's Manual Revision A (1990)
Falco Quick Setup Guide (1990)

2.1.5.4.3 RANK (FA10095/3). The RANK allows an operator to compose, edit, and enter messages to the Host. The RANK consists of 72 illuminated keys and an MWL. RANK entries are displayed and edited on either a CRT or RFSP as specified by the RCU configuration. One to five RANKs may be connected to an RCU. Each RANK is connected to the peripheral interface of one BC board.

The RANK contains the keyboard assembly, keyboard control microcomputer, microcomputer support hardware, and a 5 V power supply. The RANK interface is full duplex and uses asynchronous RS-422 protocol at 2400 baud. When a key is pressed, the RANK outputs the corresponding 8-bit ASCII code (eight data bits, odd parity bit and one stop bit) to the BC board. The RANK also receives command bytes which initiate a diagnostic test, and causes the MWL to blink.

2.1.5.4.4 RANK (FA10095/17). The RANK allows an operator to compose, edit, and enter messages to the Host. The RANK consists of 86 illuminated keys. RANK entries are displayed and edited on either a CRT or RFSP as specified by the RCU configuration. One to five RANKs may be connected to an RCU. Each RANK is connected to the peripheral interface of one BC board.

The RANK contains the keyboard assembly, keyboard control microcomputer, microcomputer support hardware, and an external 5 V power supply. The RANK interface is full duplex and uses asynchronous RS-422 protocol at 2400 baud. When a key is pressed, the RANK outputs the corresponding 8-bit ASCII code (eight data bits, odd parity and one stop bit) to the BC board.

2.1.5.4.5 Modem (Modulator-Demodulator). The FDIO system uses Codex 3600 modems. The modems and their technical manuals are furnished by the customer. Each modem contains six independent channels which are multiplexed and demultiplexed on a 4-wire, point-to-point, conditioned telephone company (TELCO) line. The FDIO modem channel operates at 2400 baud and supports synchronous communication. The interface between the modem and the control unit is via RS-232. Each modem provides the electrical interface between a CCU, the telephone line, and an RCU which links the Host to a remote site.

The FDIO system uses only one of the six available channels. The remaining five channels are used for other data communications between an ARTCC and a common remote site. Each modem channel associated with a CCU is connected to the modem interface of one BC board. Each modem channel of an RCU is connected to the modem interface of the iSBC 88/45 processor board in the Multibus cardcage assembly.

Refer to the Codex 3600 modem technical manual for the description of the operation of the modem.

2.2 DETAILED THEORY OF OPERATION

2.2.1 Host Interface

2.2.1.1 GPI/GPO Interface Board. The GPI/GPO interface board circuitry is shown in figure 2-1.

This board has the GPI and GPO cable interface connector components installed, and there are two PCB edge connectors. There are no active or passive components. The board acts only as a cable-to-cable interface.

There are four cable connectors on this board, J1 (GPI), J2 (GPO), J3 (MULTIBUS GPI/GPO), and J4 NAS Simulator (NASSIM). Connectors J1 and J2 connect only to the GPI and GPO cables furnished by the contractor. Connectors J3 and J4 connect to a forty-pin Insulation Displacement Socket (IDS) flat ribbon cable connector.

CAUTION

Never connect the NASSIM and the Host to the GPI/GPO cable interface at the same time. Disconnect the Host or the NASSIM from the GPI/GPO cable interface before connecting the other to the cable. Damage to either the Host or the NASSIM may result if this procedure is not followed.

2.2.1.2 Terminator Board. The terminator board is connected to P1 of the flat ribbon GPI/GPO interface cable from the GPI/GPO cable interface board to the Multibus assembly. The terminator board provides the proper signal terminations for the NAS PAMRI. The terminator board contains the resistor networks for the termination of the signal lines to ground required by the PAMRI. The terminator board circuitry is shown in figure 2-2.

2.2.2 Multibus Cardcage Assembly

2.2.2.1 Multibus Backplane. The Multibus backplane is a standard, off-the-shelf, PCB assembly used to connect the various PCBs in an FDIO control unit. It consists of four PCB edge connectors, two power supply connectors, and a Multibus priority arbitrator. The Multibus backplane is shown in figure 2-3.

2.2.2.1.1 PCB Edge Connectors. On the Multibus backplane there are four, 86-pin, PCB edge connectors connected in parallel as prescribed in the Intel Multibus Handbook.

There are two Multibus PCBs in each Multibus backplane assembly. In the CCU and PCU, the PCBs are the iSBC 88/45 processor board, and the utility board. In the RCU, the PCBs are the iSBC 88/45 processor board, and the 16 K RCU memory expansion board.

Each of the Multibus backplane signal lines is terminated by a pullup resistor to +5 V.

2.2.2.1.2 Power Supply Connectors. The Multibus interface specification allows for the connection of ±5 V, ±12 V, -10 V, and ground to each of the PCBs via a power distribution network on the Multibus backplane. The FDIO control units only use +5 V, and ±12 V.

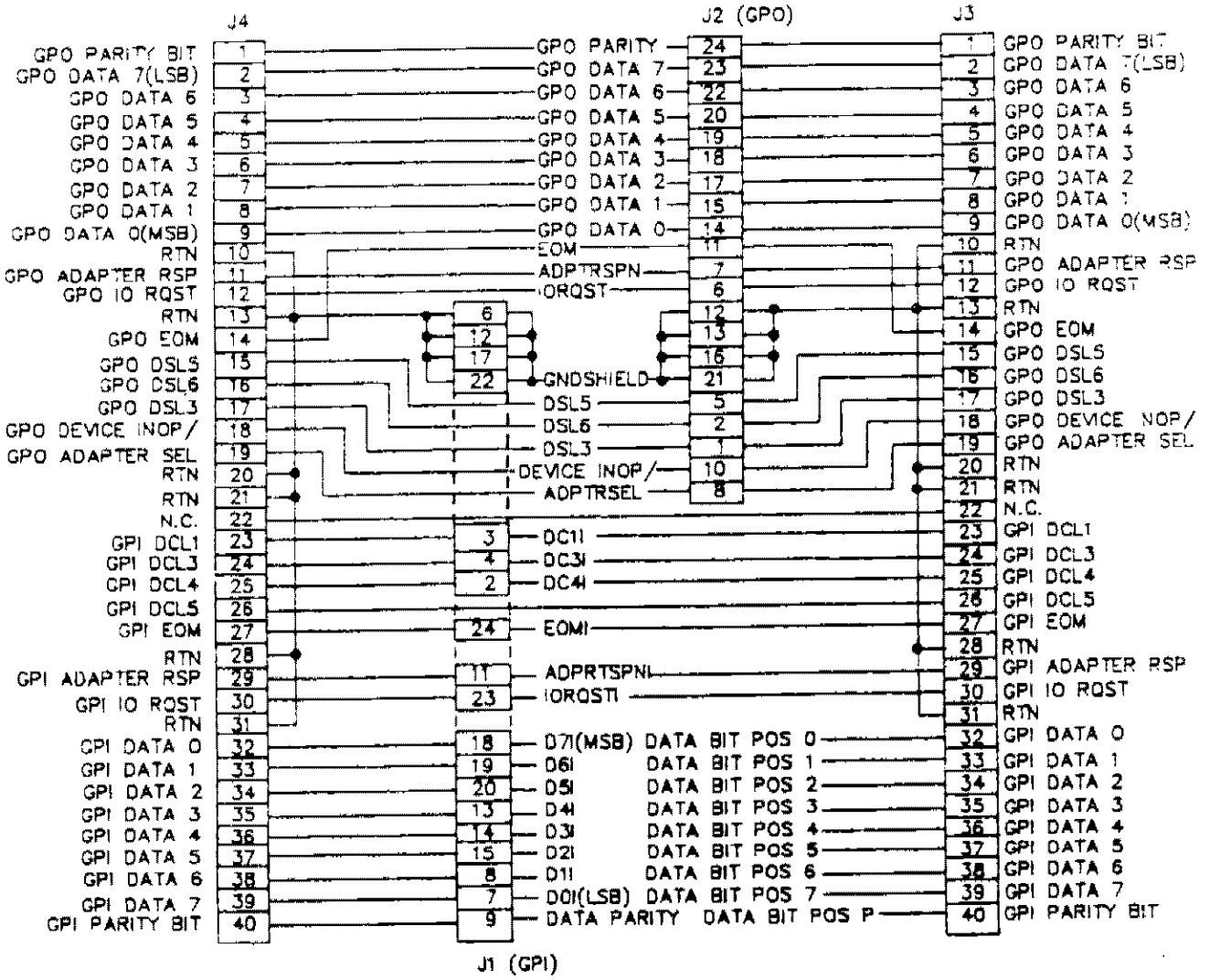


FIGURE 2-1. GPI/GPO INTERFACE BOARD

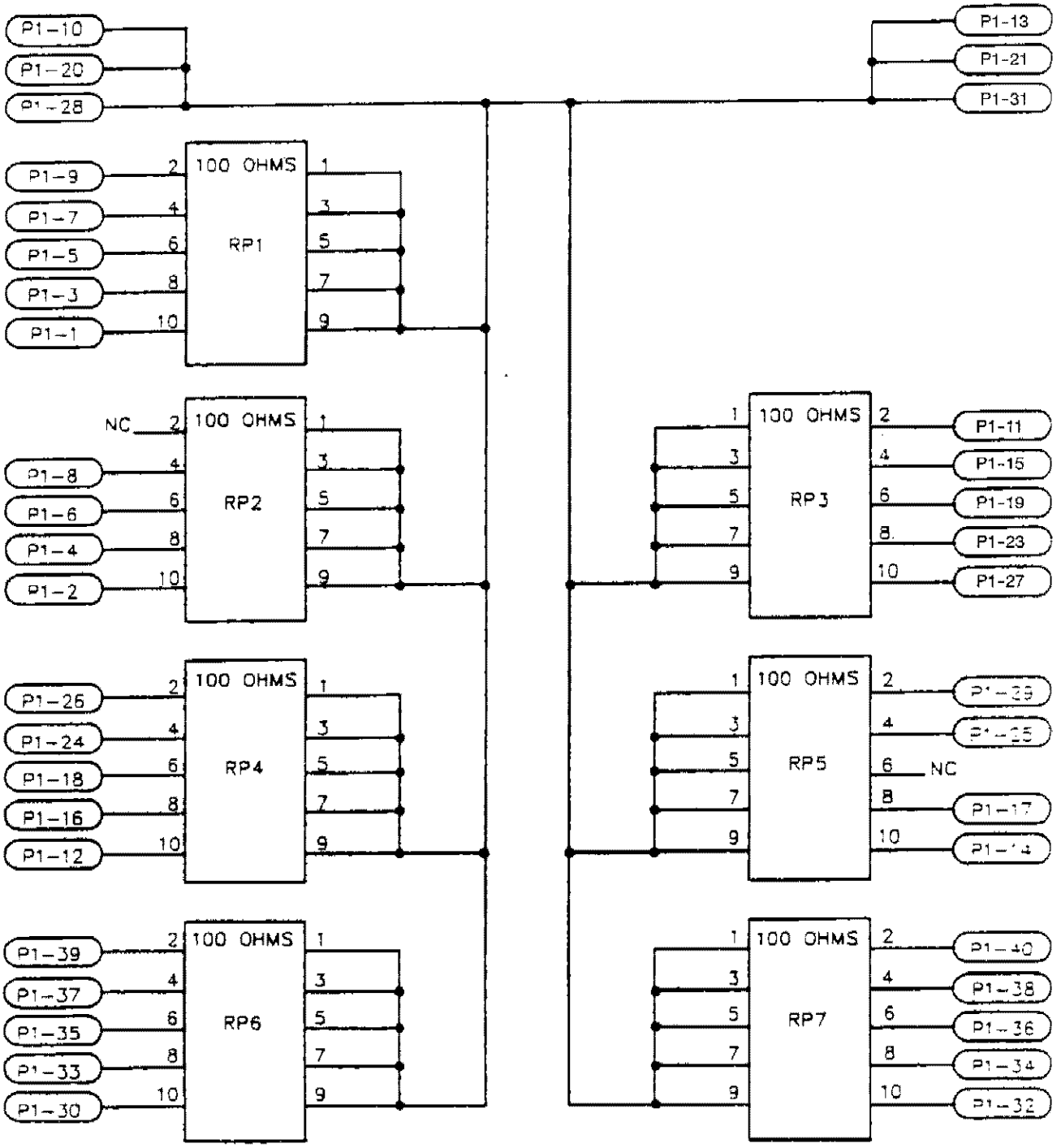


FIGURE 2-2. TERMINATOR BOARD

J1 J4

SIGNAL NAME		CONNECTOR PIN NO	TERMINATION
DATA	0/	73	RP1-2.2K-2
	1/	74	RP2-2.2K-2
	2/	71	RP1-2.2K-3
	3/	72	RP2-2.2K-3
	4/	69	RP1-2.2K-4
	5/	70	RP2-2.2K-4
	6/	67	RP1-2.2K-5
	7/	68	RP2-2.2K-5
	8/	65	RP1-2.2K-6
	9/	66	RP2-2.2K-6
	A/	63	RP2-2.2K-7
	B/	64	RP1-2.2K-7
	C/	61	RP2-2.2K-8
	D/	62	RP1-2.2K-8
	E/	59	RP2-2.2K-9
DATA	F/	60	RP1-2.2K-9
INT	0/	41	RP5-1K-3
	1/	42	RP5-1K-2
	2/	39	RP5-1K-5
	3/	40	RP5-1K-4
	4/	37	RP5-1K-7
	5/	38	RP5-1K-6
	6/	35	RP5-1K-9
INT	7/	36	RP5-1K-8
ADDR	0/	57	RP3-2.2K-2
	1/	58	RP4-2.2K-2
	2/	55	RP3-2.2K-3
	3/	56	RP4-2.2K-3
	4/	53	RP4-2.2K-4
	5/	54	RP3-2.2K-4
	6/	51	RP4-2.2K-5
	7/	52	RP3-2.2K-5
	8/	49	RP4-2.2K-6
	9/	50	RP3-2.2K-6
	A/	47	RP4-2.2K-7
	B/	48	RP3-2.2K-7
	C/	45	RP4-2.2K-8
	D/	46	RP3-2.2K-8
	E/	43	RP4-2.2K-9
	F/	44	RP3-2.2K-9
	10/	28	RP6-2.2K-8
	11/	30	RP6-2.2K-5
	12/	32	RP6-2.2K-4
ADDR	13/	34	RP6-2.2K-3

J1 J4

SIGNAL NAME	CONNECTOR PIN NO	TERMINATION
INIT/	14	RP8-1K-8
BUSY/	17	RP8-1K-6
MRDC/	19	RP8-1K-5
MWTC/	20	RP8-1K-4
IORC/	21	RP8-1K-3
IOWC/	22	RP7-1K-9
INH1/	24	RP7-1K-7
INH2	26	RP7-1K-5
BCLK/	13	RP9-220/330-4
CCLK/	31	RP9-220/330-2
XACK/	23	RP8-1K-2
		RP7-1K-8
LOCK/	25	RP7-1K-6
BHEN/	27	RP6-2.2K-9
INTA/	33	RP7-1K-2
CBRQ/	29	RP7-1K-4

J1
15

COMMIT.	DEVICE	PIN NO.
+5	P1	3,4,5,6
		81,82,83,84
	J14-J16	4,5
	J17-J19	2,3
	RP1-RP8	1,10
	RP9	6
+12	P1	7,8
	J17-J19	4
-5	P1	9,10
	J17-J19	5
-10	P1	77,78
	J14-J16	2
-12	P1	79,80
	J14-J16	3
GND	P1	1,2,11,12,75, 76,85,86
	J14-J19	1,6
	RP9	1

FIGURE 2-3. MULTIBUS BACKPLANE

2.2.2.1.3 Multibus Priority Arbitrator. FDIO control units make use of the serial bus priority method which allows for the connection of one main processor, and three subprocessors. This priority arrangement is achieved by grounding bus priority request input (BPRN/) pin 15 on the iSBC 88/45 processor board connector J1 with the configuration jumper, and daisy chaining the bus priority request output (BPRO/) pin 16 on the iSBC 88/45 processor board to the next highest subprocessor bus priority request input (BPRN/) pin 15 on the Multibus backplane jack.

In the FDIO control unit, only the iSBC 88/45 processor board is allowed to control the Multibus. All other PCBs are addressed and controlled via the Multibus and do not require daisy chaining.

The Multibus parallel priority arbitrator circuitry contains the only active components on the Multibus backplane and consists of four integrated circuits (A1 through A4), 10 K Ohm resistor terminator packs, and a configuration jumper. With the exception of the configuration jumper which is used to designate the bus main processor, the remainder of the Multibus parallel priority arbitrator is not used by the FDIO system.

2.2.2.2 iSBC 88/45 Board. The following paragraphs contain a functional description of each of the major components of the iSBC 88/45 board as shown in the block diagram in figure 2-4. Each component is designated by a circled number. For a more detailed description of the iSBC 88/45 board, refer to Intel vendor manual number 143824-003.

2.2.2.2.1 Clock Circuits. The clock signals for the iSBC 88/45 board are generated by one of three sources: the 9.8304 Megahertz (MHz) oscillator, the clock generator device, or the Programmable Interval Timer (PIT) devices.

2.2.2.2.1.1 Crystal Oscillator. (Figure 2-4 (1)): The 9.8304 MHz crystal oscillator generates BCLK/ and CCLK/ for Multibus interface synchronization and generates MCLK/ for the iSBX BC interface synchronization. It is also an input for the PIT devices.

2.2.2.2.1.2 Clock Generator Device. (Figure 2-4 (1)): The clock generator device provides a selectable 8 MHz clock to the CPU, the Multibus interface devices, and the PIT devices. It provides a 4 MHz PCLK signal to the serial interface devices. The clock generator device and the dual-port arbitration logic are driven by a 24 MHz crystal that produces a 24 MHz Oscillator (OSC) output and a selectable 8 MHz CLK output. The CLK/ signal controls the clock inputs to each of PIT device.

2.2.2.2.1.3 PIT Devices. (Figure 2-4 (11)): The PIT devices are partially dedicated to generating the transmit (TxC) and receive (RxC) clocks required by the I/O devices. The OUT2 output from each PIT provides the 5 MHz real time clock for the FDIO System.

2.2.2.2.2 Ready Synchronization Circuitry. (Figure 2-4 (2)): The READY SYNC device provides synchronization for the READY signal generated for the CPU. The READY SYNC device can synchronize generation of the READY signal with the requirements of I/O and memory devices, including EPROM, RAM, iSBX Bus interface device, and I/O devices.

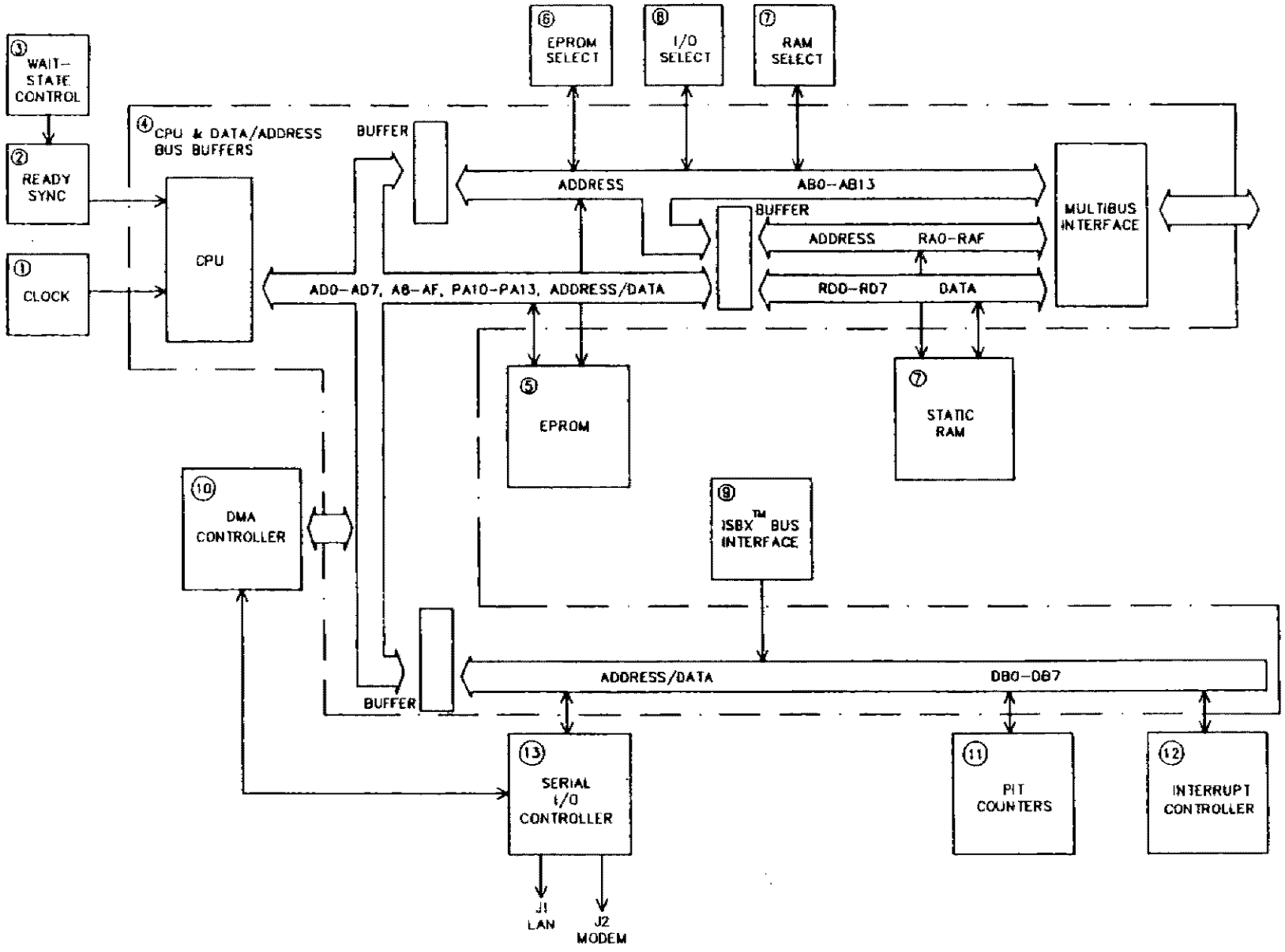


FIGURE 2-4. ISBC 88/45 BOARD BLOCK DIAGRAM

2.2.2.2.3 Wait-State Generator. (Figure 2-4 (3)): The wait state generator synchronizes the operation of various speed resources to the operation of the CPU by controlling generation of the READY signal to the CPU. The READY circuitry decides what type of memory is being accessed and matches the CPU speed to that of the memory device via a synchronous wait-state generator. RAM accesses require zero wait-states, I/O accesses require two wait-states, and EPROM accesses are configurable for zero or one wait state depending on the EPROM speed.

2.2.2.2.4 CPU and Data/Address Bus Buffers. (Figure 2-4 (4)): The interface between the CPU and the remainder of the iSBC 88/45 board consists of a series of buffer devices that provide information to the major functional areas of the board via the local address and data buses. The on-board data lines are buffered through one of several different data buffers, depending on the destination of the data. The CPU directly controls four buses in transferring addresses and data to and from the iSBC 88/45 board. The buses are labeled as follows:

a. The AD0-AD7 and A8-AF signals from the CPU provide a local 16-bit address bus output (AB0-ABF) for generating the chip select terms, the ROM/EPROM addresses, and the addresses required by LSI devices.

b. The AD0-AD7 signals from the CPU provide an 8-bit dual-port data bus output (RD0-RD7). A dual-port RAM data bus provides a data transfer path between the Multibus data transceiver and the dual-port RAM data buffers. The CPU uses the dual-port RAM data bus for the following three purposes:

   1. Local accesses to on-board RAM,

   2. MULTIBUS interface resource accesses to on-board RAM, and

   3. Local CPU accesses of Multibus interface resources.

c. The AD0-AD7 signals from CPU provide a local 8-bit data bus output (DB0-DB7). The local data bus provides an 8-bit interface for the I/O peripherals and the iSBX buses.

d. The PA10-PA13 CPU signals provide a local 4-bit address and status bus output (AB10/ through AB13/).

2.2.2.2.5 On-board EPROM. (Figure 2-4 (5)): The EPROM devices are provided by FSG and installed into EPROM device sockets U49, U50, U89, and U90. The U49 socket contains an EPROM device to hold the bootstrap routines required by the iSBC 88/45 board. The remaining device sockets are filled with the remainder of the control unit program. Jumpers are included on the iSBC 88/45 board to enable user installation of different types of EPROM devices; the FDIO system uses 27128 devices. The on-board EPROM resides at the highest locations of the highest page (1 Megabyte (Mb)) of memory that may be directly addressed by the iSBC 88/45 board. The EPROM device in socket U49 contains the highest addresses. Refer to table 2-12 for the jumper changes required to modify an iSBC 88/45 board to production configuration, table 2-13 for necessary changes to integrated circuits, and to table 2-14 for a complete jumper listing of a deliverable production configuration. See figure 11-5 for the iSBC 88/45 board jumper locations.

TABLE 2-12. PRODUCTION CONFIGURATION JUMPER CHANGES

REMOVE JUMPERS		ADD JUMPERS			
From	To	From	To		Description
E5	E6	E4	E5		Ground Clear to Send (CTS) on 8273 device
E10	E11	E11	E12		Connects the receive clock input of the 8273 to J1
		E17	E18		Connects Signal Ground (SGND) on J1 to board ground
		E30	E31		Connects Signal (SG) on JF1 to board ground
		E15	E16		Allows 8273 to disable transmit data and clock
		E46	E47		Enables bus time out if no ACK within 10 MSec
E76	E87				Interrupts
E82	E93				Interrupts
E83	E94				Interrupts
E84	E95				Interrupts
		E76	E92	(*)	EOP/ to flipflop 37
		E79	E102	(*)	Ground unused inputs to
		E101	E102	(*)	IR7
		E80	E100	(*)	TIMER 12 to IR6
		E81	E184	(*)	INT5/ to IR5
		E82	E185	(*)	INT6/ to IR2
		E83	E97	(*)	INT1 to IR1
		E84	E93	(*)	8273 RxINT to IRO
		E95	E98	(*)	latched EOP to IR7
		E128	E129		connect BCLK/
E121	E122				enables expansion memory
E150	E151	E149	E150	(*)	configure EPROM size for
		E150	E151	(*)	27128 devices
E152	E153				configure EPROM size for
		E143	E147		27128 devices
		E177	E180	(*)	INTI/ to inverter U44

(*)indicates that connection is a wire jumper, not a shorting block

TABLE 2-13. CHANGES TO INTEGRATED CIRCUITS

The removed chips enable RS-232 operation of modem channel J2 of the iSBC 88/45. The chips to be installed are packaged in conductive foam within the iSBC 88/45 shipping box.

REMOVE ICs		ADD ICs		
From	To	From	To	DESCRIPTION
U12				RS-422 receiver
U13				RS-422 driver
			U14	RS-232 receiver (1489A)
			U11	RS-232 driver (1488)

TABLE 2-14. DELIVERABLE PRODUCTION CONFIGURATION JUMPER LISTING

Configuration: 1. 64 Kb EPROM using 27128 EPROMs
2. No iSBC 341 expansion board

From	To	Description
E1	E2	Connects clock output OUT1 from PIT device U1 to the 32x clock input (32SCLK) pin of the 8273 device
E4	E5	Grounds CTS on the 8273
E7	E8	Connects clock output OUTO from PIT device U1 to transmit clock input TxC for the 8273 device
E11	E12	Connects the 8273 device receive clock input to the I/O channel clock (LAN)
E13	E14	Connects the OUTO signal from PIT device U27 to the transmit clock (TxCA) signal for channel A of the 8274.
E15	E16	Allows 8273 to disable transmit data and clock
E17	E18	Connects the SGND signal on connector J1 to board ground.
E19	E22	Connects the Receive Common (RC) signal on connector J1 to board ground
E21	E24	Connects the Send Common (SC) signal on connector J1 to board ground
E26	E27	Connects 8274 channel A receive clock input to I/O channel (modem)

TABLE 2-14. DELIVERABLE PRODUCTION CONFIGURATION JUMPER LISTING (Continued)

Configuration: 1. 64 Kb EPROM using 27128 EPROMs
2. No iSBC 341 expansion board

From	To		Description
E28	E29		Connects the Carrier Detect (CDA) input from connector J2 to the CDA input on the 8274 channel A
E30	E31		Connects the SGND signal on the J2 connector to board ground
E32	E33		Connects the RC signal on connector J2 to the board ground
E36	E37		Connects the SC signal on connector J2 to board ground
E38	E39		Connects Direct Memory A (DMA) acknowledge output signal DACK2/ from channel 2 of the 8237A-5 device to the 8273 device DMA acknowledge signal input during transmission
E41	E42		Connects 8274 Multiple Protocol Serial Controller (MPSC) device channel B receive clock (RxCB) signal to the TxCA signal on the RS-232C interface at connector J3
E46	E47		Enables bus time out if no ACK within 10 msec
E48	E49		Connects the Carrier Detect B Channel (CDB/) signal from connector J2 to the CDB input for channel B of the 8274 device
E72	E73		Connects the Data Mode (DM) signal and Data Set Ready (DSR) signal on connector J1 to a general purpose input port at Port A, bit 2 (PA2) of the 8273 device
E74	E75		Grounds the Carrier Detect (CD) input on the 8273 device
E76	E92	(*)	Connects the EOP output of the 8237 DMA controller to the clock input of edge interrupt sensing flipflop U37
E79	E102	(*)	Connects unused input for IR7 to ground
E101	E102	(*)	Connects unused input for IR7 to ground
E80	E100	(*)	Connects TIMER 12 interrupt to IR6
E81	E184	(*)	Connects external INT5/ to IR5
E82	E185	(*)	Connects external INT6/ to IR2
E83	E97	(*)	Connects inverted INT1 to IR1
E84	E93	(*)	Connects 8273 RxINT (LAN) to IR0

TABLE 2-14. DELIVERABLE PRODUCTION CONFIGURATION JUMPER LISTING (Continued)

Configuration: 1. 64 Kb EPROM using 27128 EPROMs
2. No iSBC 341 expansion board

From	To		Description
E85	E96		Grounds NMI
E95	E98	(*)	Connects latched EOP to IR7
E107	E108		Connects the 8237 DMA controller Receive DMA data request signal input (DREQ3) to the receive DMA data request signal output from the 8273 device
E110	E111		Connects the Transmit DMA data request
E112	E113		signal output from the 8273 device to DMA data request input signal DREQ2 for channel 2 of the 8237 device
E114	E115		Used for testing purposes only
E117	E118		Connects the DMA acknowledge signal output (DACK3/) from the 8237 device to the 8273 device Receive DMA acknowledge signal input
E123	E124		Connects the OUT1 output from PIT device U27 to transmit clock TxCB input for channel B of the 8274 MPSC
E125	E126		Enables decoding of the Mb page address bits of the address
E128	E129		Connects signal BCLK/ to the Multibus interface and arbiter
E130	E131		Selects 8 MHz clock operation
E132	E133		Testing purposes only
E135	E136		Testing purposes only
E137	E138		Selects one wait-state for EPROM access cycles
E140	E144		Connects +5 V to pin 1 of EPROM sockets U89, U50, and U90
E141	E145		Connects address bit ABC to pin 2 of each EPROM socket
E142	E146		Connects address bit ABB to pin 23 of each EPROM socket
E143	E147		Connects address bit ABD to pin 26 of each EPROM socket
E149	E150	(*)	Select EPROM capacity for 27128
E150	E151	(*)	Select EPROM capacity for 27128

TABLE 2-14. DELIVERABLE PRODUCTION CONFIGURATION JUMPER LISTING (Continued)

Configuration: 1. 64 Kb EPROM using 27128 EPROMs
2. No iSBC 341 expansion board

From	To		Description
E154	E155		Configures the bus arbiter
E156	E157		Connects bus arbiter output BPRO/ to the Multibus
E159	E165		Selects on-board RAM base at 40000 Hex
E171	E172		Configures the bus arbiter
E173	E174		Connects the 8088 LOCK/ signal to the Multibus
E177	E180	(*)	Connects external INT1/ to inverter U44
E189	E190		Testing purposes only
E191	E192		Connects all 8245 device clock inputs to CLK/
E195	E196		Connects pin 5 of PROM decoder device 53 to ground

(*)indicates that the connection is a wire jumper and not a shorting block

2.2.2.2.6 EPROM Select Logic. (Figure 2-4 (6)): The iSBC 88/45 board performs on-board memory resource selection by decoding the memory address presented to the Programmable Array Logic (PAL) devices, PROM SELECT, and I/O Select. An on-board EPROM address is indicated when PAL device PROM SELECT compares address lines ABB through AB13 with memory address space and activates one of the EPROM chip select signals when the memory address does reside in on-board EPROM space. The decision is indicated by activation of the PROM SELECT signal and activation of the ONBDADDR/ signal. The two signals enable PROM SELECT to activate one of eight EPROM chip select signals to enable the appropriate section of on-board EPROM.

2.2.2.2.7 On-board RAM Select and Static RAM. (Figure 2-4 (7)): The iSBC 88/45 board enables the on-board static RAM by decoding the memory address presented to the PAL device. The PAL device provides a local memory address decode for the 16 K static RAM array by generating a signal that selects the local RAM when address lines ABE through AB13 are all zero and the MEM/IO signal is HIGH. These conditions activate the on-board RAM request and the on-board RAM enable signal. The on-board RAM RQ signal enables the RAM array, controls the bus arbitration logic, and controls the direction of data transfer on the internal data buses.

2.2.2.2.8 I/O Device Select Enable Logic. (Figure 2-4 (8)): The iSBC 88/45 board performs on-board I/O device selection by decoding the I/O address. An on-board I/O address is indicated when I/O Select compares address lines AB7 through AB13 with I/O address space and activates output signal ON BD I/O. The ON BD I/O signal enables logic to further decode address lines AB4, AB5, and AB6, which control the generation of the I/O device enable signals.

2.2.2.2.9 iSBX Bus Interface. (Figure 2-4 (9)): The iSBC 88/45 board contains an iSBX BC (J5) to enable the iSBC 88/45 board to accept one single-wide, two single-wide, one double-wide and one single-wide, or one double-wide iSBX Multimodule board. The iSBC 88/45 board is capable of performing DMA operations over the iSBX bus interface if the Multimodule board can generate the required DMA control signal responses. The DMA control signals are jumpered to include a Multimodule board DMA Request signal (MDRQT) and a Multimodule board DMA acknowledge signal (MDACK/).

The clock (MCLK) provided on the iSBX BC is derived from the on-board 9.8304 MHz crystal, and it provides a clock of approximately 102 nanosecond (ns) duration.

2.2.2.2.10 DMA Controller. (Figure 2-4 (10)): The DMA Controller provides control for a maximum of two channels of serial I/O on the iSBC 88/45 board. The DMA operation control on the iSBC 88/45 board is provided by an Intel DMA Controller device. The device must be programmed via the CPU to control the serial data I/O transfer operations.

2.2.2.2.11 PIT Counters. (Figure 2-4 (11)): The two PIT devices each contain one time (OUT2) that is user configurable for generation of timing signals for on-board or off-board use. These timers may be used for a variety of on-board and off-board functions, including timed-interval DMA request, timed interval DMA termination, or fail-safe timer control to deal with improper peripheral device responses that could suspend system operation.

2.2.2.2.12 Interrupt Controller. (Figure 2-4 (12)): The interrupt controller controls sensing and reporting of external interrupt requests to the CPU. The interrupt controller can accept, mask, and/or arbitrate between the different interrupt requests that are generated on-board or from a Multibus interrupt line.

Interrupt requests to the interrupt controller can originate from on-board I/O, expansion I/O, the flag byte, or the Multibus resources. The interrupt controller is sensitive to level-type interrupt signals; however, the iSBC 88/45 board contains a flip-flop that also provides edge-sensitive interrupt detection.

2.2.2.2.13 Serial I/O Controllers. (Figure 2-4 (13)): The serial I/O interfaces on the iSBC 88/45 board are implemented via an High-Level Data Link Control (HDLC)/SDLC Protocol Controller device and an MPSC device. The serial protocol controllers provide two channels of serial output via two serial interface connectors. There are two serial interface connectors on the iSBC 88/45 board that each provide a serial communications channel interface, as follows:

1. Connector J1 for serial to the LAN and
2. Connector J2 for serial to MODEM.

Serial connectors J1 and J2 provide identical interfaces supporting both the RS-232C and the RS-422A/449 interface standards. Serial interfaces J1 and J2 have a serial interface consisting of four sockets which accept RS-232C and RS-422A/449 drivers and receivers provided with the iSBC 88/45 board.

The on-board data lines are buffered through one of several data buffers, depending on the destination of the data.

2.2.2.3 Utility Board. A utility board resides in each of the Multibus cardcage assemblies of the CCU and PCU cabinet assemblies. The RCU Multibus cardcage assembly does not contain a utility board. The utility board is a logical extension of the iSBC 88/45 processor board, in that, resources

on the utility board can be accessed by the iSBC 88/45. The communication medium between the iSBC 88/45 and the utility board is the Multibus, an electrical interface which allows for the sharing of address, data, and control lines between the two boards.

The utility board is designed specifically for the FDIO application, and contains circuitry to implement several special functions. Figure 11-6 is a functional block diagram of the utility board illustrating the following seven major functional circuits:

1. Multibus interface
2. Expansion RAM
3. GPO interface
4. GPI interface
5. FSE
6. ICL
7. Power distribution

Figure 11-7 (Sheets 1 through 9) is a detailed schematic diagram of the utility board hardware with the major functional sections marked. The following paragraphs describe each functional section. A slash (/) as part of the signal name indicates the signal is active when it is at a logical low level.

2.2.2.3.1 Multibus Interface. (Figure 11-7, Sheet 2): The Multibus interface logic on the utility board allows the onboard resources, such as expansion memory and special I/O functions, to be accessed and controlled by the iSBC 88/45 board. These resources are Memory Mapped I/O (MMIO), in that all devices are accessed from the iSBC 88/45 as memory locations. Data and control information is sent to I/O devices by performing a memory write operation to the appropriate memory address. Likewise, data and status information from the I/O devices is obtained by performing memory read operations. This allows a consistent and reliable device select logic circuit and simplifies the application firmware that must access these devices.

The Multibus interface includes data, address and control line buffers, and the board acknowledge circuitry.

2.2.2.3.1.1 Multibus Buffers. (Figure 11-7, Sheet 2 (1)) The address interface circuit consists of two 74LS240 8-bit inverting buffers (U60 and U61), and a 74LS20 4-input NAND gate (U58). The two buffers invert the 16 lower address lines (ADR0/ to ADRF/) from negative active logic to positive active logic, and also provide the driving capability for the address lines on the utility board. The 74LS20 receives the four high-order address lines (ADR10/ to ADR13/), and drives signal BANK0/. The memory can be thought of as being organized as 16 banks, with each bank containing 64 Kb of memory. The high-order address lines (ADR10/ to ADR13/) select one of the 16 banks, while the low-order lines (ADR0/ to ADRF/) address a specific location within the bank. All resources on the utility board, including expansion RAM and MMIO devices, are located within bank 0.

When the iSBC 88/45 accesses a memory location within the lowest 64 Kb bank (address range 00000 through 0FFFF hex), the signals ADR10/ through ADR13/ are inactive (high), causing signal BANK0/ to be driven active (low). The Boolean equation for BANK0/ is:

$$\text{BANK0/} = \overline{\text{ADR10/ AND ADR11/ AND ADR12/ AND ADR13}}$$

The data interface circuit consists of one 8287 (U62) 8-bit bidirectional inverting transceiver. This transceiver provides the control of the eight data lines (DAT0/ to DAT7/) between the Multibus and the utility board. The output enable signal (pin 9) is controlled by signal BANK0/. Whenever the iSBC 88/45 processor performs a memory operation within bank 0, signal BANK0/ becomes active, thereby enabling the data transceiver.

When the transceiver is enabled via BANK0/, the direction control signal (pin 11) is controlled by the MRD/ signal. When this input is high, the 8287 is configured to enable the eight Multibus data lines present at P1 onto the internal utility board data bus lines (DAT0 to DAT7). When pin 11 is low, the 8287 causes the data on the internal data bus lines to be enabled onto the Multibus data lines (DAT0/ to DAT7/).

2.2.2.3.1.2 Board Acknowledge Circuit. (Figure 11-7, Sheet 2 (2)): Whenever the iSBC 88/45 accesses the utility board, it expects an acknowledgment when the operation has been completed. If the utility board fails to do so, the iSBC 88/45 will remain in a wait loop until its onboard false acknowledgment timer expires, at which time it will continue with its operation.

The acknowledgment circuit consists of one 2-input OR gate (U52), one 2-input NAND gate (U38), and a buffer (U64). The acknowledgment signal, XACK/, is active whenever a memory read or memory write operation is performed on the utility board. The Boolean equation is as follows:

$$\text{XACK/} = \overline{(\text{MRD OR MWT}) \text{ AND } \overline{\text{BANK0}}}$$

Each time the iSBC 88/45 accesses the lowest memory bank, signal BANK0/ will become active, and either a memory read or memory write operation will activate signals MRD/ or MWT/. This will cause XACK/ to become active, informing the iSBC 88/45 processor that the utility board has completed the operation, and the iSBC 88/45 can proceed.

2.2.2.3.2 Expansion RAM. (Figure 11-7, Sheets 2 and 3): This circuitry consists of the RAM and MMIO device select logic and the 46 Kb expansion RAM array.

2.2.2.3.2.1 Device Select Circuit. (Figure 11-7, Sheet 2 (3)): This logic circuit is responsible for decoding the Multibus address, and selecting the appropriate RAM chip or MMIO device. The circuit consists of two 3-to-8 decoders (74LS138) (U46) and (U63). The RAM decoder U46 produces the RAM chip selects for each RAM chip on the utility board, while the MMIO decoder U63 produces the chip selects for the control devices on the utility board; for example GPI, GPO, FSE/FS interface, and ICL.

Memory operations to any location within the first bank (bank 0), (addresses 00000 through 0FFFF hex) will cause one of the 16 outputs of the decoders to become active. The RAM decoder (U46) is enabled by BANK0/, and selects its active output based upon the state of the three address input lines, ADRD through ADRF. Its active select outputs are RAMCS2/ through RAMCS7/, with each select line corresponding to a unique 8 Kb section of RAM. Note that the lower two select lines (U46-15 and 14) are not used, since the 16 Kb address range they correspond to exists on the iSBC 88/45 board. The upper select line (pin 7) is further qualified by signal SELMMIO, such that RAMCS7/ is not active if SELMMIO is active. SELMMIO disables RAMCS7/ if the address specified falls within the uppermost 2 Kbs of the bank 0 RAM (address range 0F800 through 0FFFF hex), which corresponds to the MMIO locations. See table 2-15 for a description of each of the RAM select lines.

TABLE 2-15. RAM SELECT SIGNALS

Active Chip Select	Memory Locations	Select RAM Device
RAMCS2/	04000H-05FFFH	U53
RAMCS3/	06000H-07FFFH	U41
RAMCS4/	08000H-09FFFH	U34
RAMCS5/	0A000H-0BFFFH	U26
RAMCS6/	0C000H-0DFFFH	U17
RAMCS7/	0E000H-0F7FFH	U3

The MMIO device select decoder (U63) is enabled by two signals: (1) the output of the RAM select decoder (U46-7), which indicates that the address range is between 0E000 through 0FFFF hex, and (2) signal SELMMIO, which further restricts the address range to the last 2 Kbs (addresses 0F800 through 0FFFF hex). Its select outputs are based upon the state of the three address input lines (ADR8 through ADRA). Each output corresponds to a 256 byte range of memory addresses within the upper 2 Kbs of bank 0. Although each select output corresponds to a wide range of addresses, each selected MMIO function typically decodes only the lower one or two address bits, thereby limiting the useful address range. See table 2-16 for a description of each of the MMIO select lines.

TABLE 2-16. MMIO SELECT SIGNALS

Select Line	Address Range	Function Selected
GPICS/	0F800-0F803 (hex)	Select GPI controller
GPOCS/	0F900-0F903	Select GPO controller
ICLCS/	0FA00-0FA03	Select ICL SCC
—	0FB00-0FBFF	Not used
FS1CS/	0FC00-0FCFF	Fail safe command/status
RDFSESTAT/	0FD00-0FDFF	Fail safe interface lines
—	0FE00-0FEFF	Not used
—	0FF00-0FFFF	Not used

2.2.2.3.2.2 46 Kb Expansion RAM Array. (Figure 11-7, Sheet 3 (4)): The RAM select decoder, U46 (74LS138), provides chip selects to the 8 Kb RAM chips on the utility board. There are six of these chips, providing for a total of 48 Kbs of expansion RAM. The last 2 Kbs of memory, from location 0F800H to 0FFFFH, is not used, and is defined as the MMIO area used to select the various MMIO

devices on the utility board. In this way, the system is able to access any device on the utility board through a regular memory access instruction instead of an I/O instruction.

2.2.2.3.3 GPO Interface Logic. (Figure 11-7, Sheets 6 and 7): The GPO circuit on the utility board employs special interface hardware that allows the FDIO system to communicate with the GPO adapter of the Host over the GPO interface. The GPO circuit consists of the following six logical sections:

1. GPO signal interface circuit
2. GPO controller
3. GPO parity checker
4. GPO handshake logic
5. GPO abort detection circuit
6. GPO byte delay circuit

2.2.2.3.3.1 GPO Signal Interface Circuit. (Figure 11-7, Sheets 6 and 7 (5)): This section consists of several 75124 receiver chips (U6, U21, U22, and U30), and 75123 driver chips (U7, U13, and U44). The following FDIO input signals are received and buffered from connector J3 to produce TTL level signals used internally to the utility board:

J3	Input Signal	Internal Signal
9	GPO DATA0 (MSB)	GPOD7
8	GPO DATA1	GPOD6
7	GPO DATA2	GPOD5
6	GPO DATA3	GPOD4
5	GPO DATA4	GPOD3
4	GPO DATA5	GPOD2
3	GPO DATA6	GPOD1
2	GPO DATA7 (LSB)	GPOD0
1	GPO PARITY	GPOPAR
19	GPO ADAPTER SELECT	ASEL
11	GPO ADAPTER RESPONSE	GPOARSP
14	GPO EOM	GPOEM

The following FDIO TTL output signals are buffered and transmitted to the GPO adapter via connector J3:

Internal Signal	Output Signal	J3
GPOIORQ	GPOIOREQ	12
(Note)	DEVICE INOP	18
GPODSL3	DSL3	17

Internal Signal	Output Signal	J3
GPODSL5	DSL5	15
GPODSL6	DSL6	16

NOTE

The output signal, DEVICE INOP, is active when signals GPOOUTENB and DINOP are both at a logical high level.

2.2.2.3.3.1.1 GPO Loopback Circuit. The GPO loopback circuit is used to provide the FDIO GPO with a self test capability on the GPO circuit. Whenever a message resend occurs, the FDIO GPO firmware can investigate the operation of the GPO hardware of the FDIO unit, allowing the FDIO unit to determine if a message resend is required due to an internal failure of the FDIO GPO hardware. For instance, if a resend occurs and is due to a parity error being detected, the GPO firmware will perform a GPO loopback test in order to determine if GPO internal hardware is operational. When GPO firmware performs a GPO loopback test, it will first activate the GPO TEST signal (U36-12), which sets the receiver (75124) to select the test data input and stop the input from the GPO interface lines. The variations of the GPO TA (U37-11) and GPO TB (U37-10) signals enable the receiver to produce four different data patterns on the data line and the GPO PAR (U21-9) signal. The four test patterns are: 00H, 55H, AAH, and FFH. Also, the combinations of the data patterns, and the GPO PAR signal allows the GPO parity checker to generate different parity according to its 9 input lines. Therefore, the GPO loopback test enables the GPO firmware to check out the GPO receiver interface circuit, GPO controller interface circuit and the GPO parity checker circuit.

2.2.2.3.3.2 GPO Controller. (Figure 11-7, Sheet 6 (6)): The GPO circuit utilizes an 8255A Programmable Peripheral Interface (PPI) and supporting logic to perform the 8-bit parallel input and control operations. The PPI is organized as three, 8-bit bidirectional I/O ports, and is directly accessible from the iSBC 88/45 processor, via the Multibus. The GPO PPI is a memory mapped I/O device, in that, data and status information is accessed by the iSBC 88/45 performing a memory read operation, and data and command information is sent by the iSBC 88/45 performing memory write operation.

The GPO PPI is assigned the memory address range 0F900 through 0F903 (hex), and is enabled by signal GPOCS/ (see paragraph 2.2.2.3.2.1). The specific address assignments are as follows:

Memory Address	Function
0F900	PORT A — output: control and status lines.
0F901	PORT B — input: GPO data byte.
0F902	PORT C — input/output: control and test lines.
0F903	CONTROL REGISTER — output.

The functional configuration of the PPI is programmed by the system firmware residing on the iSBC 88/45. Each of the three ports may be configured to be either input, output, or both.

The PPI supports the following three modes of operation:

1. Mode 0 (Basic I/O) — Each port is configured as an 8-bit input or output port, with no handshake provided. All three ports are available as I/O lines.

2. Mode 1 (Strobed I/O) — This configuration provides a means of transferring data to or from a specified port in conjunction with strobes, or handshake lines. Ports A and B provide dedicated input or output lines, while the lines of port C are used to generate, or accept the handshake signals required by ports A and B.

3. Mode 2 (Strobed Bidirectional I/O) — This mode is similar to Mode 1, except Ports A and B provide for bidirectional data transfers.

The GPO PPI is configured as follows:

Port A — This port is configured as an output operating under mode 0, and allows certain control and interface lines to be set or reset. The following control bits are available by writing an 8-bit control word to port A of the GPO PPI, memory address 0F900 (hex):

MSB							LSB
7	6	5	4	3	2	1	0

Bit	Description
0	GPO ENB/: When active (low), this signal enables the GPO transmit buffers of the primary control unit and DEVICE INOPERATIVE.
1	GPO INTACK/: When pulsed low, this signal clears the GPO IOREQ handshake signal.
2	MSGXFREN: When active (high), this signal allows the GPO IOREQ handshake signal to be set when GPO ADAPTER RESPONSE drops low while the GPO ADAPTER SELECT is active.
3	GPO DSL3: When active (high), this signal causes the DSL3 interface line to go high (indicating a receive parity error).
4	GPO DSL5: When active (high), this signal causes the DSL5 interface line to go high (indicating a receive overflow error).
5	GPO DSL6: When active (high), this signal causes the DSL6 interface line to go high (indicating a resend request).
6	This bit is used by the fail safe circuit.
7	GPO ABORTENB: When active (high), this signal enables the GPO abort detection circuit.

Port B — This port is configured as input operating under mode 0, and allows for the reading of the eight GPO data bits by performing a memory read from memory address F901 (hex):

MSB							LSB
7	6	5	4	3	2	1	0

Bit	Description
0-7	GPOD0 — POD7 8-bits of GPO data.

Port C (lower half) — The lower four bits of port C (PC0 to PC3) are configured as inputs, and allow for the reading of certain GPO status lines by performing a memory read from memory address 0F902 (hex).

MSB							LSB
X	X	X	X	3	2	1	0

Bit	Description
0	IORQIN: This status bit indicates the state of the GPO IOREQ handshake line of the redundant control unit and is used for synchronizing purposes.
1	GPO ABORT: When active (high), this signal indicates that a GPO abort condition exists.
2	BAD GPO PAR: When active (high), this signal indicates the received GPO data byte contained bad parity.
3	GPO EM: This bit indicates the state of the GPO EOM interface line.

Port C (upper half) — The upper four bits of port C (PC4 to PC7) are configured as outputs and allow for the setting of certain control bits by performing a memory write operation to memory address 0F902 (hex).

MSB							LSB
7	6	5	4	X	X	X	X

Bit	Description
4	WD: control bit used by the fail safe circuit.
5	GPO TEST: When active (high), this signal puts the GPO data buffers into loop-back mode.
6	GPO TA: Used with GPO TB to select one of four input patterns during GPO loop-back testing.
7	GPO TB

A control byte written into the control register (address 0F903 hex) determines the specific configuration as shown below:

MSB							LSB
7	6	5	4	3	2	1	0

Bit	Description
7	(=1) must be set to activate control word.
6,5	(=00) configures port A for MODE 0 operation.
4	(=0) configures port A as an output port.
3	(=0) configures port C bits 4-7 as output.
2	(=0) configures port B for MODE 0 operation.
1	(=1) configures port B as an input port.
0	(=1) configures port C bits 0-3 as input.

2.2.2.3.3.3 GPO Parity Checker. (Figure 11-7, Sheet 6 (7)): The GPO parity checker consists of a 9-bit parity generator (U31, 74LS280). If its 9 inputs has an odd number of ones (1), then it activates its odd parity output (U31-6). If its 9 inputs has an even number of ones (1), then it activates its even-parity output (U31-5).

The Host always maintains an odd parity in each byte it transfers to FDIO. If the parity result of the 8 data lines and the parity line yields an odd parity, it means that FDIO received a valid byte. If the parity result of the 8 data lines and the parity line yields an even parity, it means the FDIO received an invalid byte. Therefore, when the FDIO GPO receives the 8 data bits and a proper parity signal, the 9-input parity generator should yield an odd-parity. If this 9-input parity generator yields an even-parity (the even parity output is active), it means that the FDIO GPO received bad parity on the current byte. The active even parity output signal of this 9-input parity generator informs the GPO firmware that the parity of the currently received byte, or the received parity signal, is wrong. If a parity error occurs, the FDIO GPO firmware will activate the GPO DSL3 signal to inform the Host that a byte parity error has occurred. When FDIO informs the Host that a parity error has occurred, the Host will abort the current message transfer operation and the message will be resent to FDIO.

2.2.2.3.3.4 GPO Handshake Logic. (Figure 11-7, Sheet 7 (8)): This logic circuit provides the transmission handshake between the Host and the FDIO GPO. The handshake signals between the Host and the FDIO GPO involve the following lines: GPO Adapter Select, GPO Adapter Response, GPO I/O Request, GPO data lines (GPO DATA 0 to GPO DATA 7; where GPO DATA 0 is MSB of these 8-bit data lines), GPO Device Inoperative, and GPO status lines DSL3, DSL5, and DSL6.

Before the GPO interface can be used to communicate with the Host, it must be enabled (figure 11-7, Sheet 6 (6)). This is accomplished by performing a memory write operation to port A with bit 0 set to a logical low, causing signal GPOENB/ to become active. GPOENB/ is inverted and combined with XMTRENB via the 2-input AND gate (U45) to generate signal GPOOUTENB which enables the 75123 output drivers.

The Boolean equation for GPOOUTENB is:

GPOOUTENB = XMTRENB AND GPOENB

The following steps describe the normal GPO byte transfer sequence:

Step 1: FDIO informs the Host that the FDIO unit is ready:

FDIO will activate the Device Inoperative signal to a logical high to inform the Host that FDIO is operational. The Host PAMRI uses this signal to distinguish whether or not the FDIO unit is online. The Device Inoperative signal will maintain a logical high level whenever the FDIO unit is operational. If this line becomes inactive, the Host considers the FDIO unit not operational.

Step 2: Host informs FDIO it has a message ready for FDIO:

When the Host has a message ready to send to the FDIO GPO unit, it will activate the Adapter Select signal (U6-3), and inform the FDIO GPO circuitry that the transmission of a message will begin when the FDIO GPO is ready.

The FDIO GPO firmware prepares for the GPO message transmission by doing the following: enable the MSGXFREN signal (U36-2) which enables the GPO byte handshake hardware to generate the GPO I/O Request signal (U7-9) when the Adapter Select signal (U6-3) is active, and the GPO Adapter Response signal (U6-10) is inactive. The active MSGXFREN signal also enables the GPO interrupt hardware to generate the GPO byte interrupt signal (U45-11) when the Host has a valid byte on the GPO data lines (when the GPO I/O Request signal and the GPO Adapter Response signal are both active), and disable the GPOABORTEN signal (U36-37) to reset the GPO abort detection circuitry before the GPO transmission begins.

Step 3: FDIO GPO informs the Host that the FDIO GPO is ready to receive a byte:

MSGXFREN signal will enable the FDIO byte handshake circuit to generate the GPO I/O Request signal when the Adapter Select signal is active and the GPO Adapter Response signal is inactive. The active GPO I/O Request signal informs the NAS to put the next (or the very first) data byte on the GPO data lines. The output of 4-input AND gate (U49-6) is activated since the ASEL signal Adapter Select (U6-7) is active, the MSGXFREN signal is active, GPOARSP/ is inactive in a TTL high voltage level (because the GPO ADAPTER RESPONSE signal is inactive and the inverted output of this signal will generate a high on U57-12), and the BYTEDLY/ signal is inactive (U55-7 is at logic high because the GPO byte delay logic is inactive). The active output of the 4-input AND gate (U49-6) acts as a clock which triggers the flip-flop (U50) and activates the Q output of this flip-flop. The active Q output signal and the active ASEL signal produces an active high signal on the 2-input AND gate (U45-3). The output of this 2-input AND gate, the GPO IORQ signal, activates the GPO I/O Request signal (U7-9), output of the FDIO GPO. In addition, the GPO will activate the GPOABORTENB (U36-37) signal to enable the GPO abort detection circuit. The GPO abort detection circuit is used to detect any GPO abort sequence during a message transfer.

Step 4: Host informs FDIO GPO that a byte is ready on the GPO data interface lines:

Upon receiving an active high on the I/O Request signal (GPOIOREQ), the Host puts the next (or the first) byte on the GPO data lines and activates the GPO Adapter Response signal. The active GPO Adapter Response signal informs the FDIO GPO that a byte is available on the GPO data lines.

The GPO Adapter Response signal and GPO I/O Request generates an active BYTE INT signal on the output of the 2-input AND gate (U45-11). This active BYTE INT signal activates the GPO INT signal, and interrupts the current processor operation. This interrupt causes the GPO interrupt service routine to process the current GPO byte by reading the GPO controller port B and storing the byte into the GPO data buffer area, provided there is no parity error. If there is a parity error, the GPO interrupt firmware will set the DSL3 signal (U36-1) to inform the Host that FDIO has detected a parity error.

If no error is detected, the GPO interrupt firmware will de-activate the GPO I/O Request signal by pulsing the GPOINTACK/ signal (U36-3) to end the current message byte transfer sequence before it exits the GPO interrupt routine. If any error is found, the FDIO GPO firmware will activate the corresponding device status line(s) to reflect the error before the FDIO GPO firmware deactivates the GPO I/O Request signal.

If there is a byte parity error, the GPO firmware will raise the proper status line (DSL3) to report the error condition to the Host before it pulses the GPOINTACK/ signal which terminates the GPO I/O Request signal. If there is an overrun error, the GPO firmware will raise the DSL5 signal to indicate an overrun error condition.

Step 5: FDIO GPO informs the Host that FDIO GPO has received the current byte, and the result of the current byte transmission is ready on the device status lines:

When the GPO firmware pulses the GPOINTACK/ signal, it clears the GPO I/O Request signal on the Q output of the flip-flop (U50), clearing GPO I/O Request signal. The drop of the GPO I/O Request signal informs the Host that the FDIO GPO has received the data, and the result of current byte transmission is ready on the device status lines. The Host will examine the device status lines in order to determine if it should continue the current message transfer, or if it should restart and transfer the first byte of the same message. If any of the device status lines are activated, the Host will terminate the current message transfer sequence and may or may not initiate a resend of the message.

Step 6: Host informs the FDIO GPO of the completion of the current byte transmission:

Upon receiving the inactive GPO I/O Request signal, the Host de-activates the Adapter Response signal and ends the handshake of a message byte transmission sequence. The Host checks the result of the current byte transmission by checking the GPO device status line before it drops the GPO Adapter Response signal. If any of the GPO status lines are active, the Host will proceed with the error recovery process and initiate a GPO abort sequence.

Step 7: Continue byte transmissions until the EOM:

The FDIO GPO follows Step 3 to Step 6 of paragraph 2.2.2.3.3.4 to continue the subsequent transmission of bytes of a GPO message if no error is detected in each byte transmission.

Step 8: The Host informs FDIO GPO of the EOM transmission:

After the last byte handshake sequence is complete, the Host will raise the GPO EOM signal (U6-14) and put a dummy byte on the GPO data lines before the Host raises the GPO Adapter Response signal. The active GPO EOM signal informs the FDIO GPO firmware that the current message transmission is complete, and that the Host is waiting for the result of the current message transfer operation. Upon receiving the active GPO EOM signal, the primary unit will compare its message checksum with the message checksum of the secondary unit through the ICL channel. If the checksum generated by the two units are different, the FDIO GPO firmware will raise DSL6 and cause the Host to resend the message.

2.2.2.3.3.5 GPO Abort Detection Circuit. Refer to figure 2-5, GPO Abort Timing diagram, and (figure 11-7, Sheet 7 (9)): for the following discussion.

The GPO abort detection circuit consists of one inverter (U57, 74LS04), one flip-flop (U50, 74LS74), and one 3-input AND gate (U47, 74LS11). The GPO ABORTENB signal controls the GPO abort detection circuit, and is controlled by GPO firmware. The GPO ABORTENB signal is activated by the FDIO GPO firmware after the first byte of a message is received. This signal is de-activated by the FDIO GPO firmware after completion of a message transfer sequence, or after completion of an abort sequence. This signal remains active during a message transfer in order to detect any drop of the GPO Adapter Select signal of the Host. The GPO ABORT flip-flop (U50) is triggered by dropping the GPO Adapter Select signal while the GPO ABORTENB (U36-37) signal is active. This sets the Q output of this flip-flop (U50-9) active. The active GPO ABORT signal will cause a GPO abort interrupt on the output of the 3-input AND gate (U47-12). This interrupt activates the GPO interrupt firmware. The GPO firmware is able to tell the difference between the regular GPO byte interrupt and a GPO abort interrupt by reading the GPO abort signal on Port C data bit 1 (U36-15) of the GPO controller. If the GPO ABORT signal is active when the GPO interrupt is serviced, the GPO firmware knows the current GPO interrupt is caused by the detection of a GPO abort condition.

The Host will drop its Adapter Select signal after it senses any device status line (DSL3, DSL5 or DSL6) active. The Host reads these status lines at the end of each byte transfer as described in paragraph 2.2.2.3.3.4, step 5. When the GPO ABORTENB is inactive which maintains the flip-flop (U50) in the clear state, Q output of the flip-flop maintains at TTL low voltage level, and thus inhibits GPO detection circuit. When signal GPO ABORTENB is activated, the clear input of flip-flop U50-13 is removed, thereby allowing it to set when GPO Adapter Select goes low. The GPO abort circuit is used to inform the GPO firmware that the Host acknowledged the transmission error condition. For instance, if at the end of the message transfer sequence, the checksums generated by the two units are different, the GPO primary firmware will raise DSL6. This informs the Host to resend the same message. In response to this error condition the Host will drop the Adapter Select signal and prepare to resend the same message. The drop of the Adapter Select signal while the GPO ABORTENB signal is active will cause the GPO abort circuit to generate a GPO abort interrupt. This GPO abort interrupt informs the GPO firmware that the NAS has acknowledged the error, and that the Host is ready to resend the same message to FDIO the next time it raises the Adapter Select signal. The GPO firmware will de-activate the GPO ABORTENB signal to reset the GPO abort detection circuit, and prepare itself to receive the resend message.

The GPO checks four special error conditions:

1. parity error,
2. overrun error,
3. resend error, and
4. bad message format.

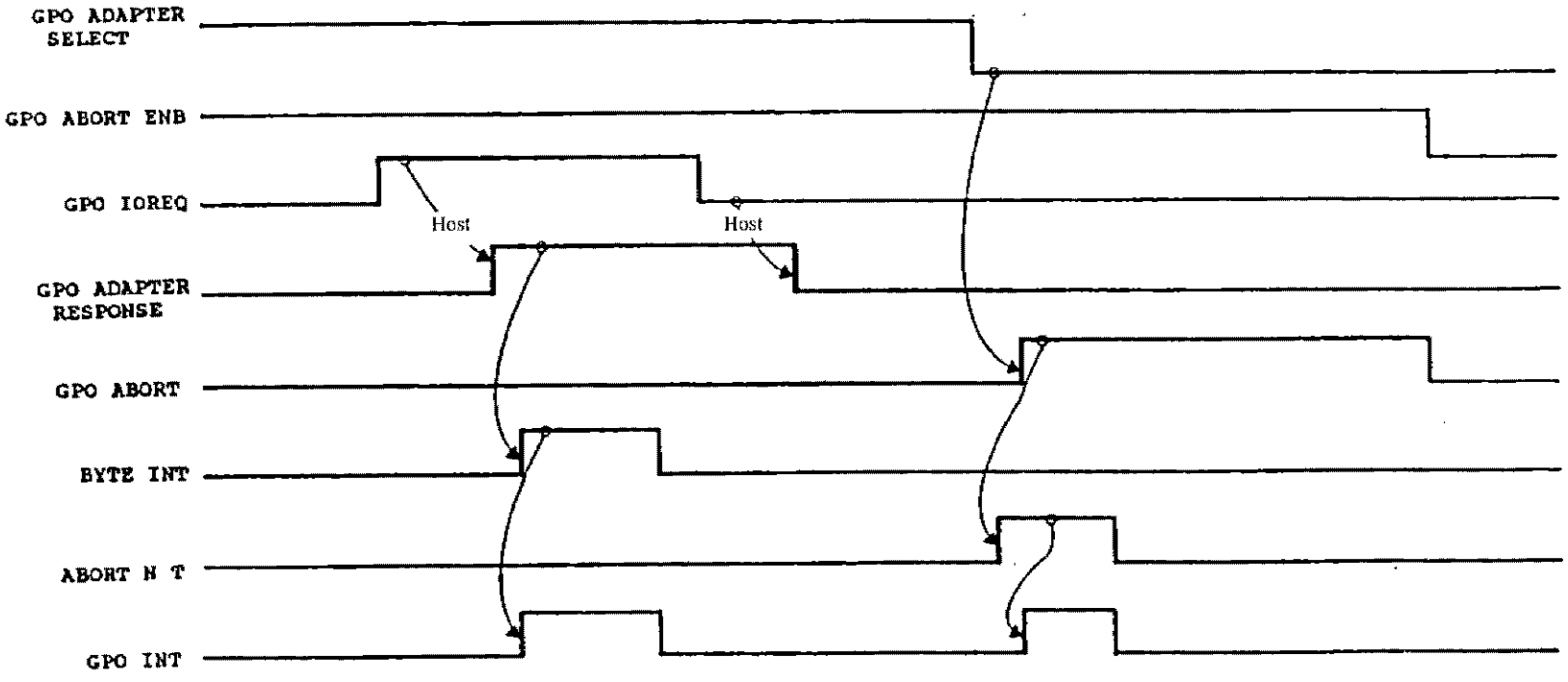


FIGURE 2-5. GPO ABORT TIMING DIAGRAM

2.2.2.3.3.5.1 GPO Parity Error Condition. A GPO parity error occurs when the parity result of the GPO parity checker, between the current byte and the current parity signal, is not an odd parity. When a parity error occurs, the GPO firmware will raise the DSL3 status line before it drops the GPO I/O REQUEST signal. The dropping of the GPO I/O REQUEST signal informs the Host that the FDIO GPO has finished the current byte transmission and the result of the byte transfer is ready on the device status lines. Then, the Host checks the device status lines, if no line is activated, it means no error was found during the current byte transmission. If the Host found no error on the device status lines, the Host will disable the GPO ADAPTER REQUEST signal which ends the current byte transfer sequence. If the Host detects the DSL3 device status line is active, in addition to dropping the GPO ADAPTER RESPONSE signal to end the regular byte transfer sequence, the Host will drop the GPO ADAPTER SELECT signal and prepare itself for a resend sequence. The dropping of the GPO ADAPTER SELECT signal by the Host will activate a GPO abort interrupt. This interrupt informs the GPO firmware that the Host has aborted the current message transmission due to a parity error. The GPO firmware then de-activates the GPO ABORTENB signal to reset the GPO abort detection circuit and prepare itself to receive the resend message.

2.2.2.3.3.5.2 GPO Overrun Error Condition. The overrun error condition occurs when the Host sends a message which has a message length over the maximum allowable byte length. When an overrun error occurs, the GPO firmware will raise the DSL5 status line before it drops the GPO I/O REQUEST signal. The dropping of the GPO I/O REQUEST signal will inform the Host to check the GPO device status lines. As described in the GPO parity error condition, the Host will then de-activate both the GPO ADAPTER SELECT signal and the GPO ADAPTER RESPONSE signal upon detecting the DSL5 status line active. The dropping of the ADAPTER SELECT signal will cause a GPO abort interrupt on the FDIO GPO unit. The GPO abort interrupt informs the GPO firmware that the Host has acknowledged the overrun error condition and will resend the message. The GPO firmware then de-activates the GPO ABORTENB signal to reset the GPO abort detection circuit, and prepare itself to receive the resend message.

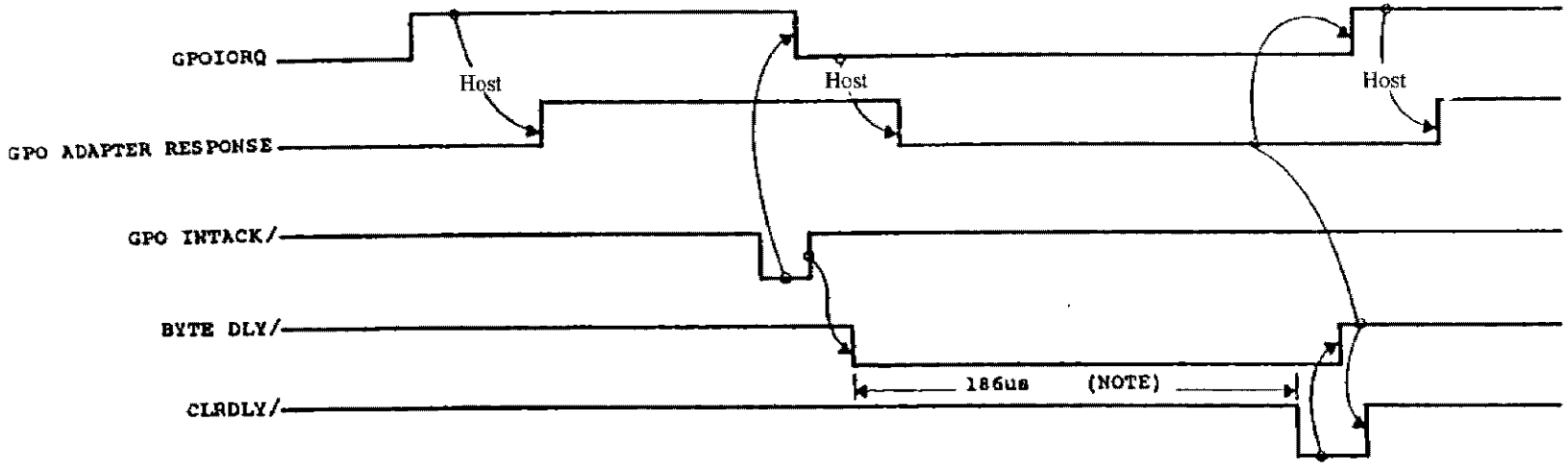
2.2.2.3.3.5.3 GPO Resend Error Condition. The GPO resend error condition occurs when the checksum between two units (the primary unit and the secondary unit) are different. When the resend condition occurs, the FDIO GPO firmware will raise the DSL6 device status line to inform the Host to resend the same message. Upon detecting that the DSL6 status line is active, the Host will drop its ADAPTER SELECT signal and the ADAPTER RESPONSE signal. The dropping of the ADAPTER SELECT while the FDIO GPO ABORTENB signal is still active, causes the generation of a GPO abort interrupt. The GPO abort interrupt informs the FDIO GPO firmware that the Host has acknowledged the resend error condition and will be ready to resend the message. The FDIO GPO firmware will de-activate the GPO ABORTENB signal and prepare itself to receive the resend message.

2.2.2.3.3.5.4 Bad Message Format. The GPO firmware checks the contents of each message it receives. Format failures such as a wrong header format, or missing End of Text (ETX) are flagged and result in the activation of the DSL6 device status line.

The Host will respond to the DSL6 being activated due to a bad message format as though the error was due to a resend condition, as described in paragraph 2.2.2.3.3.5.3.

2.2.2.3.3.6 GPO Byte Delay Circuit. The GPO byte delay circuit is set to 186 µs. This value was determined during the software/firmware integration testing phase. The additional jumper settings were incorporated into the design of the Utility PCB to permit optimizing the byte delay with any future releases of the off the shelf VRTX firmware module.

Refer to Figure 2-6, GPO Byte Delay Timing Diagram, and figure 11-7, Sheet 7 (10), for the following discussion.



NOTE: THIS FIXED DELAY IS SELECTABLE TO 186µs, 93µs, 46.5µs, or 5.8µs, BY CHANGING HARDWARE JUMPERS W7 - W10.

FIGURE 2-6. GPO BYTE DELAY TIMING DIAGRAM

Each byte received over the GPO interface causes a hardware interrupt to occur. This operation causes the program to stop executing its current application and process the GPO interrupt.

When the interrupt has been serviced, the program execution resumes where it left off. Due to the inherent speed of the Host PAMRI, GPO interrupts can occur so rapidly that they occupy a large portion of the available processing time, effectively locking out other application routines from execution.

The GPO byte delay circuit is used to create a fixed period of time following each GPO byte transfer in which subsequent GPO byte interrupts are locked out. This guarantees that other routines and tasks will be able to execute during that time period.

At the end of each byte transfer sequence, the FDIO GPO will pulse the GPOINTACK/ signal to terminate the GPO I/O REQUEST signal and inform the Host that the FDIO GPO has finished the current byte operation. The pulsing of the GPOINTACK/ signal produces a low to high transition, which also is a clock input to the delay flip-flop (U55). This clock input sets the byte delay flip-flop, making its Q output (U55-7) a logic low. The active Q/ output (or the active BYTEDLY/ at the TTL voltage level) releases the counter from its reset state and starts the counter. The active BYTEDLY/ signal is one of the 4 inputs to the 4-input AND gate (U49-5) and prohibits the FDIO GPO hardware from generating the next GPO I/O REQUEST signal. This delays the next byte transfer sequence. When the counter reaches its preset count value, the output of the counter will produce an active logic output. Through an inverter (U57) and an OR gate (U45), the output of this counter is converted to the proper logic state to reset the delay flip-flop on its CLR/ input (U55-1). When the delay flip-flop is reset, the Q/ output of the delay flip-flop switches from a logic low state to a logic high state, the BYTEDLY/ signal becomes a TTL high voltage level. The inactive BYTEDLY/ signal resets the counter and maintains the counter in its reset state. Also, the inactive BYTEDLY/ signal releases the FDIO GPO hardware to produce the next GPO I/O REQUEST signal and thus resume the next byte transmission.

2.2.2.3.4 GPI Interface Logic. (Figure 11-7, Sheet 8) The GPI circuit on the utility board employs special interface hardware that allows the FDIO system to communicate with the GPI adapter of the Host over the GPI interface.

The GPI circuit consists of the four following logical sections:

1. GPI signal interface circuit
2. GPI controller and handshake logic
3. GPI parity generator
4. GPI abort detection circuit

2.2.2.3.4.1 GPI Signal Interface Circuit. (Figure 11-7, Sheet 8 (11)): This circuitry consists of two 75124 receiver chips (U12 and U20), and several 75123 driver chips (U5, U11, U14, U19, U29, and U44). The following input signals are received from connector J3, and buffered to produce TTL level signals used internal to the utility board:

J3	Input Signal	Internal Signal
29	GPI Adapter Response	GPIARSP/
23	DCL1	GPIDCL1
24	DCL3	GPIDCL3

J3	Input Signal	Internal Signal
25	DCL4	GPIDCL4
26	DCL5	GPIDCL5

The following utility board internal TTL output signals are buffered and transmitted via connector J3:

Internal Signal	Output Signal	J3
GPID0 (MSB)	GPIDATA7	39
GPID1	GPIDATA6	38
GPID2	GPIDATA5	37
GPID3	GPIDATA4	36
GPID4	GPIDATA3	35
GPID5	GPIDATA2	34
GPID6	GPIDATA1	33
GPID7 (LSB)	GPIDATA0	32
GPIPAR	GPIPARITY	40
OBF	GPIIOREQ	30
GPIEM	GPIEOM	27

2.2.2.3.4.2 GPI Controller and Handshake Logic. (Figure 11-7, Sheet 8 (12)) The GPI circuit utilizes an 8255A PPI and supporting logic to perform the 8-bit parallel output and handshake operations. The PPI is organized as three 8-bit bidirectional I/O ports and is directly accessible from the iSBC 88/45 processor, via the Multibus. The GPI PPI is a memory mapped I/O device, in that data and status inputs are accomplished by the iSBC 88/45 performing a memory read operation and data and command operations are accomplished by the iSBC 88/45 performing a memory write.

The GPI PPI is assigned the memory address range 0F800 through 0F803 (hex), and is enabled by the signal GPICS/ (see paragraph 2.2.2.3.2.1). The specific address assignments are as follows:

Memory Address	Function
0F800	PORT A — output: output 8-bit GPI data character
0F801	PORT B — input: GPI control and status lines
0F802	PORT C — input/output: GPI handshake lines
0F803	CONTROL REGISTER — output

The functional configuration of the PPI is programmed by the system firmware residing on the iSBC 88/45. Each of the three ports may be configured to be either input, output, or both. In addition, the PPI supports three modes of operation:

1. Mode 0 (Basic I/O) — Each port is configured as an 8-bit input or output port, with no handshake provided. All three ports are available as I/O lines.

2. Mode 1 (Strobed I/O) — This configuration provides a means for transferring data to or from a specified port in conjunction with strobes or handshake lines. In this mode, ports A and B provide dedicated input or output lines, while the lines of port C are used to generate or accept the handshake signals required by ports A and B.

3. Mode 2 (Strobed bidirectional I/O) — This mode is similar to Mode 1, except Ports A and B provide for bidirectional data transfers.

The GPI PPI is configured as follows:

Port A — This port is configured as output port operating under mode 1. The 8-bit data byte to be sent to the Host via the GPI interface is output on port A. Port C bits 3, 6, and 7 provide the interrupt and handshake signals required by the interface.

The 8-bit GPI data character is output by writing to port A of the GPI PPI, memory address 0F800 (hex):

MSB LSB

7	6	5	4	3	2	1	0

Bit	Description
0-7	GPID0-GPID7 8-bits of GPI data

Port B — Port B of the GPI PPI is configured as an input port and allows for the reading of eight GPI status bits (not to be confused with DSL lines). This is accomplished by reading memory address 0F801 (hex):

MSB LSB

7	6	5	4	3	2	1	0

Bit	Description
0	GPI PAR: This bit is a copy of the parity bit output of the parity generator that is sent out over the GPI interface.
1	ICL INT/: This bit is used by the ICL interrupt handler
2	CK FOR PAR: This bit is set when DCL1 drops low.
3	GPI ABORT: This bit is set when a GPI abort condition exists.

Bit	Description
4	GPI DCL5: This bit is a copy of DCL5.
5	GPI DCL4: This bit is a copy of DCL4.
6	GPI DCL3: This bit is a copy of DCL3.
7	GPI DCL1: This bit is a copy of DCL1.

Port C — Port C of the GPI PPI performs both dedicated output operations as well as the handshake functions required by port A. All bits except 3, 6, and 7 are configured as output and are used as control bits. Bits 6 and 7 provide the handshake lines for port A and bit 3 is the port A interrupt line. The following control bits are set or reset by writing an 8-bit control word to port C of the GPI PPI, memory address 0F802 (hex):

Bit	Description
0	EVEN PARITY: When inactive (low), this signal sets the parity for the GPI character to odd.
1	WAIT DCL1: When active (high), this signal enables the circuit that tests for DCL1 going inactive.
2	CLR GPIINT/: When active (low), this signal clears the GPI interrupt request signal.
3	GPI INTREQ: This signal invokes a GPI hardware interrupt and is generated automatically by the GPI PPI when a character has been sent.
4	GPI EM: When active (high), this signal raises the GPI EOM interface line.
5	GPI ENB: When active (high), this signal enables the GPI transmit buffers of the primary control unit.
6	ACK/: This is an automatic handshake signal, and receives the GPI ADAPTER RESPONSE signal.
7	OBF/: This is an automatic handshake signal and activates GPI IOREQ.

A control byte written into the control register (address 0F803 hex) determines the specific configuration as shown below:

MSB LSB

7	6	5	4	3	2	1	0

Bit	Description
7	(=1) must be set to activate control word.
6,5	(=01) configures port A for MODE 1 operation.

Bit	Description
4	(=0) configures port A as an output port.
3	(=0) configures port C bits 4-7 as output.
2	(=0) configures port B for MODE 0 operation.
1	(=1) configures port B as an input port.
0	(=0) configures port C bits 0-3 as output.

2.2.2.3.4.2.1 Operational Sequence. Before the GPI interface can be used to communicate with the Host, it must be enabled. This is accomplished by performing a memory write operation to port B with bit 5 set to a logical high, causing signal GPIENB to become active. GPIENB is combined with XMTRENB and GPIABORT/ (U47), and generates signal GPIOUTENB which enables the 75123 output drivers. The Boolean for GPIOUTENB is as follows:

GPIOUTENB = XMTRENB AND GPIENB AND GPIABORT/

XMTRENB originates with the fail-safe interface logic, and indicates that the utility board is a part of the primary control unit, and therefore has control of the GPI transmitter logic. GPIABORT/ indicates a GPI abort operation is in progress, and is normally high (See paragraph 2.2.2.3.4.4. for a description of the GPI abort detection logic).

Whenever the GPI firmware wishes to send a character to the Host over the GPI interface, it performs a memory write operation to port A of the GPI PPI. Port A operates in mode 1, using bits 3, 6, and 7 of port C for handshake and interrupt lines.

Refer to Figure 2-7, Port A GPI Timing diagram, during the following discussion.

The GPI data byte written to port A of the GPI PPI is latched by the low to high transition of the memory write line (MWT/), and appears on lines GPID0 through GPID7 (U37-37 to 40, and 1 to 4). As part of the mode 1 operation, internal logic within the GPI PPI causes signal OBF/ (U37-10) to drop, indicating that valid data is present on the port A output lines. OBF/ is inverted, and buffered by the driver (U14-6), and becomes the interface signal GPI IOREQ. The active OBF/ signal produces an active GPI IOREQ signal.

The Host recognizes that a character is available from FDIO when GPI IOREQ is active. When it is ready to accept the data byte, the Host raises the interface handshake signal GPI ADAPTER RESPONSE, which is received by the 75124 receiver (U12-14), inverted, and becomes GPIARSP/. This signal passes through the GPI abort detection circuit, becoming ACK/ which is presented to the GPI PPI (U37-11). Upon detecting the high to low transition of ACK/, the GPI PPI raises the signal OBF/, thereby causing GPI IOREQ to go low. The Host responds by dropping GPI ADAPTER RESPONSE, causing ACK/ to go high, indicating the end of the byte transfer. Upon sensing the trailing edge of ACK/, the GPI PPI raises the interrupt line GPI INTREQ (U37-17). This causes the interrupt flip-flop (U43-9) to set. The signal is buffered by the 7407 (U69), and becomes signal GPIINT which is presented to the Multibus, and ultimately causes a GPI interrupt operation to be performed. This interrupt informs the GPI firmware that the previous byte has been received by the Host, and that another byte can be sent. The interrupt flip-flop is cleared during the interrupt handler via signal CLRGPIINT/, and signal GPIINTREQ is automatically cleared by the GPI PPI when the next data byte is written to port A.

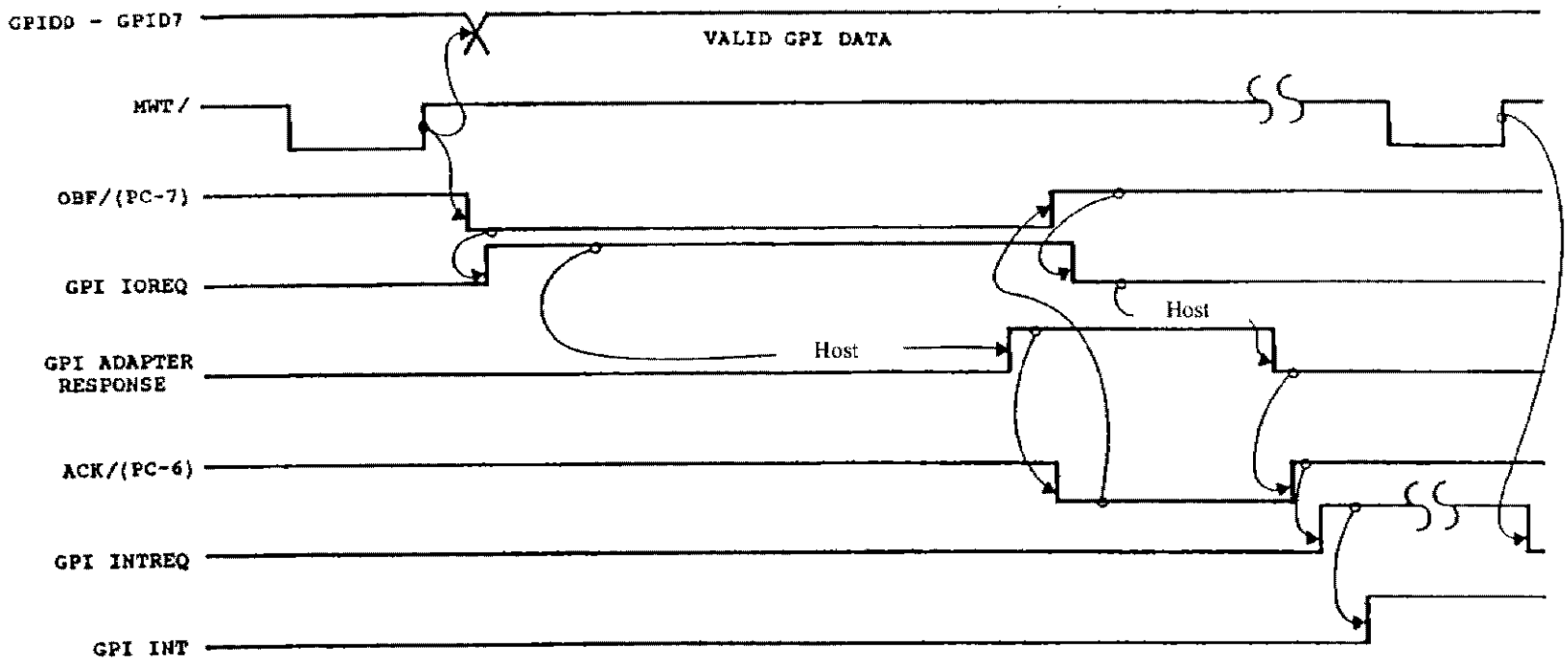


FIGURE 2-7. PORT A GPI TIMING DIAGRAM

When the last data byte has been sent, the GPI firmware activates signal GPIEM (U37-13). This signal is buffered by the 75123 driver (U14-15), and becomes the interface signal GPIEOM. Following the setting of GPIEM, a dummy GPI byte is sent out via port A in the same manner as mentioned above.

When the Host recognizes the EOM sequence, it will drop the interface signal, DCL1. When DCL1 is raised again, it will activate DCL3 if the previous received message has a parity error. The GPI interface contains logic to detect this temporary drop in DCL1, and to determine when GPI firmware should sample the DCL3 line.

During the EOM processing, after the GPI firmware has activated GPIEM, it raises signal WAIT DCL1 (U37-15) high. This arms the **K**/ input of the flip-flop (U55-13), and the 2-input AND gate (U48-2). When DCL1 drops at the EOM, the signal GPIDCL1/ presented to the other input of the 2-input gate (U48-1) goes high, causing the **J** input of the flip-flop (U55-14) to go high. On the next transition of the 1.37 MHz system clock, the **Q** output (U55-10) drives signal CKFORPAR high. The GPI firmware monitors this signal by reading port B bit 2 (U37-20). DCL1 must remain low for a minimum of .730 µs to guarantee being captured by this circuit.

The GPI firmware then monitors DCL1 by reading port B bit 7 (U37-25). When DCL1 goes high, the state of DCL3 may be determined by reading port B bit 6 (U37-24) to determine whether the preceding received GPI message has a parity error. CKFORPAR may be cleared at any time after its recognition by dropping signal WAITDCL1.

2.2.2.3.4.3 GPI Parity Generator. (Figure 11-7, Sheet 8 (13)): The 8-bit GPI data byte present on lines GPID0 through GPID7 are presented to the 74LS280 parity generator (U28) in addition to the 75123 drivers. The input signal EVEN PARITY is developed by the GPI PPI (U37-14), and determines whether even or odd parity will be generated. For normal operations, EVEN PARITY will be low. If an even number of the lines GPID0 through GPID7 are high, the even parity output (U28-5) will be high, driving GPIPAR high; producing odd parity overall. GPIPAR is buffered by the 75123 driver (U44-6), and becomes the GPI interface signal GPI PARITY.

The parity generator can be checked by outputting data with known parity to port A, setting EVEN PARITY accordingly, and reading the generated parity bit GPIPAR on port B bit 0 (U37-18).

2.2.2.3.4.4 GPI Abort Detection Circuit. Refer to Figure 2-8, GPI Abort Timing Diagram, and (figure 11-7, Sheet 8 (14)): during the following discussion.

A GPI abort condition is defined as the loss of DCL1 prior to the normal EOM processing. The GPI abort detection circuit constantly monitors the state of DCL1, and reports back to the GPI firmware. If an abort occurs prior to EOM processing, signal GPIEM will be low, and its inverse applied to the **D** input of the abort detect flip-flop (U43-2) will be high, thereby enabling it. If DCL1 drops low, signal GPIDCL1/ will make a low to high transition, clocking the **Q** output (U43-5) high, and setting signal GPIABORT. The inverse of this signal, GPIABORT/, is applied to the 3-input AND gate (U47-9), causing signal GPIOUTENB to become inactive. This disables the GPI drivers, preventing spurious signal transitions on the control lines.

GPIABORT/ is logically ANDed with signal OBF/ to emulate a false acknowledgment on ACK/ to the GPI PPI in case an abort condition disrupts the normal handshake sequence. It is imperative that the ACK/ line be activated to allow the internal mode 1 logic of the GPI PPI to complete its normal sequence, and generate the GPI interrupt.

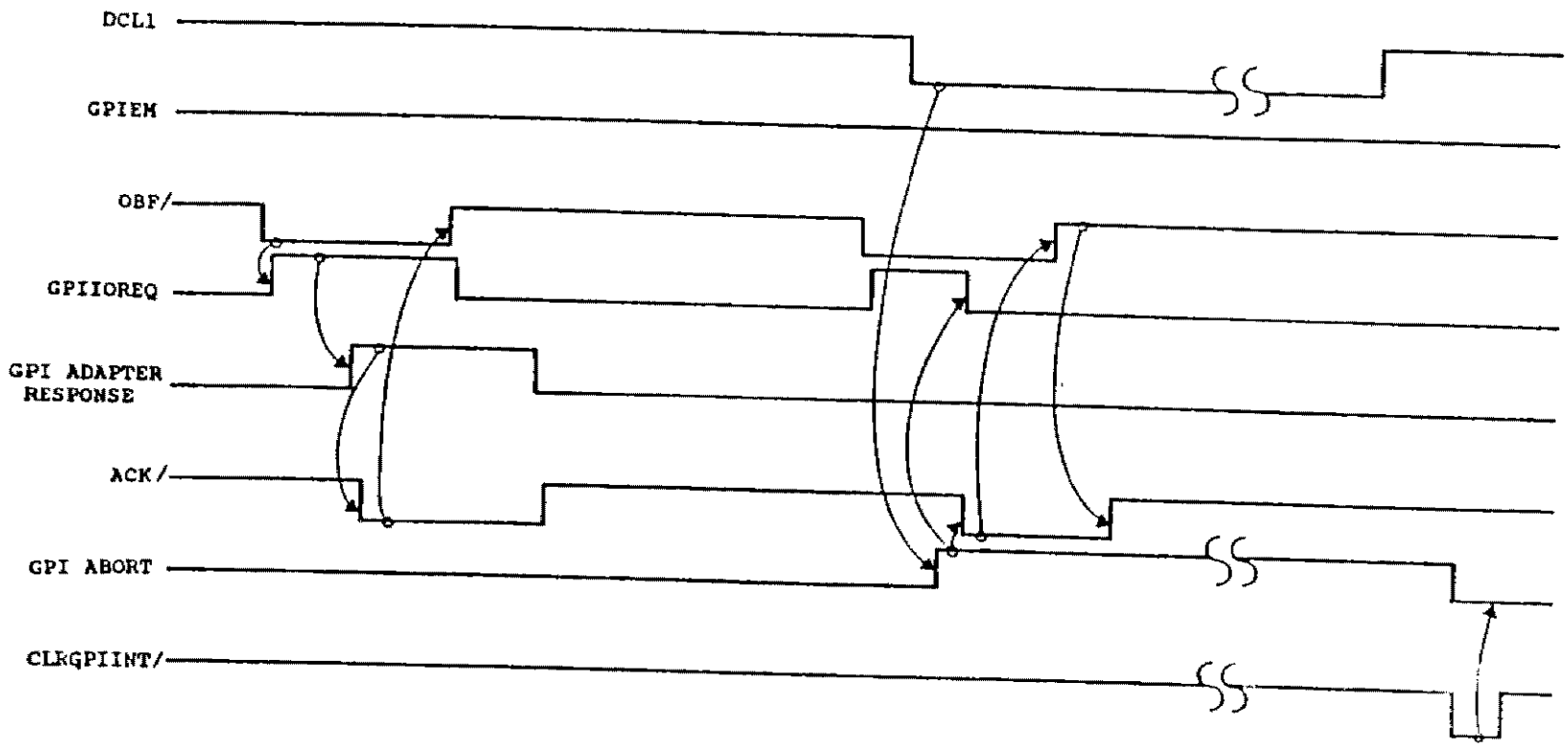


FIGURE 2-8. GPI ABORT TIMING DIAGRAM

During the GPI interrupt, the firmware reads the state of GPIABORT by looking at port B bit 3 (U37-21). If an abort condition exists, the output operation ceases, and DCL1 is monitored (by reading port B bit 7), waiting for it to go active again. When DCL1 becomes high, the state of DCL3 determines whether or not the original aborted message is resent (DCL3 is high), or the next message is sent (DCL3 is low).

2.2.2.3.5 FSE. (Figure 11-7, Sheets 4 and 5): The FSE consists of an independent microprocessor (8031 based) control unit and the transmitter control circuit. In a redundant system environment, the FSE arbitrates the transmitter control of the GPI/GPO and the LAN communication links. The FSE monitors the performance of the iSBC 88/45 processor and the FSE processor (8031-based) for the system fail safe operation.

The FSE circuit consists of the following three logical sections:

1. FSE controller
2. Expansion program memory
3. FSE interface circuit

2.2.2.3.5.1 FSE Controller. (Figure 11-7, Sheet 4 (15)): The FSE controller consists of the following three major sections:

1. Clock Circuit,
2. Jumpers on FSE Controller, and
3. Single Chip Microcomputer.

2.2.2.3.5.1.1 Clock Circuit. An external oscillator (OSC), operating at 11.059 MHz, is used to provide a square wave TTL clock. This clock, presented to the XTAL2 input of the microcomputer chip (U32), becomes the time base for all internal clocking signals. In addition, the 11.059 MHz clock is fed to the clock input of the transmitter available flip-flop (U35) and to a 4-bit binary divider (U51) 74LS161, where it is divided by 4 to produce a 2.74 MHz clock at its QB output (U51-13). The 11.059 MHz clock is also divided by 8 to produce a 1.37 MHz clock at its QC output (U51-12). The 2.74 MHz clock signal is used as a clock source for the asynchronous communication by the ICL controller (U15-20). The 1.37 MHz clock signal is used as the clock input (U54-10) of the GPO byte delay circuit, and is used as the clock input (U55-12) of the GPI interface control circuit.

NOTE

The path of the 11.059 MHz clock signal is provided through the Ground Plane of the Utility board, and prevents the clock signal from interfering with the surrounding signals.

2.2.2.3.5.1.2 Jumpers on FSE Controller. Jumper W5 disconnects the oscillator from the rest of the circuit allowing an external clock source to be injected during test. Jumper W1, when it is installed, allows a reset of the 8031 processor without having to generate a power reset. Jumper W3 and W4 are used for injecting external signals to test the processor.

2.2.2.3.5.1.3 Single Chip Microcomputer. The 8031 microcomputer (U32) is a complete, functional, microcomputer on a single silicon chip containing an 8-bit CPU, on-chip read/write memory,

parallel I/O, two 16-bit timer/counters, a full duplex serial port, and a five-source interrupt structure. The 128 bytes of internal RAM are partitioned into general purpose registers, special function registers, program stack, and general purpose memory for storing variables. The program for controlling the FSE resides in 4 Kb of off-chip EPROM.

Upon power up, a reset circuit made up of R8 and C22 guarantees that the reset input (U32-9) remains active until the power supply stabilizes, and the 8031 microprocessor is able to begin operation.

The 8031 contains four 8-bit bidirectional I/O ports (P0 through P3), which perform the following functions:

Port 0 — This port is used during the process of accessing external EPROM (U24). The port alternates between containing the lower 8-bits of the 16-bit external address and the actual data read from the EPROM, or the data read from the transmitter status register. The address latch, U23, is used to latch the lower eight address lines (FSED0 through FSED7) emanating from port 0 of the 8031 during the address set up time.

Port 1 — These 8 bits are configured as a special output port for controlling the transmitter circuit. The function of each bit of the Port 1 is described as follows:

Bit	Description
0	DINOP: When active this signal forces the interface signal, DEVICE INOP, into an active state. It is used when the GPO interface undergoes an internal reset, and keeps the Host PAMRI from timing out.
1	DCLTEST/: This signal is used by the secondary unit to induce the condition of a Host hardware special read operation, by activating the DCL1, 3, and 4 lines. The secondary unit uses a special read circuit if operational.
2	XRELCMD/: This signal is activated when a switch is caused due to the other unit exhibiting a failure condition. It allows this unit to reset the other unit and force the failed unit to a reset condition to prevent the failed unit from interfering with operations
3	XREQ/: This signal is activated as a first step when control unit wishes to become the primary unit, and gain control of the transmitter.
4	WD: This signal is used to indicate the operation of the watchdog pulse of the other unit.
5	SELFERR: When this signal is activated, it indicates that the unit detected a failure with itself. The self failure occurs when the time elapsed since the last handshake between FS and FSE of this unit has exceeded its time limit.
6	WDERR: When this signal is activated, it means the other unit failed to update the watchdog timer on this unit within the allowable time.
7	FSEINT/: When used, this signal will provide the FSE with the capability to report any error to the FS module through an interrupt instead of polling. This scheme is not currently used.

Port 2 — Port 2 contains the upper 8-bits of the 16-bit address that accesses the external memory locations, such as the EPROM and the transmitter control status.

Port 3 — Port 3 is configured as a special function port, with each bit position performing the following special functions: Bit 2 and bit 3 are used for inputs and the remaining bits are used for outputs. Bit 7 is the MSB. Bit 0 is the LSB.

Bit	Description
0	RSTENB/: FSE activates this signal when it detects it has an internal failure, and allows the other unit to reset this failed unit's iSBC 88/45 processor.
1	Not used.
2	WDIN/: External interrupt 0 is generated by the other unit's FS module when it resets the watchdog time out counter (timer 1 of 8031) of this unit.
3	CMDSECSW/: External interrupt 1 is generated when the Host activates a special read switch, or secondary unit tests the special read switch circuit by activating the DCL1, 3, and 4 device control lines.
4-5	Not used.
6	FSEWT/: This output signal is activated when 8031 processor executes an external write operation (external data write strobe signal).
7	FSERD/: This output signal is activated when 8031 processor executes an external read operation (external data read strobe signal).

These signals will be discussed in detail in the subsequent paragraphs.

2.2.2.3.5.2 Expansion Program Memory. (Figure 11-7, Sheet 4 (16)): The 8031 microcomputer fetches and executes program instructions from the off-chip expansion program memory EPROM. Although the 8031 microprocessor can address up to 64 Kb of program memory, the FSE only contains a single 24-pin socket (U24) that can accommodate a 2732 (4 Kb) EPROM. The 4 Kb EPROM requires 12 address lines in order to access all possible locations.

Refer to the Figure 2-9, EPROM Read Cycle Timing diagram, for the following description of an EPROM read cycle. To access off-chip memory, the 8031 microprocessor makes use of ports 0 and 2.

During the first part of the read cycle, the lower 8 bits of the address are output on port 0 (FSED0-FSED7), and the upper 8 bits are output on port 2 (FSEA8-FSEAF). When the address lines are stable, the 8031 causes signal ALE (U32-30) to make a high to low transition, causing the lower 8 address bits from port 0 to be latched by the transparent latch (U23). The upper address bits do not require external latching, since the 8031 keeps them stable throughout the entire read operation. The latched addresses (FSEA0-FSEA7) are presented to the EPROM to select the desired location.

When the required address setup time delay has elapsed, the 8031 causes signal PSEN/ (U32-29) to go active low. This enables the contents of the selected EPROM location onto the port 0 lines, which have since become inputs.

The 8031 reads the contents of the EPROM via port 0. When the operation is complete, PSEN/ is de-activated thereby disabling the output of the EPROM, and a new memory address is set up on ports 0 and 2.

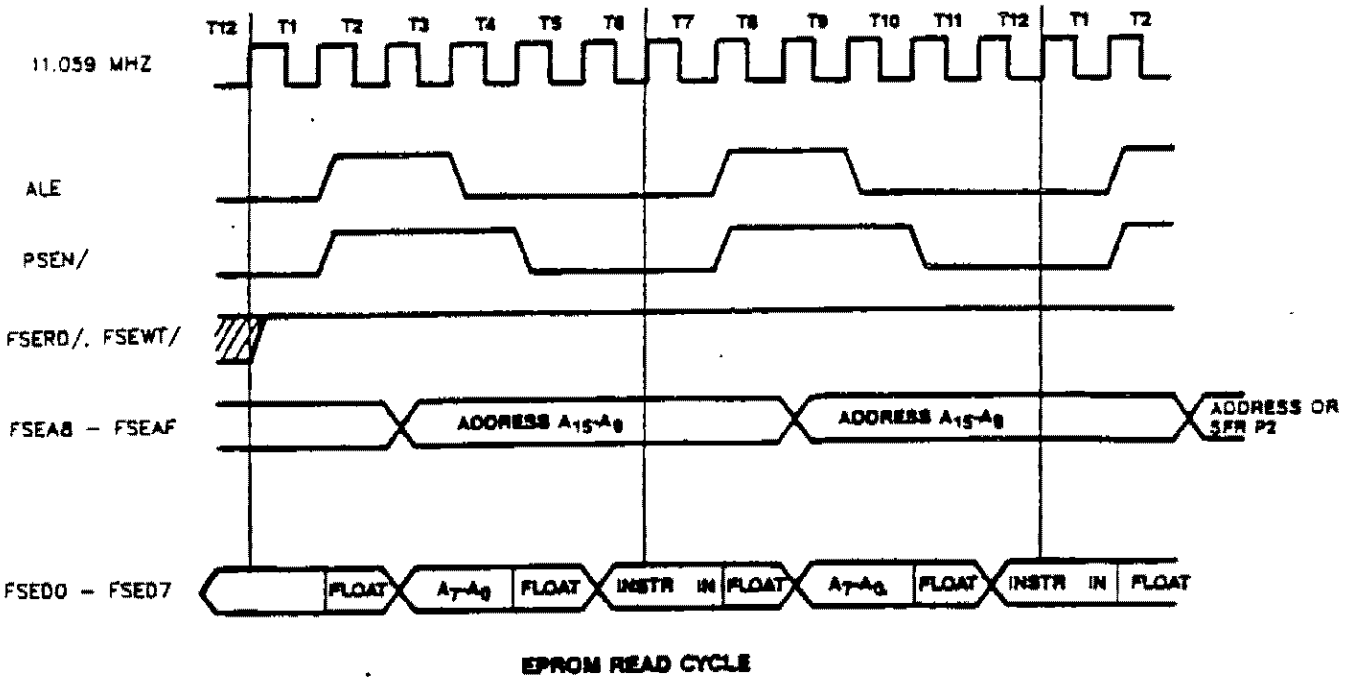


FIGURE 2-9. EPROM READ CYCLE TIMING DIAGRAM

2.2.2.3.5.3 FSE Interface Circuit. (Figure 11-7, Sheets 4 and 5 (17)): The FSE interface circuit consists of: Fail Safe (FS) to FSE interface circuit, FSE transmitter control circuit, and a watchdog timer circuit.

2.2.2.3.5.3.1 FS to FSE Interface Circuit. The FS module is a part of the FDIO firmware which communicates with the FSE through two registers. The first register is the FS command register, and the second register is the FSE status register. The FS command register (U25) is a write-only register for the FS module and a read-only register for the FSE. The FS module writes the FS command to this register, and the FSE reads the command contained in this register. The FS issues a command to the FSE by performing a memory write operation at the location of the FS command register (0FC00 hex). When the FS performs a write operation at this location, it will output the address and data for this location, and then activate the memory write signal (MWT/). The address lines, set for location 0FC00 hex, will activate the FSECS1/ signal through the MMIO device select decoder (U63). The active MWT/ and FSECS1/ signals will activate the OR gate output (U38-6). This active low signal enables the 8-bit latch, to latch the current FS command on the data bus into the latch (U25, 74LS374). The contents of this 8-bit latch will not be altered until the next FS command write operation. The FSE receives the FS command through a memory read operation at external address location 0. To read at this address, the 8031 processor will activate the FSERD/ signal with the address bit, FSEA0, being a logic low. The FSEA0 being low and FSERD/ signal produce an active low FSECMDRD/ signal. The active FSECMDRD/ signal activates the output enable of the latch (U25-1) which allows the current FS command onto the FSE data bus.

The FSE status register (U33) is used for the FSE to pass the transmitter control status to the FS module. The FSE status register is write-only for the FSE, and read-only for the FS module. The FSE writes the current transmitter control status through a memory write operation at external address location 1. This external write operation will activate the FSEWT/ signal which latches the current FSE status data on the FSE data bus into the FSE status register. When the iSBC 88/45 performs

a memory read operation at address location 0FC00 hex, the FSECS1/ and the MRD/ signals are activated which generates the FSSTATRD/ signal at the OR gate output (U38-8). The FSSTATRD/ signal activates the output enable of the latch (U33-1) which allows the FSE status to pass to the FS.

The data format of the FS command register and the FSE status register is described in the following:

Bit	iSBC 88/45 Description
0	DIAG: The FS activates this bit when it starts the handshake with the FSE. The FSE de-activates the AVAIL bit to tell the FS module that the FSE has finished the diagnostics and the result is ready for FS module. Upon ending this handshake sequence the FS de-activates the DIAG bit and FSE activates the AVAIL signal to acknowledge the end of handshake sequence.
1	8031 RDY: The FSE activates this bit to inform the FS module that the FSE is operational.
2	SW: The FS activates this bit when it wishes the FSE to perform a unit switch operation.
3	FAIL: This signal is activated when a failure is detected.
4	AVAIL: This bit is used in conjunction with the DIAG bit for FS module to FSE handshake operations.
5	SYNC: When this bit is active, the system is in redundant operation (the primary unit and the secondary unit are operational).
6	(PRI or SEC/): When this bit is active, this unit is assigned as the primary unit.
7	XMTRRDY: The FSE will activate this bit when it acquires the transmitter control. This bit is used for the FSE to report the result of the transmitter request issued by the FS module.

2.2.2.3.5.3.2 Transmitter Control Circuit. The purpose of this circuit is to arbitrate the control of the transmitter between the redundant units.

The XMTRAVAIL signal is shared between two units and used by each unit in order to determine whether the current transmitter is busy. Upon power reset, the transmitter control flip-flop (U35) is reset (the Q output of the flip-flop (U35-9) is in a low state). When a unit requests control of the transmitter, the FS module of this unit will issue a transmitter command to the FSE. The FSE will check the current transmitter status before it issues the transmitter request to the transmitter control circuit. If the transmitter is not busy, which is indicated by the XMTRAVAIL signal being active, the FSE will issue a transmitter command by activating the XREQ/ signal. The XMTRAVAIL signal is active and the Q output of the flip-flop is inactive which produces an active high on the 2-input XOR-gate (U10-3). Also, during normal operation, the RSTENB/ signal is inactive, and the XRELCMDIN/ signal from the other unit is in a logic high state. The XRELCMDIN/ signal will activate the 3-input AND gate (U18-6), since the other 2 inputs are also in a logic high state. This active signal on the D input of the flip-flop allows the flip-flip to be set on the next rising edge of the 11.059 MHz clock signal. The active Q output and inactive Q/ output latches the transmitter control state by activating the 2-input XOR-gate. Therefore, once a unit acquires the control of the transmitter, the unit will continue to control the transmitter until it releases the transmitter control (by de-activating the XREQ/), or it is forced

by the other unit (due to a detection of a failure on this unit). When the flip-flop is set, the Q/ output becomes low, and de-activates the XMTRAVAIL signal. The inactive XMTRAVAIL signal implies that the transmitter is busy.

There are two registers (U16 and U9) provided for the FSE and the FS module to read the current transmitter control status. The first register is the transmitter status register (U16) which is used by the FSE to read the current transmitter control status. The FSE can read the XMTRAVAIL, CMDSECSW, XMTRENB, and XREL/ signals through the read operation at external address location 1. The FS module is able to read the transmitter control status through the read operation at memory location 0FD00 hex. After the FSE issues the XREQ/ signal to the transmitter control circuit, the FSE can read the XMTRENB signal to determine if the request to control the transmitter is successful. If the result of transmitter request with the XMTRENB signal, is active, then the request is granted, and the current unit becomes the primary unit.

When a primary unit fail-safe failure condition occurs, the FSE of the failed primary will detect this due to the elapsed time since the last handshake between the FS module being longer than the allowable time-out limit (2 seconds). The FSE of the failed primary unit will activate the RSENB/ signal (U32-10) to indicate the primary failed condition and allow the other unit to take over and reset the failed unit. The FSE of the other unit will detect the primary unit has failed due to the time elapsed. In this condition, the secondary unit will force the failed primary unit offline by switching out the failed primary unit. In the switch process, the FSE secondary unit will activate the XRELCMD/ signal, and the FS module will activate the CMDSWENB/ signal. The active XRELCMD/ and CMDSWWNB/ signals will activate the output of 2-input OR gate (U27-11). The active U27-11 signal is fed into the failed unit through the FSE cable along with the active RSTENB/ signal which activates the 2-input OR-gate (U27-8). The active U27-8 signal will first de-activate the 3-input AND gate and de-activate the D input of the flip-flop which resets the control flip-flop on the next rising edge of the 11.059 MHz clock. This releases the transmitter control from the failed primary unit. Then the active U27-8 signal produces an active INIT/ through an open-collector (U4). The active INIT/ signal activates the reset signal to the processor on the iSBC 88/45 board through the Multibus interface backplane. The failed unit will remain in the reset state until it is powered down.

2.2.2.3.5.3.3 Secondary Unit Special Read Circuit. The FSE of the secondary unit tests the special read circuit (when the DLC1, 3, and 4 lines are active, generating a special read switch command to the switch unit), during the period when FSE handshakes with the FS task. When FSE tests the special read circuit, the DCLTEST/ signal is activated at U32 port 1 pin 2. The active DCLTEST/ signal forces the 75124 GPI receiver (U12 and U20) to output a logic 1 on each output; that is, the DCL1, 3, and 4 lines become high when the DCLTEST/ signal is active. The active DCL1, 3, and 4 lines in turn activate the output of the 3-input AND GATE (U18-8 on figure 11-7) generating an active CMDSECSW. The active CMDSECSW signal triggers the 8031 processor with an interrupt through the inverter, U42. The active low output on U42-10 provides the interrupt request to the 8031 processor (FSE). Then, the FSE services this interrupt and determines that the special read circuit is functional. If FSE does not receive the interrupt during the time out period, the circuit being checked is considered to have failed, and FSE reports the failure to the FS task.

2.2.2.3.5.3.4 Watchdog Circuit. The criteria to determine if a unit of a redundant pair is operational, is determined by the time elapsed since the last watchdog pulse. The FS module of each unit will output a watchdog pulse every second to the FSE of the other unit via the FSE cable (See table 2-17 for a description of the interface signals). The appearance of the watchdog pulse will reset the watchdog time-out timer of the other unit, and resume the counting on the next watchdog clock pulse. The FS module outputs a watchdog pulse which sets the Port C data bit 4 WD signal (U36-13) to logic high state. This signal drives an open-collector inverter (U8), and converts it to low active logic.

The appearance of this low-active signal will cause an interrupt on the FSE of the other unit. This watchdog interrupt causes this FSE to reset the time-out timer and restart the counting from the beginning value.

TABLE 2-17. FSE CABLE DEFINITION

J1 Pin	Signal Name	Signal Definition
2	WDOUT/	Watchdog timer output pulse to the other control unit.
1	WDOUTECHO/	Watchdog timer output pulse echo from the other control unit.
13	WDIN/	Watchdog timer input pulse from the other control unit.
14	WDINECHO/	Watchdog timer input pulse echo to the other control unit.
5	XRELCMDIN/	Request from the other control unit to release the transmitter.
10	XRELCMDOUT/	Request to the redundant control unit to release the transmitter.
6, 9	XMTRAVAIL/	Signal common to both control units indicating that the transmitter is available.
4	FSECABLE/	Signal indicating the FSE cable is connected.
3, 7, 8, 11,12	GROUND	FSE signal ground.

2.2.2.3.6 ICL. (Figure 11-7, Sheet 9) The ICL provides the communication link between two redundant units (the primary unit and the secondary unit). Through the ICL communication link, these two units are able to communicate with each other in order to synchronize the operation of both units.

The hardware link occurs via the ICL cable connected to connector J2 of the utility boards. Table 2-18 describes the signals present on the ICL interconnect cable. The ICL consists of a serial communications controller, a loop-back circuit, and interface signal drivers.

TABLE 2-18. ICL CABLE DEFINITION

J2 Pin	Signal Name	Signal Definition
2	TxDA	Serial transmit data channel A
7	TxDB	Serial transmit data channel B
9	RxDA	Serial receive data channel A
4	RxDB	Serial receive data channel B
1	ICLCABLE/	Signal indicating the ICL cable is connected.
3	IORQOUT	I/O REQUEST signal from GPO handshake logic to the other control unit.

TABLE 2-18. ICL CABLE DEFINITION (Continued)

J2 Pin	Signal Name	Signal Definition
8	IORQIN I/O	REQUEST signal from GPO handshake logic of the other control unit.
5, 6,		
10	GROUND	ICL signal ground

2.2.2.3.6.1 Serial Communications Controller. (Figure 11-7, Sheet 9 (18)): The Serial Communications Controller (SCC) circuit consists of an 82530 (U15) containing two separate serial communications channels, A and B. Channel A is used for transmitting commands and data to the other control unit, while channel B is used for responding to commands and data received from the other control unit.

Upon power up of the utility board, signal RESET/ is held active low until the system has stabilized. This signal is ORed with the MRD/ and MWT/ signals applied to the SCC by the 74LS08 gates (U40). This causes the RD/ and WR/ inputs to the SCC (pins 35 and 36) to be driven low simultaneously. This normally **illegal** condition causes the SCC to perform an internal reset operation.

The SCC is accessed as an MMIO device, in that it appears to the processor (on the iSBC 88/45) as a range of memory locations. Commands and data are sent to the SCC by performing a write to the desired memory location; status and data are read from the SCC by performing a read from the desired location. The MMIO addresses are as follows:

Address (hex)	SCC Port Selected
0FA00	Channel B command/status port
0FA01	Channel A command/status port
0FA02	Channel B data port
0FA03	Channel A data port

Address bits ADR0 and ADR1 are presented to the SCC to select the desired port (A, B, command/status, or data), and address bits ADR8 through ADRF are decoded by the MMIO select circuit. Signal ICLCS/ originates from the MMIO device select decoder U63-13, and is connected to the chip select input of the SCC (U15-33). ICLCS/ becomes an active logic low level when the SCC is the selected source of a memory read or write operation. This occurs when ADRF, ADRE, ADRD, ADRC, ADRE, and ADR9 are all at a logic one, and ADR8 and ADRA are at a logic zero. The Boolean equation is as follows:

$$\text{ICLCS/} = \overline{\text{ADRF AND ADRE AND ADRD AND ADRC AND ADRB AND ADRA/ AND ADR9 AND ADR8/}}$$

When a memory read or write is made within the address range of 0FA00 through 0FAFF (hex), ICLCS/ is activated, which enables the SCC for I/O operations.

If a read operation is to be performed, signal MRD/ is applied to the SCC, via pin 36, after the required address and chip select setup delays have elapsed. This enables the contents of the status, or data register onto the data lines (DAT0-DAT7). This data can then be read by the iSBC 88/45 processor board.

If a write operation is to be performed to the SCC, the control, or data byte is placed on the data lines (DAT0-DAT7). After the required address, data, and chip select setup delays have elapsed, signal MWT/ is applied to pin 35 of the SCC in the form of a negative pulse. This cause the contents of the data bus to be written into the SCC.

2.2.2.3.6.2 Loopback Circuit. (Figure 11-7, Sheet 9 (19)): The 74LS241 (U2) functions as a loopback circuit for the two ICL channels. This part contains eight tri-state buffers organized as two independent groups of four. Each group of four is enabled by an appropriate input signal. Group A consists of four buffers with inputs of 1A0 through 1A3, and outputs of YA0 through YA3, and is enabled by the input line OEA/ dropping to a logical low level. Group B consists of four buffers with inputs of 1B0 through 1B3, and outputs of YB0 through YB3, and is enabled by the input line OEB being raised to a logical high level. OEA/ and OEB are connected together, and to signal LOOPTEST. Whenever LOOPTEST is low, group A buffers are enabled, and group B buffers are disabled. When LOOPTEST is high, group A buffers are disabled, and group B is enabled. LOOPTEST is driven from the DTRA/ pin of the SCC (U15-16).

The inputs and outputs of the loopback circuit are such that when LOOPTEST is low, the ICL receive data input signals RxDA (J2-9) and RxDB (J2-4) are connected to the inputs of the SCC; the ICL output signals TxDA (J2-2) and TxDB (J2-7) are connected to the outputs of the SCC (via 7407 buffers at U4). When LOOPTEST is high, the data outputs of the SCC are looped back to the inputs. This is illustrated in figure 2-10.

2.2.2.3.6.3 Interface Signal Drivers. (Figure 11-7, Sheet 9 (20)): When operating in non-loopback mode, the transmitted data from the SCC (TxDA and TxDB) is buffered by U4. The buffer (7407) is an open collector device with a 1K Ohm pull-up resistor on its output to provide the increased current drive necessary for driving the ICL cable. The interrupt output of the SCC (U15-5 is buffered by the 7404 (U64), and applied to the Multibus interface (P1-42).

2.2.2.3.7 Power Distribution. (Figure 11-7, Sheet 1 (21)): Power for the utility board is provided through the Multibus backplane, and enters on P1. The utility board requires only +5 V dc for operation. C32 and C33 are 10 Ultrasonic Frequency (UF) solid tantalum capacitors, and provide the bulk of the board decoupling, while a distribution of 0.1 UF capacitors provide for individual chip decoupling.

2.2.2.3.8 LED Indicators. Refer to paragraphs 3.2.1.1 and 3.2.1.2 for information regarding the functions of the LEDs on the utility board.

2.2.2.4 16 K RCU Memory Expansion Board. The purpose of the 16 K RCU memory expansion board is to increase the amount of buffer memory available in the RCU from 3.3 Kb of memory (the amount available on the Intel iSBC 88/45 processor board) to 19.3 Kb.

All address and data lines for the 16 K RCU memory expansion board are buffered, and present only one 74LS type load to the Multibus interface.

A block diagram of the 16 K RCU memory expansion board is shown in figure 2-11, and the schematic is shown in figure 11-8.

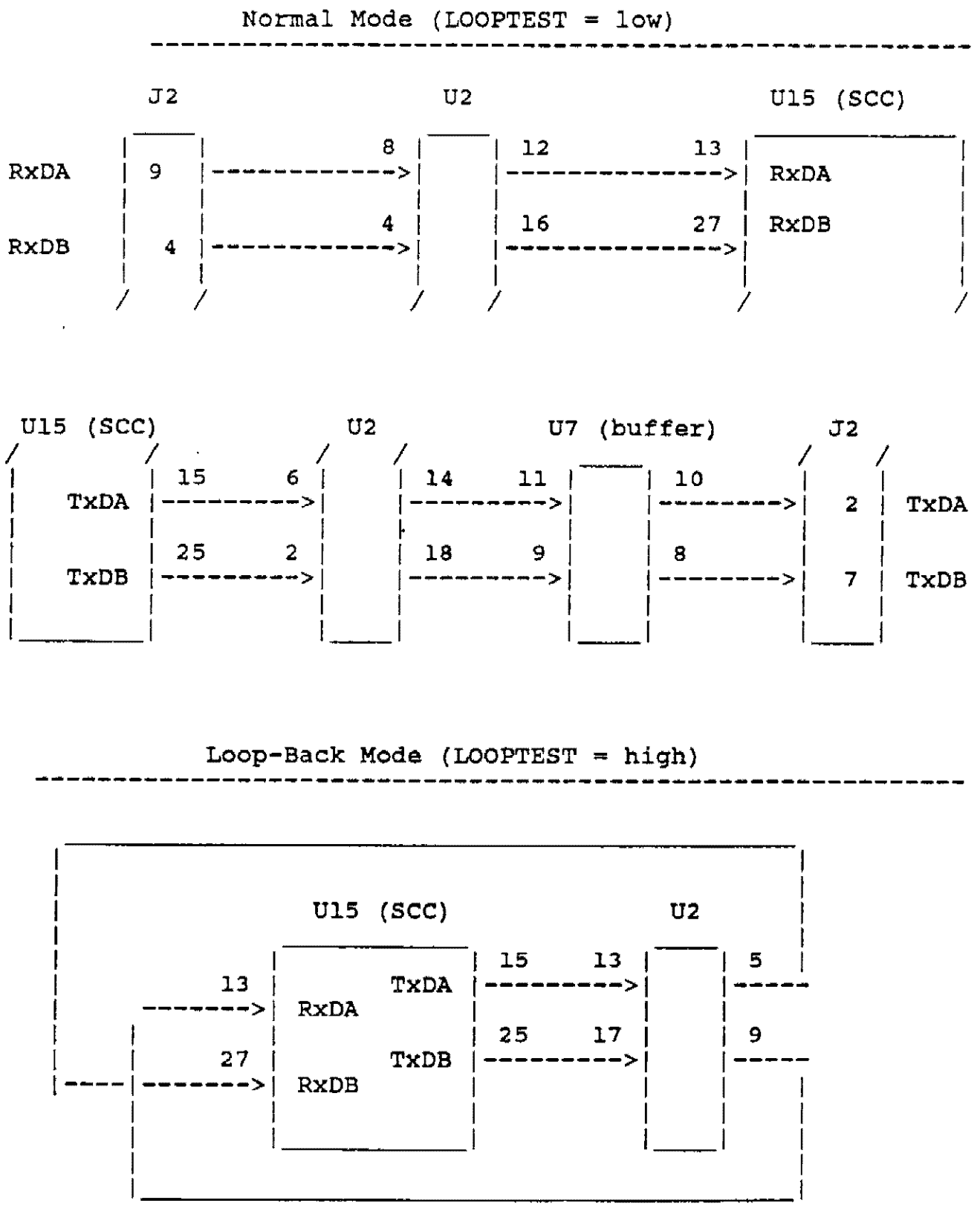


FIGURE 2-10. LOOPBACK OPERATION

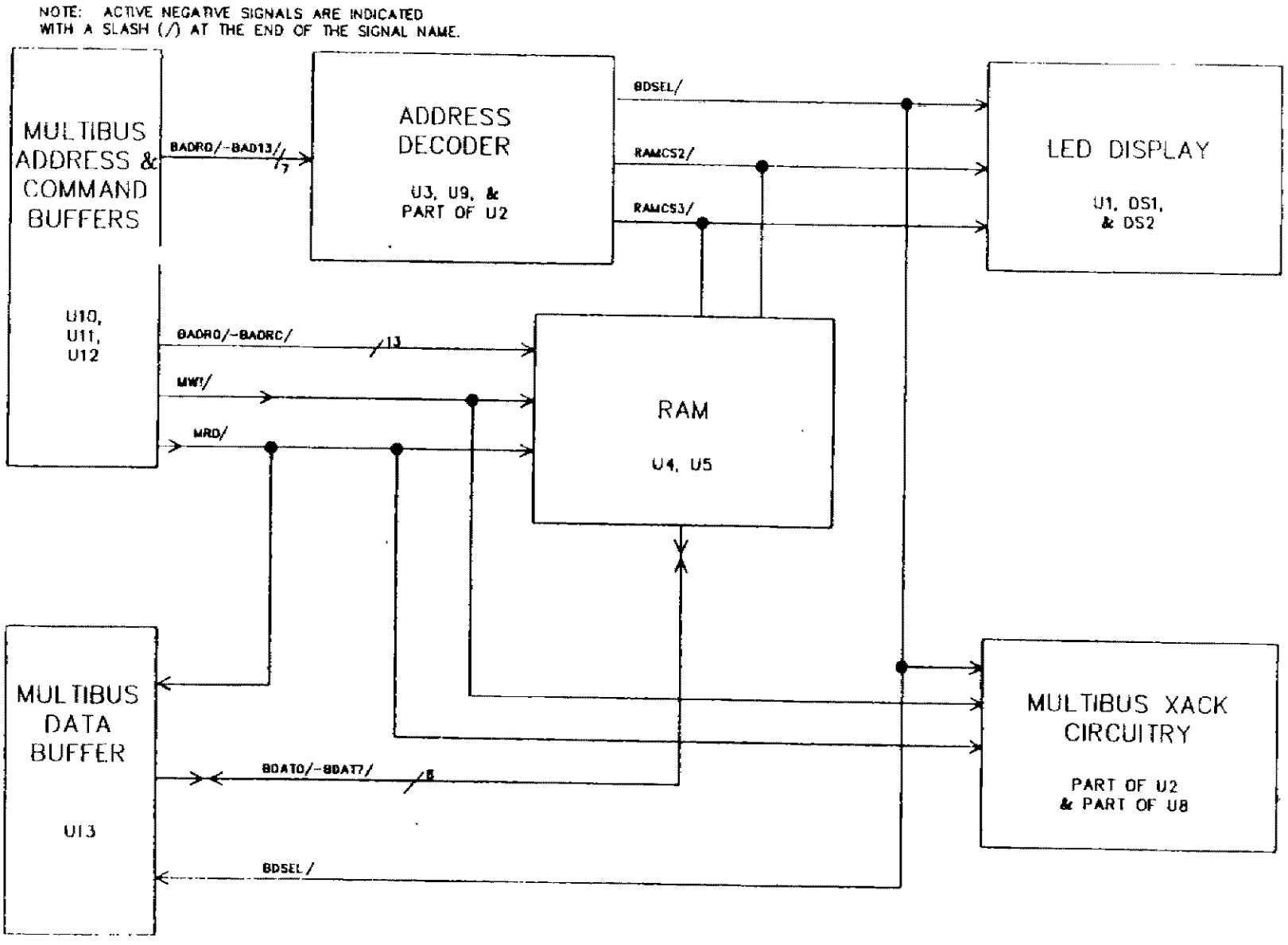


FIGURE 2-11. 16 K RCU MEMORY EXPANSION BOARD BLOCK DIAGRAM

2.2.2.4.1 Data Path. The data bus is bidirectionally buffered by data buffer, U13, (figure 11-8 (1)) which is a 74LS245 integrated circuit.

When data is written to RAM on the expansion board from the Multibus interface, the Multibus data is stored as presented in its inverted state. When the data is read from RAM on the expansion board and presented to the Multibus interface, the inverted data is corrected by the receivers on the iSBC 88/45 processor board.

Two signal lines, BDSEL/ and MRD/, to the 74LS245 control the direction of data in and out of RAM, and whether the data is in a location on the expansion board.

The BDSEL/ signal is generated by the expansion board in response to the address lines selecting an address from 00000H to 0FFFFH (the first 64 Kb segment or bank of memory). When the BDSEL/ line is active, the 74LS245 is enabled allowing data to be written to or read from RAM on the expansion board, depending on the MRD/ signal line status. Although the RAM on the Intel iSBC 88/45 processor board occupies a section of this area (00000H to 03FFFH), the iSBC 88/45 disregards any data presented by the Multibus interface when this section of RAM is selected. This allows for a simple address decoder discussed in paragraph 2.2.2.4.3.

The MRD/ signal is the buffered memory read command (MRdc/) presented by the Multibus interface to the expansion board. When the MRD/ line is active (low), the Multibus is requesting the data stored in the memory location selected by the address lines to be placed on Multibus data lines DAT7/ through DAT0/. When the address selected by the Multibus interface has caused the BDSEL/ line to become active, the 74LS245 will drive the Multibus interface with the data presented to it from the RAM on the expansion board.

If the MRD/ line is inactive (high) and the BDSEL/ line is active (low), a memory write command is in progress and the 74LS245 will drive the memory expansion board internal data bus with data received from the Multibus interface. The data is written to the memory expansion RAM when the MWT/ line is activated. MWT/ is the buffered memory write command (MWTC/).

2.2.2.4.2 Address Buffers. (Figure 11-8 (2)): The address buffers for the memory expansion board are U10, U11 and U12, and are all 74LS244 integrated circuits. These devices buffer the addresses presented to the memory expansion board from the Multibus interface.

2.2.2.4.3 Address Decoder. (Figure 11-8 (3)): The address decoder has four components: U3, U9, one NAND gate from U2, and a three position Berg jumper. The Berg jumper remains in the 1 to 2 connection position for operation. The 2 to 3 connection position is used for testing purposes only. The buffered segment address, ADR13/, is sent to the NAND gate (used as an inverter) and ADR10/ through ADR12/ are sent to U3, the segment decoder. The NAND gate inverts signal ADR13/. When the input signal to the NAND gate is inactive (high), the segment decoder is to be enabled. The NAND gate output signal is driven low which enables the segment decoder, U3. Since segment 0 is the address of the memory expansion board, and all the address lines (ADR10/ through ADR12/) are inverted, the segment decoder decodes segments as shown in table 2-19.

TABLE 2-19. SEGMENT DECODER OPERATION TABLE

ADR13/	ADR12/	ADR11/	ADR10/	DECODER OUTPUT	SEGMENT OR BANK
0	0	0	0	N/A	N/A
0	0	0	1	N/A	N/A

TABLE 2-19. SEGMENT DECODER OPERATION TABLE (Continued)

ADR13/	ADR12/	ADR11/	ADR10/	DECODER OUTPUT	SEGMENT OR BANK
0	0	1	0	N/A	N/A
0	0	1	1	N/A	N/A
0	1	0	0	N/A	N/A
0	1	0	1	N/A	N/A
0	1	1	0	N/A	N/A
0	1	1	1	N/A	N/A
1	0	0	0	0	7
1	0	0	1	1	6
1	0	1	0	2	5
1	0	1	1	3	4
1	1	0	0	4	3
1	1	0	1	5	2
1	1	1	0	6	1
1	1	1	1	7	0

The segment decoder output pin 7 decodes address 7, which is segment 0, and generates signal BDSEL/. The BDSEL/ is used to enable the 74LS245, the RAM chip decoder, U9, and the Multibus external acknowledge signal, XACK/.

When signal BDSEL/ is activated (low), the RAM chip decoder, U9, is enabled. The decoder selects which 8 Kb block in the 64 Kb segment is to be enabled from address lines ADRD/, ADRE/ and ADRF/. Each RAM chip is 8 K. Because the address lines ADRD/, ADRE/ and ADFR/ are inverted, the RAMs are selected as shown in table 2-20.

TABLE 2-20. RAM CHIP DECODER OPERATION TABLE

ADRF/	ADRE/	ADRD/	DECODER OUTPUT	RAM SELECTED
0	0	0	0	7
0	0	1	1	6
0	1	0	2	5
0	1	1	3	4
1	0	0	4	3
1	0	1	5	2
1	1	0	6	1
1	1	1	7	0

RAM0 and RAM1 are resident on the Intel iSBC 88/45 processor board. The first RAM that is active on the memory expansion board is RAM2, the second is RAM3. RAM4 through RAM7 are not used. Address lines ADR0 through ADRC are used to select a specific location within the selected RAMS on the memory expansion board.

The address lines, together with the BDSEL/ line, drive the input of the LED driver, U1, to indicate which RAM is being accessed on the memory expansion board.

2.2.2.4.4 XACK/ Operation. (Figure 11-8 (4)): The XACK/ line on the Multibus interface is used to inform the Intel iSBC 88/45 processor board that current offboard operations are completed. The signal is generated by three NAND gates of U2 and one open collector driver from U8. Because the speed of the RAMs used for the memory expansion board require no additional **wait states**, the XACK signal is generated by a memory read or write command to the 16 K RCU memory expansion board while the BDSEL/ signal is active.

When signal BDSEL/ is active (low), the input to the NAND gate on U2 at pin 12 is low. The NAND gate (used as an inverter) causes the output to go high which enables the second NAND gate to go low at pin 10. The output of the second NAND gate goes low whenever its input at pin 9 goes high, and this occurs in response to a memory read or write function detected by the third NAND gate.

When signal BDSEL/ is low, and either signal MRD/ or MWT/ is detected, the output of the NAND gate at pin 9 goes low driving the open collector driver at pin 1 of U1 to generate the XACK/ signal on the Multibus interface.

2.2.2.4.5 Memory Chip Operation. (Figure 11-8 (5)): The lower address lines, BADR0/ through BADRC/, are placed on all RAM address pins for internal decoding. Only the RAM, U4 (RAM 2) or U5 (RAM 3), which is selected by the RAM chip decoder, will decode this information (the enabled RAM Chip Select (CS) at pin 20 is low).

When a read operation is active, the information contained in the RAM location accessed by the address lines is placed on the memory expansion board internal bus when signal MRD/ is active (low).

When a write operation is active, the information on the memory expansion board internal data bus is stored into the location accessed by the address lines in response to the toggling of the MWT/ line by the Multibus interface.

2.2.2.5 LAN Interface Adapter Board. The LAN interface adapter board provides the circuitry to connect the LAN cable assembly to the iSBC 88/45 board. P1 of the LAN cable assembly attaches to J1 of LAN interface adapter board. P1 of the LAN interface adapter board attaches to J1 of the iSBC 88/45 board. The signals travel on the LAN interface adapter board from the pins of J1 to the pins of P1 as follows:

J1	P1
1	9
2	12
3	13
4	16
5	14
6	1
7	5
8	8
9	3
10	6

2.2.3 Front Panel Assembly

The human interface to any of the three FDIO control cabinets is the front panel assembly which consists of the following units:

1. Front panel interface board

2. Front panel control board

3. LCD module

2.2.3.1 Front Panel Interface Board. (Figure 11-9): The front panel interface board provides the interface between the Intel iSBC 88/45 CPU board and the boards of the front panel assembly. The front panel interface board connects directly to the Intel iSBC 88/45 via an Intel iSBC connector. A ribbon cable carries signals between the front panel interface board and the front panel control board. It also contains the EEPROM that holds configuration data for various FDIO control cabinets and the error messages from the System Error Logger (SEL) task.

The front panel interface board consists of the following:

1. Clock divider

2. Address decoder

3. Keypad switch interface

4. LCD and EEPROM interface

5. EEPROM

2.2.3.1.1 Clock Divider. (Figure 11-9 1): This circuit uses two flip-flops (U1) to divide the Intel iSBC 88/45 9.83 MHz clock by four to produce a 2.46 MHz square wave clock required for the keypad interface (U3).

2.2.3.1.2 Address Decoder. (Figure 11-9 2): The address decoder (U2) for the front panel interface board is enabled when the MCS0/ line is low. The outputs of the decoder depend on the status of the MA2 signal. When the MA2 signal is high, the keyboard interface control chip, U3, is selected for input or output of control or data. When the MA2 signal is low, U4, the LCD and EEPROM interface, is selected for input or output of control or data.

2.2.3.1.3 Keypad Switch Interface. (Figure 11-9 3): The keypad switch interface, U3, is enabled by the KPEN/ signal from the address decoder. The internal registers are selected by the MA0 signal from the Intel iSBC 88/45 interface.

The outputs, SL0 through SL3, select the key row to be monitored and scan the rows of the keypad one at a time. The inputs, RL0 through RL7, contain the column data for the row selected by the outputs.

MINTRO is used as an interrupt to inform the Intel iSBC 88/45 that a pressed key has been recognized by the keypad switch interface. If two keys are depressed at the same time, the keypad switch interface performs 2-key lockout to ignore the keypad.

2.2.3.1.4 LCD and EEPROM Interface. (Figure 11-9 4): The LCD and EEPROM interface (U4) is enabled by signal DREN/ from the address decoder. Internal registers are selected by signals MA0 and MA1 from the iSBC 88/45 interface.

Data or command information is transferred to U4 when the IOWRT/ line is strobed low and the chip is selected. Data or status is transferred from U4 when the IORD/ signal is strobed low and the chip is selected.

There are three output sections to the LCD and EEPROM interface controller chip. These ports, A, B, and C, are eight bits wide and are described in the following chart:

PORT	BIT	FUNCTION
A	7	EEPROM address bit 7 and LCD data bit 7
	6	EEPROM address bit 6 and LCD data bit 6
	5	EEPROM address bit 5 and LCD data bit 5
	4	EEPROM address bit 4 and LCD data bit 4
	3	EEPROM address bit 3 and LCD data bit 3
	2	EEPROM address bit 2 and LCD data bit 2
	1	EEPROM address bit 1 and LCD data bit 1
	0	EEPROM address bit 0 and LCD data bit 0
B	7-3	Not used.
	2	EEPROM address bit 10
	1	EEPROM address bit 9
	0	EEPROM address bit 8
C	7-5	Not used.
	4	BUSY/ or READY status from the EEPROM
	3	Sonalert ON/ or OFF control signal
	2	DEN signal to LCD display module
	1	DRW signal to LCD display module
	0	DRS signal to LCD display module

2.2.3.1.5 EEPROM. (Figure 11-9 (5)): The EEPROM electrically is a cross between a Programmable Read Only Memory (PROM) and RAM. While the system is powered up, data may be read from or written into the EEPROM in the same manner as RAM. When the unit is powered OFF, the EEPROM retains the last data written into it, in a manner identical to a PROM.

When the MCS1/ signal is low, the EEPROM is selected for input or output at the address presented by the EEPROM interface. Data to be stored in the EEPROM is placed on the data bus (MD0 through MD7), and the IOWRT/ signal is strobed low. Data to be read from the EEPROM is placed on the data bus (MD0 through MD7) when the IORD/ signal is low.

The RDY signal (EEPROM pin 1) is high when the EEPROM has set up the internal address, and the signal is low when the internal address is in transition from one address to another.

2.2.3.2 Front Panel Control Board. (Figure 2-12): The front panel control board consists of the following:

1. LCD interconnectandcontrast control

2. Sonalert interface

3. Keypad control circuitry

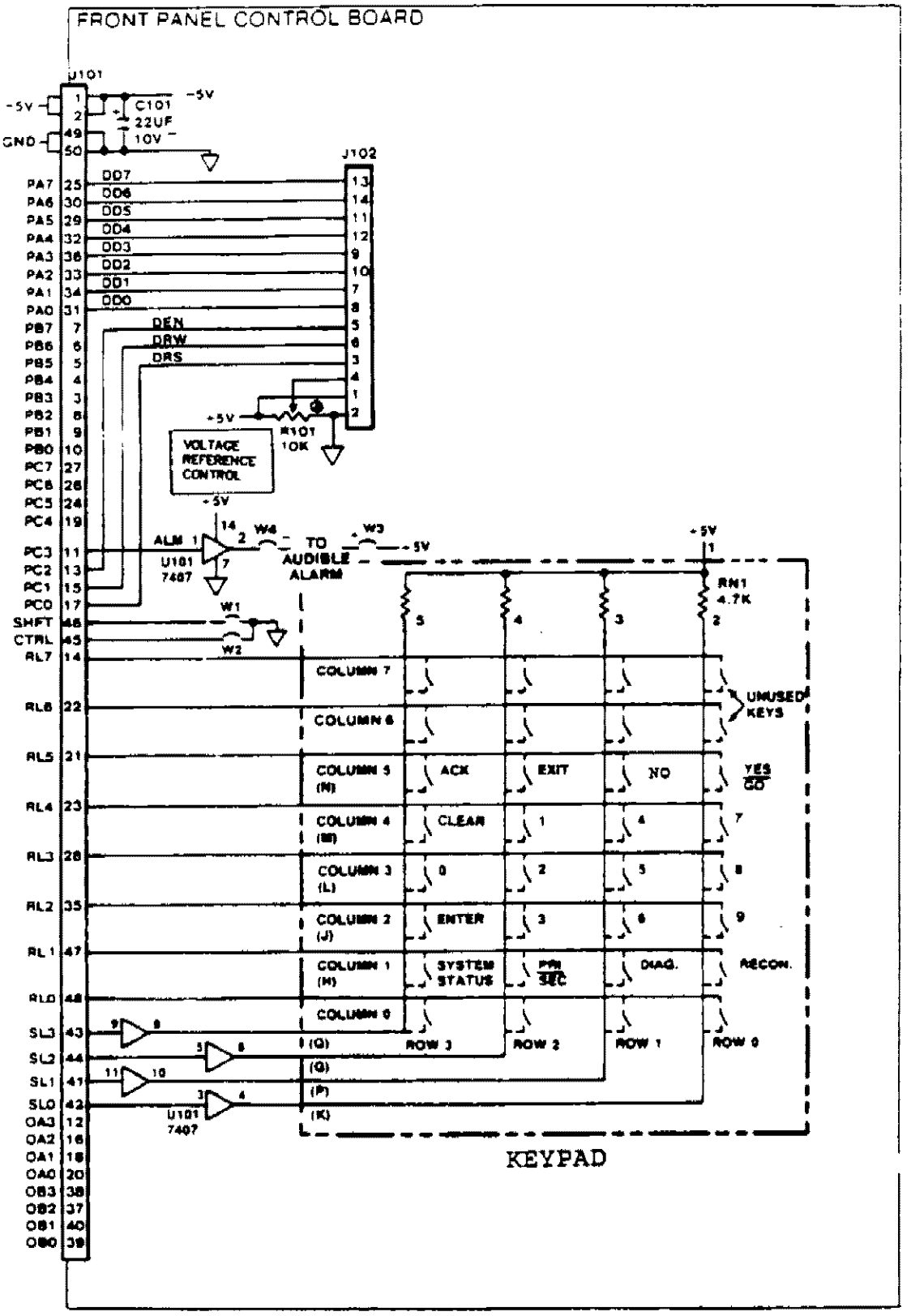


FIGURE 2-12. FRONT PANEL CONTROL BOARD BLOCKED SCHEMATIC

2.2.3.2.1 LCD Interconnect and Vage Reference Control. The front panel control board is a cable interconnect for the cables used to supply data and power from the front panel interface board (50-pin cable) to the LCD display module (14-pin cable). In addition, the Vage reference control (R101) for the LCD module is located on the front panel control board.

2.2.3.2.2 Sonalert Interface. The sonalert interface on the front panel control board consists of pins 1 and 2 of U101. The gate buffers the sonalert ON/ or OFF signal (PC3) from the front panel interface board. When the output of the gate is low, the sonalert sounds. When the output of the gate is high, the sonalert is silenced.

2.2.3.2.3 Keypad Control Circuitry. Four gates from U101 buffer the row select lines from the front panel interface board. When a given select line is low, the row of switches controlled by this select line places its data on column information lines RL0 through RL7.

When a switch is closed and the row is not selected, the output of the column data contains only the data of the selected row, and this switch is ignored. When a switch is closed and the row is selected, the output of the column data bit for this switch is low. An open switch on a selected row presents a high signal to the column data.

2.2.3.3 LCD Display Module. The LCD display module communicates with the front panel interface via the front panel control board using eight data lines (DD0 through DD7) and three control lines (DEN, DRW, and DRS).

2.2.3.3.1 LCD Data Bus. The eight data lines of the data bus (DD0 through DD7) are bidirectional. They receive the eight bit parallel data from the front panel interface for the character to be displayed or the command to be performed. The data lines also transmit the current cursor position and status to the front panel interface.

2.2.3.3.2 DEN Line. This line is the data strobe for data transmissions across the data bus. When data is written to the LCD display module from the front panel interface, this line must be low and the data placed on the data bus before the line is strobed high and returned low awaiting the next byte. When data is read from the LCD display module, this line must be low and strobed high, the data transferred, and the line returned low awaiting the next byte.

2.2.3.3.3 DRS Line. The DRS line, when low, indicates that command or status information is being transferred on the data bus. The DRS line, when high, indicates that data is being transferred on the data bus.

2.2.3.3.4 DRW Line. This line controls the direction of the data bus. When the DRW line is low, the data on the data bus is being read from the LCD display module. When the DRW line is high, data on the data bus is being written to the LCD display module.

2.2.4 LAN Assembly

2.2.4.1 BC Backplane. The BC backplane PCB is the hardware interface for the BCs to the iSBC 88/45 LAN. BC PCBs can be added or removed from the FDIO system configuration at any time without having to turn OFF power to the entire control unit.

The BC backplane consists of five sections as shown in figure 2-13, and also in figures 11-10 and 11-11 (Sheets 1 through 4).

1. Power supply connections
2. LED indicators

3. BC interface
4. LAN input
5. LAN output

2.2.4.1.1 Power Supply Connections. (Figure 11-11, Sheet 1 (1)): Each BC backplane is configured with two complete LAN and power supply connections allowing them to operate in either a remote cabinet with a single LAN and power supply, or a central cabinet with a redundant LAN and power supply. Only one power supply connection will be discussed. The applicable redundant connector is in parentheses.

A CCU has two ac power distribution sources, and two dc power supply assemblies for each BC backplane. In order to provide redundancy, one dc power supply is attached to one ac distribution source, and the second dc power supply is attached to the other ac power distribution source. Each dc power supply assembly consists of one +5 V and one ±12 V power supply.

A PCU has two ac power distribution sources, and two dc power supply assemblies for each BC backplane. In order to provide redundancy, one dc power supply is attached to one ac distribution source, and the second dc power supply is attached to the other ac power distribution source. Each dc power supply assembly consists of one +5 V power supply.

An RCU has one ac power distribution source, and one +5 V dc power supply assembly for each BC backplane.

The power supply connection for the BC backplane is P21 (P22).

2.2.4.1.1.1 +5 V Distribution. The +5 V supply enters the BC backplane via P21 at pins 3, 4, 5 and 6 (P22 at pins 3, 4, 5 and 6). From P21, power is distributed to all 16 BC PCB jacks at pins 1 and 2 (P22 at pins 11 and 12) for use by the BCs, the +5 V LED indicator, I1 (I6), and to steering diode, CR1 (CR2).

The LED indicators are illuminated when power is applied to the BC backplane. The steering diodes allow both the primary and secondary power supplies to provide power to the BC backplane, without using specially designed circuitry.

2.2.4.1.1.2 +12 V Distribution. The +12 V supply is required for use by BCs in a CCU to operate the RS-232 line drivers and receivers.

The +12 V supply enters the BC backplane via P21 at pin 2 (P22 at pin 2). From P21 it goes to a steering diode, CR3 (CR4), and to the +12 V LED indicator, I2 (I7).

The steering diodes allow both the primary and secondary power supplies to provide power to the BC backplane, without using specially designed circuitry. The LEDs are illuminated when power is applied to the BC backplane.

2.2.4.1.1.3 -12 V Distribution. The -12 V supply is required for use by BCs in a CCU to operate the RS-232 line drivers and receivers.

The -12 V supply enters the BC backplane via P21 at pin 1 (P22 at pin 1). From P21 it goes to a steering diode, CR5 (CR6), and to the -12 V LED indicator, I3 (I8).

The steering diodes allow both the primary and secondary power supplies to provide power to the BC backplane, without using specially designed circuitry. The LEDs are illuminated when power is applied to the BC backplane.

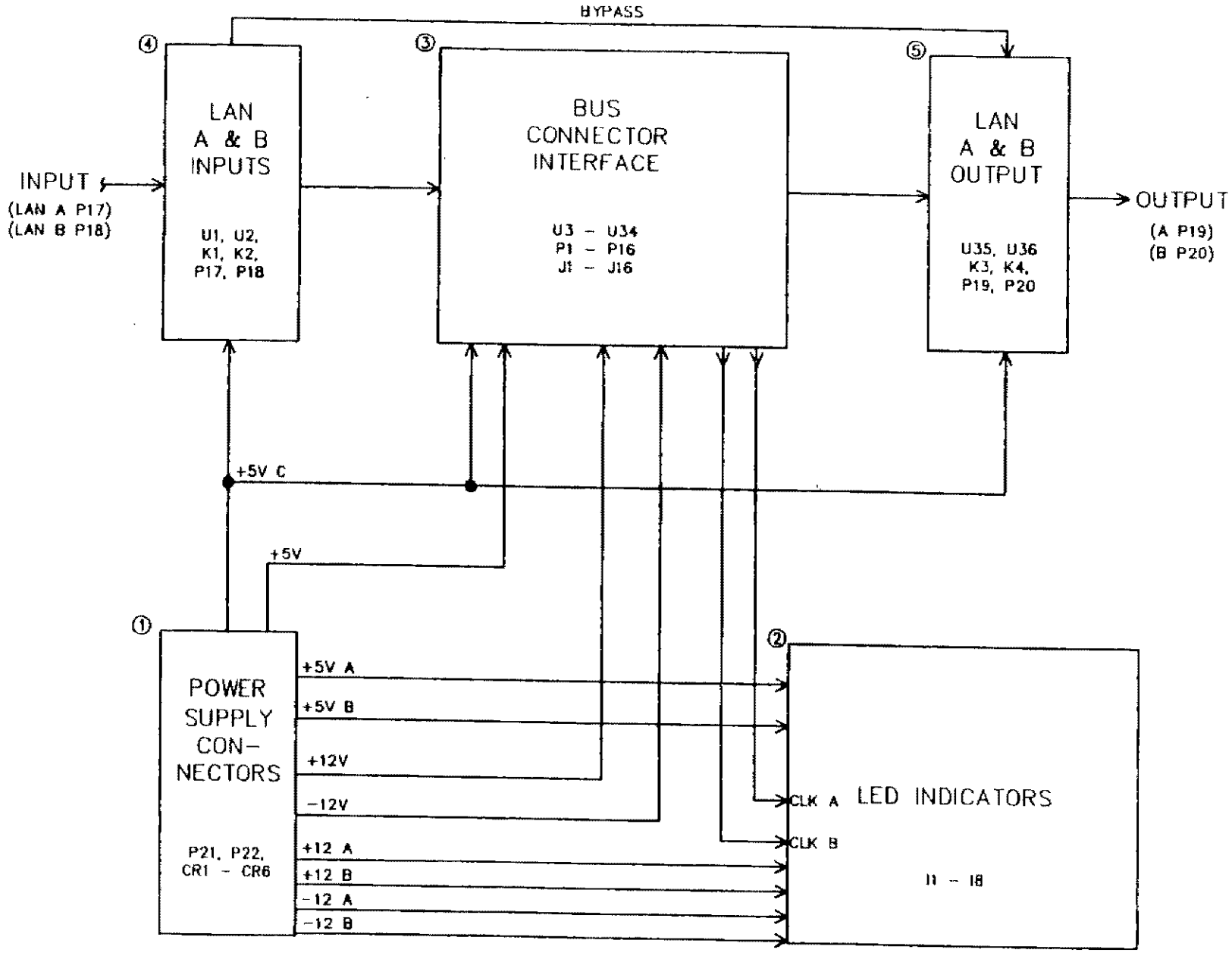


FIGURE 2-13. BC BACKPLANE BLOCK DIAGRAM

2.2.4.1.2 LED Indicators. (Figure 11-11, Sheets 1 and 2 (2)): on each BC backplane there are eight LED indicators. The power supply LED indicators are illuminated when power is supplied to the BC backplane. Clock A and B indicators are illuminated when any BC detects the presence of the associated clock. From left to right these LEDs are:

O	O	O	O	O	O	O	O
+5 V	+12 V	-12 V	CLK	CLK	+5 V	+12 V	-12 V
A	A	A	A	B	B	B	B

NOTE

Both LAN LEDs will be illuminated when a BC installed into the BC backplane is turned OFF. To correctly determine the information from the LAN LEDs, it is necessary to remove all unpowered BCs from the BC backplane to eliminate any leakage current from the BCs that are OFF.

2.2.4.1.3 BC Interface. (Figure 11-11, Sheets 2, 3, and 4 (3)): The BC interface consists of 16 Berg sockets arranged in a 2x17 matrix. It is through this interface that the BC, attached to the peripheral or modem interface plugs P1 through P16, receives power, the LAN clock, and data.

There are two LANs on each BC backplane PCB, LAN A, and LAN B. Each LAN is a synchronous RS-422 serial communications link containing the data transfer clock and data.

2.2.4.1.3.1 LAN A Clock and Data. Signals from LAN A enter the BC interface at pin 3 (LAN data) and pin 5 (LAN clock). These signals go directly to the multiplexer (U4, U6,...,U34). The LAN is delayed by one bit cell time, and buffered by each active BC it passes through. The signals exit the BC at pin 4 (LAN data) and pin 6 (LAN clock).

If a BC is installed in the BC backplane and power is ON, the multiplexer control signal on pin 7 will be low. The LAN data and LAN clock signals will enter the BC at its jack to be buffered. A one bit cell time delay occurs before the signals are passed to the next BC by the multiplexer.

If a BC is not installed into the BC backplane, or power is not ON, the multiplexer control signal on pin 7 will be high. The LAN data and LAN clock signals will bypass this BC jack and proceed to the next BC with no delay.

2.2.4.1.3.2 LAN B Clock and Data. Signals from LAN B enter the BC interface at pin 14 (LAN data) and pin 16 (LAN clock). These signals go directly to the multiplexer (U3, U5 ... U33). The LAN is delayed by one bit cell time, and buffered by each active BC it passes through. The signals exit the BC at pin 15 (LAN data) and pin 17 (LAN clock).

If a BC is installed in the BC backplane and power is on, the multiplexer control signal on pin 18 will be low.

The LAN data and LAN clock signals will enter the BC at its jack to be buffered. A delay occurs before the signals are passed to the next BC by the multiplexer. If a BC is not installed into the BC backplane, or power is not on, the multiplexer control signal on pin 18 will be high. The LAN data and LAN clock signals will bypass this BC jack and proceed to the next BC with no delay.

2.2.4.1.3.3 BC Peripheral Interface. The BC peripheral interface to the BC backplane consists of a DB9 jack, and BC interface pins 25 through 33.

In a CCU the peripheral is a modem using an RS-232 synchronous serial interface. The signals for this interface are generated by the BC and are routed to the interface connections for each peripheral interface jack described below:

Signal Name	BC Interface Pin	Peripheral Interface Pin
Modem Receive Data (MRX)	25	1
Modem Receive Clock (MRC)	27	2
Modem Transmit Data (MTX)	29	3
Modem Transmit Clock (MTC)	31	4
Ground	33	5

In a PCU the peripheral is an RFSP, and in an RCU the peripheral can be an RFSP, a CRT, or a RANK. The BC peripheral interface for both the PCU and the RCU is an RS-422 serial interface. The signals for this interface are generated by the BC and are routed to the interface connections for each peripheral interface jack described below:

Signal Name	BC Interface Pin	Peripheral Interface Pin
Peripheral Transmit Data Negative (PTXN)	30	8
Peripheral Transmit Data Positive (PTXP)	32	9
Peripheral Receive Data Negative (PRXN)	26	6
Peripheral Receive Data Positive (PRXP)	28	7
Ground	33	5

2.2.4.1.4 LAN A and B Inputs. (Figure 11-11, Sheet 2 (4)): Each LAN has its own input connector to the BC backplane. LAN A input connector is P17 and LAN B input connector is P18.

2.2.4.1.4.1 LAN A Input. The RS-422 clock and data signals for LAN A are input to the BC backplane via the P17 connector. From P17 the signals enter a miniature reed relay, K1.

Relay K1 is one of two LAN A bypass relays (K1 or K3). When power is removed from the BC backplane, K1 and K3 open, and the LAN signals bypass the entire BC backplane. This allows the rest of the control unit to operate if the power supply to a BC backplane is disabled. When power is applied to the BC backplane, K1 and K3 close, and the LAN A signals are sent to the LAN terminator adapter at U2.

U2 terminates and converts each of the double-ended RS-422 serial data and clock signals to a single ended signal which is sent to the first BC jack and multiplexer described in paragraph 2.2.4.1.3.3.

2.2.4.1.4.2 LAN B Input. The RS-422 clock and data signals for LAN B are input to the BC backplane via the P18 connector. From P18 the the signals enter a miniature reed relay, K2.

Relay K2 is one of two LAN B bypass relays (K2 or K4). When power is removed from the BC backplane, K2 and K4 open, and the LAN signals bypass the entire BC backplane. This allows the rest of the control unit to operate if the power supply to a BC backplane is disabled. When power is applied to the BC backplane, K2 and K4 close, and the LAN B signals are sent to the LAN terminator adapter at U1.

U1 terminates and converts each of the double-ended RS-422 serial data and clock signals to a single ended signal, which is sent to the first BC jack and multiplexer described in paragraph 2.2.4.1.3.3.

2.2.4.1.5 LAN A and B Outputs. (Figure 11-11, Sheet 4 (5)): Each LAN has its own output connector to the BC backplane. LAN A output connector is P19 and LAN B output connector is P20.

2.2.4.1.5.1 LAN A Output. LAN A output circuitry consists of U35, K3, and P19. U35 converts the single-ended LAN data and clock signals into double-ended RS-422 signals. These signals are passed to the LAN A output bypass reed relay, K3. Relay K3 in conjunction with relay K1, allow the LAN A data and clock lines to bypass the BC backplane if the power supply is disabled. When K1 and K3 are open, the LAN A signals are passed from the LAN A input bypass relay (K1) to the LAN A output bypass relay (K3), and then output at P19. When K1 and K3 are closed, the LAN A signals from the output of U35 are sent to P19 via the LAN A output bypass reed relay, K3.

2.2.4.1.5.2 LAN B Output. LAN B output circuitry consists of U36, K4, and P20. U36 converts the single-ended LAN data and clock signals into double-ended RS-422 signals. These signals are passed to the LAN B output bypass reed relay, K4. Relay K4 in conjunction with relay K2, allow the LAN B data and clock lines to bypass the BC backplane if the power supply is disabled. When K2 and K4 are open, the LAN B signals are passed from the LAN B input bypass relay (K2) to the LAN B output bypass relay (K4), and then output at P20. When K2 and K4 are closed, the LAN B signals from the output of U36 are sent to P20 via the LAN B output bypass reed relay, K4.

2.2.4.2 BC. The BC is a stand-alone microcomputer system which provides the interface between a peripheral device and the Multibus assembly.

The BC has the following three modes of operation:

1. ignored (BC address = 0)
2. operational with a peripheral (BC address range depends on control unit type)
3. maintenance channel (address is unit dependent)

These modes of operation are described in the paragraphs 2.2.4.2.1 through 2.2.4.2.3.

2.2.4.2.1 Ignored Operation. Even though a BC is powered up and is ready, the LAN A and LAN B LEDs are not illuminated, and the BC cannot communicate with the control unit.

2.2.4.2.2 Normal Operation. The BC interfaces between its peripheral and its control unit.

2.2.4.2.3 Maintenance Channel. Any BC can be used as a maintenance channel. Usage as a maintenance channel depends on the control unit type (RCU and PCU) and the BC's address (21 for RCU or 29 for PCU). When powered up as a maintenance channel, and attached to an RFSP, the BC sends the RFSP front panel enable sequence to the RFSP. (The actual command sequence has been purposely left out of this document according to FAA request.) The front panel enable sequence is ignored by RFSP FA 10095/11 and RFSP FA 10095/14. Otherwise, a maintenance channel BC is identical to any other BC in the system.

Figure 2-14 illustrates the following seven major functional circuits of the BC:

1. Microcomputer
2. Expansion EPROM
3. Expansion RAM
4. Serial communications controller
5. LAN select and array logic
6. Fail-Safe counter
7. Power distribution

Figure 11-12 (Sheets 1 through 3) is a detailed schematic diagram of the BC hardware with the major functional circuits designated by a circled number. The following subparagraphs describe each functional section.

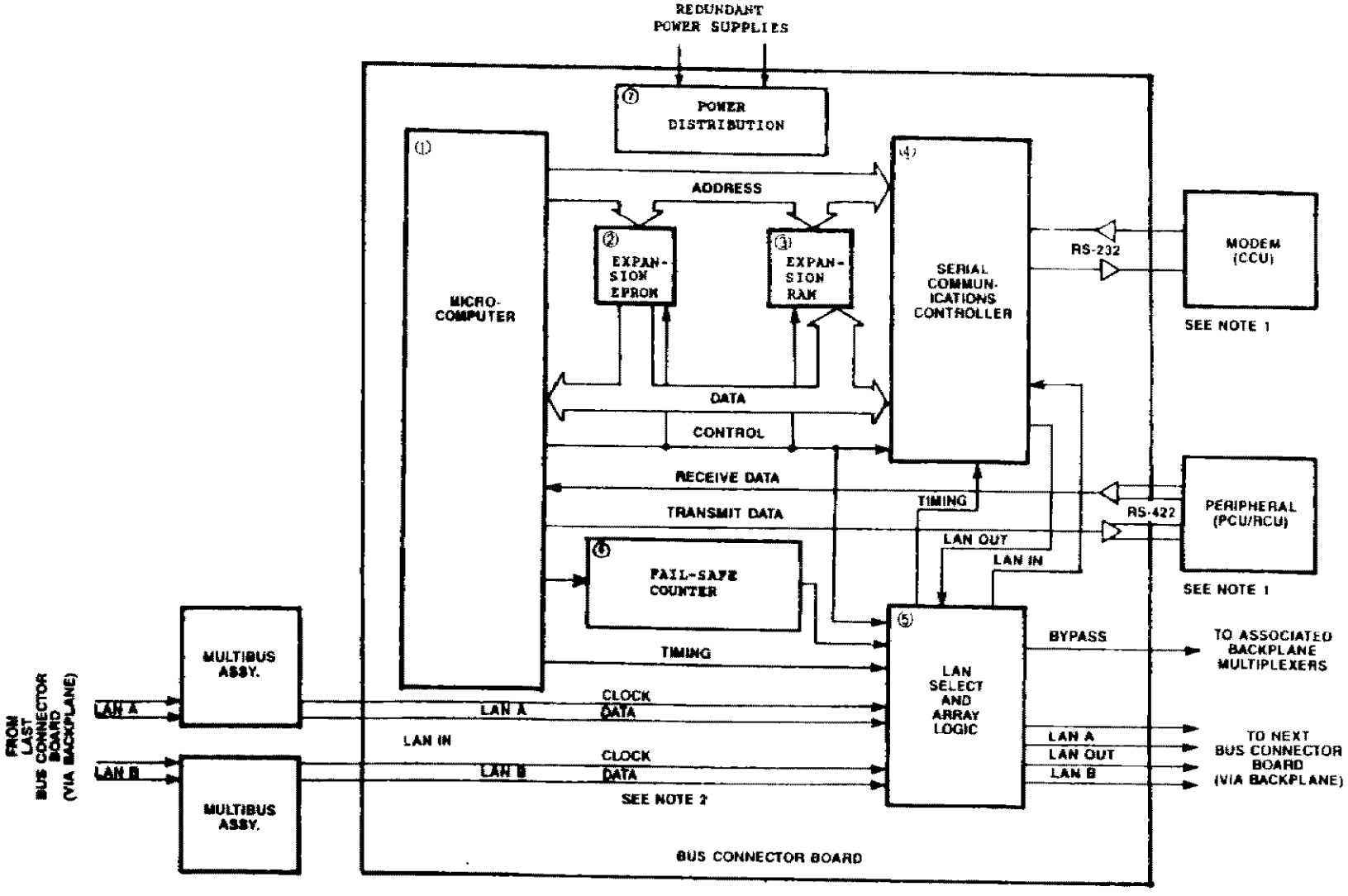
2.2.4.2.4 Microcomputer. (Figure 11-12, Sheets 2 and 3 (1)): The microcomputer contains the clock oscillator, 8031 microcomputer, address latch and LAN address switches. It fetches and executes instructions from the EPROM memory and performs other I/O and control operations.

2.2.4.2.4.1 Clock Circuit. An external 11.059 MHz oscillator (Y1) provides a square wave TTL clock. This clock, presented to the XTAL2 input of the microcomputer chip (U1), becomes the time base for all internal clocking signals. The 11.059 MHz clock is fed to the PAL device which divides the clock by 4 to produce a 2.76 MHz clock (U2). The 2.76 MHz clock is used by the SCC for internal timing. Jumper E1 disconnects the oscillator from the rest of the circuit allowing injection of an external clock source during testing.

2.2.4.2.4.2 8031 Microcomputer. The 8031 microcomputer (U1) is a functional microcomputer on a silicon chip. The microcomputer contains an 8-bit CPU, a read/write memory, a parallel I/O, two 16-bit timer/counters, a full-duplex serial port, and a five-source interrupt structure. 128-bytes of internal RAM are partitioned into general purpose registers, special function registers, program stack, and general purpose memory for variable storage. The internal RAM is augmented by 8 Kbs of off-chip expansion RAM (U6).

The program for controlling the BC resides in 8 Kbs of EPROM external to the 8031 chip.

On power up, a reset circuit consisting of R1 and C1 guarantees that the reset input (U1 pin 9) remains active until the power supply stabilizes and the 8031 microcomputer is able to begin operation.



NOTE 1: EACH BUS CONNECTOR BOARD SUPPORTS ONE PERIPHERAL OR ONE MODEM.
NOTE 2: CCU/PCU REDUNDANT LAN SHOWN. RCU USES ONLY ONE LAN CHANNEL.

FIGURE 2-14. BC MAJOR FUNCTION DIAGRAM

The 8031 contains four 8-bit bidirectional I/O ports, P0 through P3, which perform the following functions:

Port 0: This port is used during the process of accessing expansion memory (RAM or EPROM). The port alternately contains actual data or the lower eight bits of the 16-bit external address. The actual data has been read from RAM, EPROM, or the SCC, or the actual data is to be written to RAM or the SCC. The address latch, U3, is used to latch the lower eight address lines (AD0 through AD7) emanating from port 0 of the 8031.

Port 1: The lower seven bits of port 1 are configured as inputs and are connected to the seven-position DIP switch (S2). S2 contains the LAN address. Bit 8 of port 1 is the output signal, LANEN/. LANEN/, when active (low), the BC is connected to the LAN bus.

Port 2: Port 2 contains the upper eight bits of the 16-bit address when accessing expansion RAM, EPROM, or SCC.

Port 3: Port 3 is configured as a special function port. Each bit position performs the following special function:

MSB LSB

7	6	5	4	3	2	1	0

Bit	Description
0	RxD: Data received by the internal serial port from the RANK, CRT, or RFSP.
1	TxD: Serial data transmitted by the internal serial port to the RANK, CRT, or RFSP.
2	INT0/: External interrupt generated by the SCC due to a LAN, or modem character interrupt.
3	RESET/: Output signal used to reset the LAN clock detection logic.
4	TEST: Output signal that places the LAN select logic into loop back mode.
5	TRST/: Output signal that resets the fail-safe timer.
6	WR/: Output signal that is the external data memory write strobe.
7	RD/: Output signal that is the external data memory read strobe.

The 8031 contains an asynchronous interface for communicating with a RANK, CRT, or RFSP. An internal baud rate generator provides the 2400 Hz clock. The serial input signals from the peripheral device enter the BC from the BC backplane via P1 (PTXP and PTXN) and are converted from RS-422 to TTL by receiver chip U11. The converted signals enter the RxD input (port 3 bit 0) of the 8031. Serial output data to the peripheral device exits the 8031 microcomputer via the TxD output pin (port 3 bit 1). The data is then routed to driver chip U12 where the serial TTL signal is converted to RS-422. The RS-422 output signals (PRXP and PRXN) exit the BC via P1 to the BC backplane and then to the peripheral device.

2.2.4.2.4.3 LAN Address Switches. The BC LAN address is encoded in the 7-bit DIP switch (S2) for 128 possible LAN (or BC) addresses. The individual switch elements are connected to the

lower seven bits of port 1 and are pulled to a nominal TTL high logic level by the pull-up resistor (RN1). If the switch is closed, the logic level is forced to a TTL low level. Table 2-21 lists the switch settings necessary to configure the BC for addresses 1 through 29 as required for FDIO operation.

TABLE 2-21. LAN ADDRESS SWITCH SETTINGS

C = closed O = open
(ON = "0") (OFF = "1")

BC Card Cage Slot	Recommended BC Address(decimal/hex)	BC Address Switches						
		1	2	3	4	5	6	7
upper cardcage 1	1 / 01	O	O	C	C	C	C	O
2	2 / 02	O	O	C	C	C	O	C
3	3 / 03	O	O	C	C	C	O	O
4	4 / 04	O	O	C	C	O	C	C
5	5 / 05	O	O	C	C	O	C	O
6	6 / 06	O	O	C	C	O	O	C
7	7 / 07	O	O	C	C	O	O	O
8	8 / 08	O	O	C	O	C	C	C
9	9 / 09	O	O	C	O	C	C	O
10	10 / 0A	O	O	C	O	C	O	C
11	11 / 0B	O	O	C	O	C	O	O
12	12 / 0C	O	O	C	O	O	C	C
13	13 / 0D	O	O	C	O	O	C	O
14	14 / 0E	O	O	C	O	O	O	C
15	15 / 0F	O	O	C	O	O	O	O
16	16 / 10	O	O	O	C	C	C	C

TABLE 2-21. LAN ADDRESS SWITCH SETTINGS (Continued)

BC Card Cage Slot	Recommended BC Address(decimal/hex)	BC Address Switches						
		1	2	3	4	5	6	7
MSB	1 2 3 4 5 6 7 O N Dip Switch							LSB
lower cardcage 1	17 / 11	O	O	O	C	C	C	O
2	18 / 12	O	O	O	C	C	O	C
3	19 / 13	O	O	O	C	C	O	O
4	20 / 14	O	O	O	C	O	C	C
5	21 / 15	O	O	O	C	O	C	O
6	22 / 16	O	O	O	C	O	O	C
7	23 / 17	O	O	O	C	O	O	O
8	24 / 18	O	O	O	O	C	C	C
9	25 / 19	O	O	O	O	C	C	O
10	26 / 1A	O	O	O	O	C	O	C
11	27 / 1B	O	O	O	O	C	O	O
12	28 / 1C	O	O	O	O	O	C	C
13	29 / 1D	O	O	O	O	O	C	O

2.2.4.2.5 Expansion EPROM. (Figure 11-12, Sheet 2 (2)): The 8031 microcomputer fetches and executes program instructions from off-chip expansion program memory EPROM. Although the 8031 microcomputer can address up to 64 Kbs of program memory, the BC contains a 28-pin socket (U4) that can accommodate a 2764 (8 Kbs) EPROM or a 27128 (16 Kbs) EPROM. In order to access all locations, the 8 Kb EPROM requires 13 address lines, and the 16 Kb EPROM requires 14 address lines. When the 16 Kb capability is to be used, jumper E2 connects the highest address line (pin 26 of U4) to address line A13; otherwise, jumper E3 connects pin 26 of U4 to a logical high via pullup resistor RN2.

See the EPROM read cycle timing in figure 2-15, for a graphic depiction of the following description of an EPROM read cycle. The 8031 microcomputer uses ports 0 and 2 to access off-chip memory. During the first part of the read cycle, the lower eight bits of the address are output on port 0, and the upper eight bits are output on port 2. When the address lines are stable, the 8031 causes signal ALE to change from high to low. This causes the lower eight address bits from port 0 to be latched by transparent latch U3. The upper address bits do not require external latching, since the 8031 keeps them stable throughout the read operation.

The latched addresses are presented to the EPROM to select the desired location. When the required address setup time delay has elapsed, the 8031 causes signal PSEN/ to go active low. This connects the contents of the selected EPROM location to the port 0 lines. These lines have since become inputs. The 8031 reads the contents of the EPROM via port 0. When the operation is complete, PSEN/ is de-activated to disable the output of the EPROM, and a new memory address is setup on ports 0 and 2.

2.2.4.2.6 Expansion RAM. (Figure 11-12, Sheet 2 (3)): Although the 8031 microcomputer can address up to 64 Kbs of expansion RAM, the BC contains a single byte-wide 8 Kb RAM (U6). See the RAM Read/Write Operations Timing diagram, figure 2-15, for a graphic depiction of the following descriptions.

In order to access off-chip RAM, the 8031 microcomputer uses ports 0 and 2. During the first part of the read/write cycle, the lower eight bits of the address are output on port 0, and the upper eight bits are output on port 2. When the address lines are stable, the 8031 causes signal ALE to change from high to low. This causes the lower eight address bits from port 0 to be latched by transparent latch U3. The upper address bits do not require external latching, since the 8031 keeps them stable throughout the read/write operation.

Latched address bits A0 through A12 are presented to the RAM to select the desired location, and address bits A13 through A15 are decoded by the select logic contained in the PAL (U2). PAL output RAMEN/ is active low when input lines A13, A14, and A15 are each a logical low. This is shown in the following Boolean equation:

$$\text{RAMEN/} = \overline{\overline{A13} \text{ AND } \overline{A14} \text{ AND } \overline{A15}}$$

When a read/write request is made of the lower 8 Kbs of RAM, A13 through A15 are low. This activates RAMEN/ which is connected to the chip select input of the RAM (U6 pin 20).

If a RAM read operation is to be performed, the 8031 microcomputer causes signal RD/ to go active (low) after the required address and chip select setup delays have elapsed. This connects the contents of the selected RAM location to the port 0 lines which have become inputs. The 8031 reads the contents of the RAM via port 0. When the operation is complete, RD/ is de-activated to disable the output of the RAM.

When a RAM write operation is performed, the 8031 outputs the data to be written into RAM to port 0. After the required address data and chip select setup delays have elapsed, the 8031 strobes WR/ low. This causes the contents of port 0 to be written into the selected RAM location.

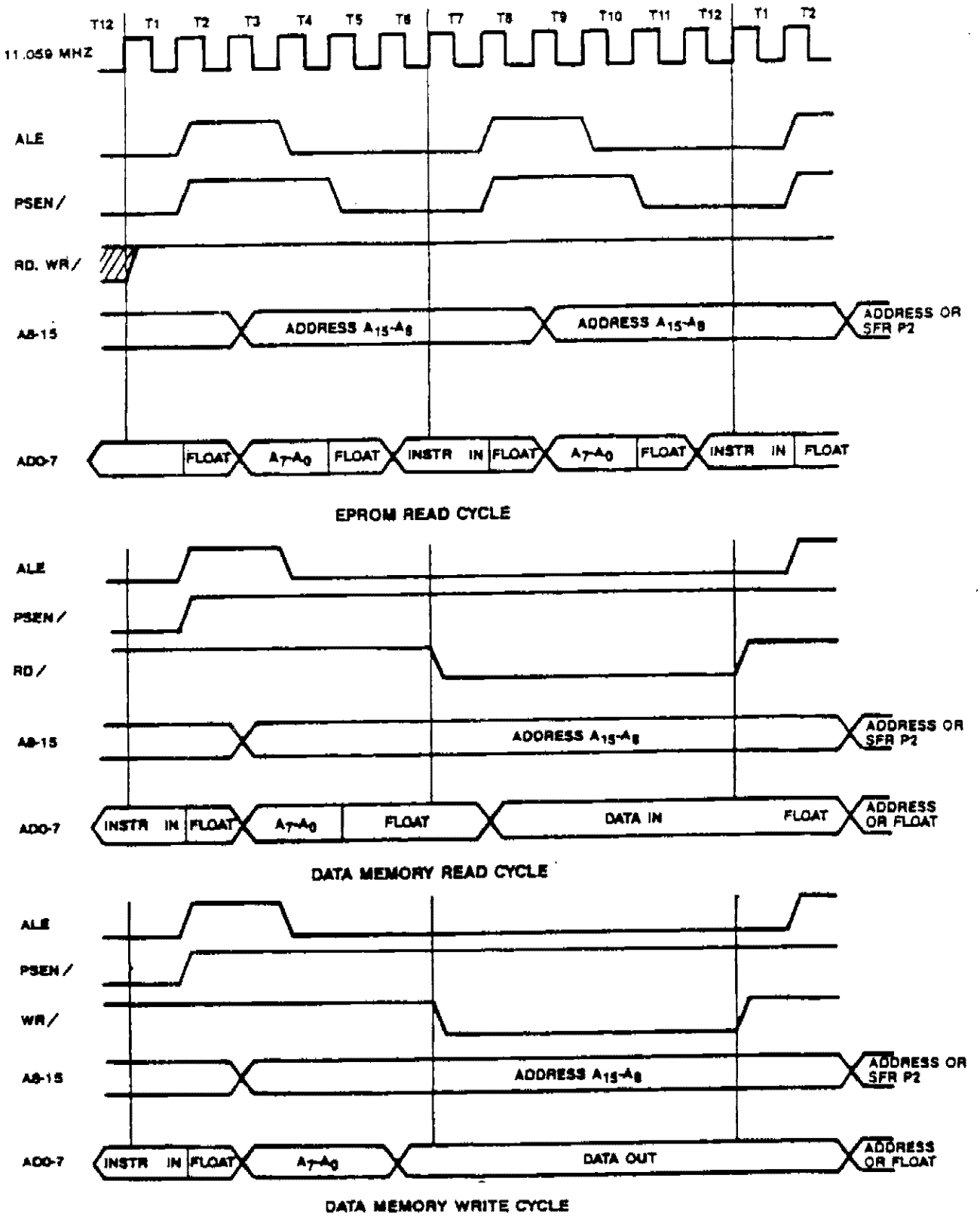


FIGURE 2-15. MICROCOMPUTER TIMING DIAGRAM

2.2.4.2.7 SCC. (Figure 11-12, Sheets 2 and 3 (4)): The SCC circuit consists of an 82530 (U5) containing two separate serial channels. Channel A is used for communication with the LAN and channel B for communication with a modem. This circuit contains separate RS-232 drivers and receivers for the modem interface.

The SCC is controlled by the 8031 microcomputer in the same way external RAM is accessed. The SCC is a MMIO device which the processor views as a range of memory locations. Commands and data are sent to the SCC by performing an external memory write to the desired location; status and data are read from the SCC by performing an external memory read from the desired location. The MMIO addresses are as follows:

Address (hex)	SCC Port Selected
A000	Modem command/status port
A001	Modem data port
A002	LAN command/status port
A003	LAN data port

The read/write operational sequence is the same as the one described for expansion RAM operation except that the SCC requires address bits A0 and A1, and the chip select is enabled by signal COMEN/.

Latched address bits A0 and A1 are presented to the SCC for selection of the desired port (LAN, modem, command/status, or data), and address bits A13 through A15 are decoded by the select logic contained within the PAL (U2). PAL output COMEN/ is active low when input lines A13, A14, and A15 are at logic one, zero and one, respectively. This is shown in the following Boolean equation:

$$\text{COMEN/} = \overline{\overline{A13} \text{ AND } \overline{A14} \text{ AND } \overline{A15}}$$

When a read/write request is made within the address range A000 through BFFF (hex), COMEN/ is activated enabling the SCC for I/O operations via its chip select line (pin 33).

When a read operation of the SCC is performed, the 8031 microcomputer causes signal RD/ to go active (low) after the required address and chip select setup delays have elapsed. This connects the status or data register to port 0 lines. These lines have since become inputs. The 8031 then reads the information via port 0. When the operation is complete, RD/ is de-activated to disable the output of the SCC.

When a write operation to the SCC is to be performed, the 8031 outputs the control or data byte to port 0. After the required address data and chip select setup delays have elapsed, the 8031 pulses WR/ (low). This causes the contents of port 0 to be written into the SCC.

2.2.4.2.7.1 LAN Channel. The LAN operates in synchronous mode at a 19,200 baud rate. The TTL data (RxDA) and clock (TxCA) signals are received from the iSBC 88/45 via the LAN select logic and enter the SCC at the receive data (RxDA) and receive clock (RTxCA/) pins, respectively. The LAN clock is provided by the LAN interface circuit on the iSBC 88/45 board and becomes the master LAN clock for receive and transmit operations of each BC. This is accomplished by connecting receive clock input pin RxCA to transmit clock output pin TxCA of the SCC. The transmit data (TxDA) and clock (TxCA) signals are passed to the LAN select logic where they are buffered, directed to the appropriate redundant LAN, and sent to the BC backplane via P1.

2.2.4.2.7.2 Modem Channel. The modem operates in synchronous mode at a 2400 baud rate. The modem transmit data (MTX) and clock (MTC) signals enter the BC from the BC backplane via

connector P1 (pins 29 and 31). These signals are converted from RS-232 to TTL by receiver U7, becoming RxDB and TxCB. The signals then enter the SCC at the receive data (RxDB, pin 27) and receive clock (RxCB/, pin 28), respectively. The modem clock originates at the modem and becomes the master clock for both receive and transmit operations. This is accomplished by connecting receive clock input pin RxCB/ to transmit clock output pin TxCB/ (pin 26) of the SCC. The transmitted data (TxDB, pin 23) and clock (TxCB) lines are converted to RS-232 by drivers (U13), becoming MRX (pin 25) and MRC (pin 27) for transmission to the modem via the BC backplane via P1.

2.2.4.2.8 LAN Select and Array Logic. (Figure 11-12, Sheet 3 (5)): This circuit consists of a PAL device and other supporting circuitry and performs the following five major functions:

1. Four stage binary counter
2. MMIO decode logic
3. LAN source select and access control
4. LAN loop-back operation
5. BC self-test operation

See the internal PAL logic equivalent circuit in figure 2-16 while reading the following discussions.

2.2.4.2.8.1 Four Stage Binary Counter. The PAL contains internal logic that operates as a four-stage binary counter. The PAL inputs and outputs are as follows:

Inputs	Outputs	Description
11.059 MHz		Input clock from crystal oscillator
	2.76 MHz	Output clock derived by dividing the input clock by 4, used as an input by the SCC
	TESTCLK	691 kHz output clock derived by dividing the input clock by 16, used during LAN loopback test

2.2.4.2.8.2 MMIO Decode Logic. The PAL contains logic that performs unconditional decoding of the address inputs A13, A14, and A15. The two output chip select lines are for the RAM (RAMEN/) and the SCC (COMEN/).

Inputs	Outputs	Description
A13,A14,A15		Address inputs from the 8031 microcomputer to be decoded
	RAMEN/	Output line enabling the RAM for the correct address combination of the input address lines
	COMEN/	Output line enabling the SCC for the correct address combination of the input address lines

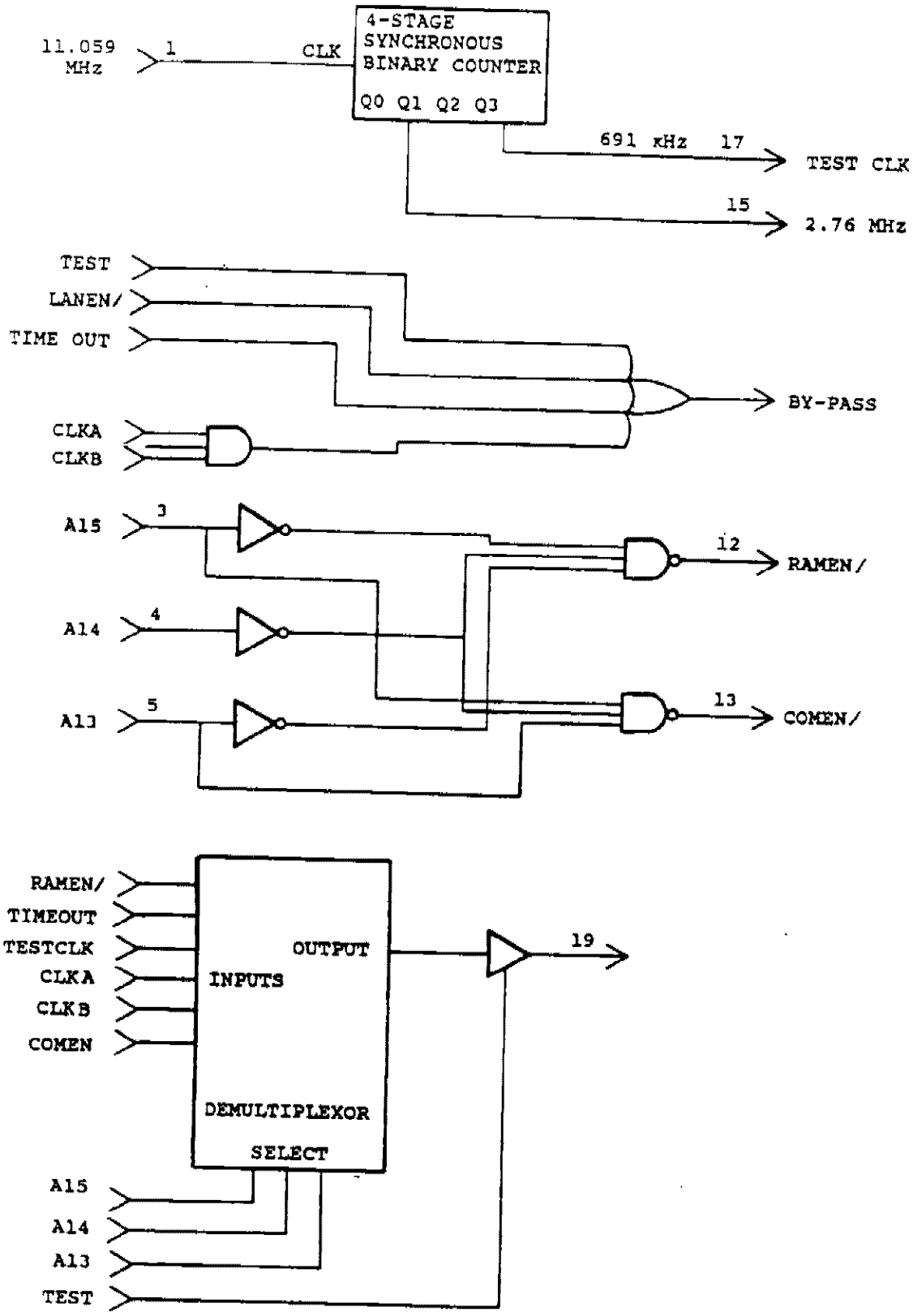


FIGURE 2-16. PAL LOGIC DIAGRAM

PAL output RAMEN/ is active low when input lines A13, A14, and A15 are a logical low. The following Boolean equation describes this:

$$\text{RAMEN/} = \overline{\overline{A13} \text{ AND } \overline{A14} \text{ AND } \overline{A15}}$$

PAL output COMEN/ is active low when input lines A13, A14, and A15 are at logic one, zero, and one, respectively. The following Boolean equation describes this:

$$\text{COMEN/} = \overline{\overline{A13} \text{ AND } \overline{A14} \text{ AND } \overline{A15}}$$

2.2.4.2.8.3 LAN Source Select and Access Control. This circuit determines which one of two LAN buses is the active LAN and connects that LAN bus to the SCC. The LAN clock detect circuit consists of the dual mono-stable multivibrator circuits (U9). Only the LAN bus of the primary control unit will be operational and contain an active clock. The output of the LAN clock detect circuit selects the LAN bus to be connected to the SCC via demultiplexors U4 and U8. The active LAN information goes to the PAL where the decision to enable the BC onto the active LAN bus is made.

The two LAN clocks, CLOCKA and CLOCKB, enter the BC via P1. From P1 the clocks are routed to demultiplexor circuit U8 and to the **A** inputs of one of two identical LAN clock detect mono-stables (half of U9). Each mono-stable creates a positive pulse at the **Q** output when the clock signal present at the **A** input makes a logical high to low transition (the **B** input being at a logical high). The time constant of the mono-stables is defined by the attached resistor and capacitor combination (R3/C12 and R2/C11). This yields an approximate 1 MSec pulse.

The mono-stables are retriggerable since the **Q** output remains high if the **A** input continues to transition from the high to low logical state within that 1 MSec period. The **Q/** output of each mono-stable exhibits the logical inverse signal of the **Q** output and is connected to the **B** input of the other mono-stable circuit. If one of the mono-stables is constantly being retriggered (due to a constant LAN clock at its **A** input) its **Q/** output is held low. This disables the other mono-stable by causing its **B** input to be low. Any noise or signal artifact coming in on the non-active LAN is filtered out and does not confuse the LAN clock detect circuit.

The outputs of the LAN clock detect circuit are the signals CLKA and CLKB. If the CLOCKA input is active (contains a square wave equal to the baud rate), clock detect line CLKA remains at an active high logical level and line CLKB remains at an inactive low logical level. If the CLOCKB input is active, signal CLKB remains at an active high level, and line CLKA is inactive. Signals CLKA/ and CLKB/ are buffered by U8 and illuminate green clock indicators I2 and I3. I2 is on if LAN A is active, and I3 is on if LAN B is active.

An active low signal on CLKA/ or CLKB/ results in BC backplane signal CLOCKA/ or CLOCKB/ being pulled low through diode CR2 or CR4. CLOCKA/ and CLOCKB/ are common to all BCs and can be activated by any active BC on the SCLC loop (i.e., BYPASS is low). These signals illuminate indicators on the BC backplane indicating the currently active LAN.

Signal CLKB is presented to the LAN select circuit consisting of U4, U8, and U15. If the active clock is from LAN B, CLKB will be high. When signal TEST is inactive (low), output U15 pin 6 will be low, and U15 pin 11 will be high. This enables the top four buffers of U4 and disables the top four buffers of U8. B LAN data and clock signals, DATA B and CLOCK B, are connected to the SCC via RxDA and TxCA. (RxDA and TxCA refer to channel A of the dual channel SCC handling the LAN interface.) Similarly, the LAN select circuit routs the SCC transmit data (TxDA) and clock (TxCA) signals to active LAN B bus output signals DATAB and CLOCKB.

When the A LAN is active, signal CLKB is low. This connects the A LAN data and clock signals, DATA A and CLOCK A, to the SCC via RxDA and TxCA. The SCC transmit data and clock signals drive the active LAN A bus signals DATA A and CLOCKA.

Another section of the PAL is responsible for determining whether the BC may access the LAN bus. The following signals are involved in the decision process:

Inputs	Outputs	Description
CLKA		LAN A clock detect signal
CLKB		LAN B clock detect signal
LANEN/		Signal under 8031 firmware control, set when BC becomes part of SDLC loop
TEST		Signal under 8031 firmware control, set to activate self test
TIMEOUT		Output of hardware timeout circuit, goes high if system fails and a time out occurs
	BYPASS	Output signal goes inactive (low) to enable the BC onto active LAN bus and become part of SDLC loop

When PAL output BYPASS is active (high), the BC backplane ignores BC output, causing the BC to be bypassed by the SDLC loop. When inactive (low), the BC backplane connects the BC output to the input of the next BC to propagate the signal around the SDLC loop. The following boolean equation shows this:

$$\text{BYPASS} = \text{TEST OR } \overline{\text{LANEN}} \text{ OR TIMEOUT OR (CLKA AND CLKB)}$$

If the TEST or TIMEOUT signal is active, the BC is bypassed. If both LAN clocks are active, the BC is bypassed. If the above conditions are correct and the firmware enables LANEN/, the BC will exit the bypass state and become an active part of the SDLC loop.

When the BC is communicating with the LAN (BYPASS is low), green indicator I1 is illuminated.

2.2.4.2.8.4 LAN Loopback Operation. The basic LAN operation is verified by enabling the LAN loopback feature. By enabling signal TEST, the 8031 microcomputer checks the operation of the SCC LAN channel without an operational LAN.

When activated, TEST causes the PAL to activate signal BYPASS to remove the BC from the SDLC loop and avoid any contamination of loop operations. This disables the top four buffers of U4 and U8, and enables the bottom two buffers of U4. The SCC LAN channel data output (TxDA) is effectively connected to its own input (RxDA) in order to verify the transmit and receive operations of the SCC. The SCC interrupt operation is also verified in this manner.

2.2.4.2.8.5 BC Self-Test Operation. See figure 2-16 for the PAL logic diagram. The BC self-test operation. This operation is performed by the PAL (U2), and monitors some of the BC functions not directly accessible by the 8031. These functions include the outputs of two clock detectors, the Q3 output of the 4-stage binary counter, and the TIMEOUT signal. The PAL circuit permits the 8031 to monitor these internal signals during test mode by connecting pin 19 of the PAL to the signal LANEN/. When not in test mode, pin 19 is tri-stated and does not affect the operation of LANEN/. When self-test

is enabled by turning on TEST, the BC is forced into bypass mode, and one of the internal signals is enabled onto pin 19 of the PAL. Since bypass mode is forced here, the 8031 microcomputer redefines LANEN/ as an input pin and facilitates signal reading.

By selecting the proper address on A13 through A15, the state of each input is sent back to the 8031 by reading signal LANEN/. The list below shows the monitored signals and the addresses required for each.

Address	Signal Enabled Onto LANEN/
0XXX (hex)	RAMEN
2XXX (hex)	TIMEOUT
4XXX (hex)	TESTCLK
6XXX (hex)	CLKA
8XXX (hex)	CLKB
AXXX (hex)	COMEN
CXXX (hex)	None-used to reset 4-stage counter

2.2.4.2.9 Fail-Safe Counter. (Figure 11-12, Sheet 3 (6)): The fail-safe counter consists of a 14-stage Complimentary-Metal Oxide Semiconductor (CMOS) counter (U10) and select jumpers E4 through E9. The clock input is connected to the active LAN clock (TxCA) which operates at 19,200 baud. The output stages of six of the counters are routed to jumper pins, allowing the user to select the time out period as follows:

Jumper	Output Term	Time Out Period (Note)
E6	Q9	13 MSec (divide by 256)
E5	Q10	27 MSec (divide by 512)
E4	Q11	53 MSec (divide by 1024)
E9	Q12	107 MSec (divide by 2048)
E8	Q13	213 MSec (divide by 4096)
E7	Q14	427 MSec (divide by 8192)

NOTE

These times assume a LAN baud clock of 19.2K Baud.

The reset input of the fail-safe timer (U10 pin 11) is connected to signal TRST, which is controlled by the 8031 microcomputer. When TRST is brought low, the reset input is removed, and the counter begins to count. If TRST remains low, the selected time out eventually elapses, and signal TIMEOUT goes high. This forces the BC into bypass mode via the internal PAL logic. The microcomputer holds off the time out by periodically pulsing TRST high to reset the counter. The reset pulse must be issued before the time out period to prevent the time out from occurring. Typically, an internal counter or other periodic occurrence within the 8031 microcomputer or its environment will trigger the reset of the fail-safe timer. If the microcomputer fails to operate correctly, the fail-safe timer forces the BC off the LAN bus and avoids contamination of the entire LAN.

2.2.4.2.10 Power Distribution. (Figure 11-12, Sheet 1 (7)): The BC requires three voltages for proper operation: +5 V dc for the logic circuits, microcomputer, and memory, and +12 V dc for the RS-232 drivers and receivers required for the modem interface. If the BC is not part of the CCU

LAN, the +12 V dc sources are not required. These voltages are distributed to each BC through the BC backplane.

The BC backplane and BC are powered by redundant + 5 V dc power supplies. If one supply fails, the other can assume responsibility. The BC receives the two +5 V dc sources via P1, one on pins 1 and 2 and the other on pins 11 and 12. The input voltage at the P1 pins of the BC is higher than nominal, approximately +5.3 V dc. Schottky silicon diodes on the BC (CR5 and CR6) constitute a power steering circuit protected by picofuses (F1 and F2). The voltage drop across the diode is approximately .3 V and results in applying a net voltage of 5 V to power switch S1. When S1 is closed, this voltage is applied across filter capacitor C2 and to the logic circuits.

If either of the +5.3 V dc sources fails, its steering diode is reverse biased, and the redundant supply takes over. This prevents a short circuit of the output stage of either power supply, or a drop in its output voltage from affecting the BC logic operation.

2.2.5 Peripheral Devices

2.2.5.1 RANK (FA 10095/3). (Figure 11-13): The RANK enables an operator to compose, edit, and enter messages to the Host. The RANK consists of 71 illuminated keys, a space bar, and a MWL. RANK entries may be displayed on a CRT and edited on either a CRT or RFSP as specified by the RCU configuration. From one to five RANKs may interface with an RCU cabinet assembly. Each RANK is connected to the peripheral interface of one BC board.

The RANK contains the keyboard assembly, keyboard control microcomputer, support hardware, and a 5 V power supply. The RANK interface is full duplex, RS-422 and asynchronous at 2400 baud. When a key is pressed, the RANK outputs the corresponding 8-bit ASCII code (seven data bits and one odd parity bit) to the BC board. The RANK also receives command bytes which initiate a diagnostic test, and turn the MWL lamp ON and OFF.

2.2.5.2 Keyboard Switch Matrix. (Figure 11-13 (1)): The keyboard consists of 72, Hall-effect, push button switches wired together in an 8x10 (X, Y) matrix. There are two unlabeled keys for future application. Both are now not operable. When a key is pressed, continuity is established between the horizontal (X axis) and the vertical (Y axis) matrix lines. The X and Y lines are connected to the keyboard microcomputer (U4) which identifies each key entry. Figure 11-15 shows the codes output by the RANK when each key is pressed.

2.2.5.3 Microcomputer (U4). (Figure 11-13 (2)): The microcomputer consists of a model Analog to Digital Converter (ADC) 8039 device which functions as the keyboard controller and interface. The microcomputer operation is specified by a firmware program contained in the EPROM (U2). The microcomputer is programmed to perform the following functions:

- Detect and identify key depression(s).
- Generate 8-bit ASCII key codes.
- Buffer each key code and parity in an internal 8x8 First In First Out (FIFO).
- Assemble and output each key code in serial asynchronous format (one start bit, one stop bit).
- Perform EPROM checksum test when commanded by RCU.

- Turn MWL ON and OFF when commanded:

  ON = 11
  OFF = 13

The detection and identification of key depressions are accomplished by a scanning technique described as follows:

- The RANK microcomputer continuously scans each of the 10 keyboard rows (X0-X9) in sequence, by applying 5 V to each row for approximately 10 milliseconds (ms).
- During the time each row is scanned, the microcomputer reads all eight column lines (Y0-Y7). Pressing a key, switches 5 V from the key row line to the key column line. The microprocessor detects a key depression when a column line is at 5 V. The microprocessor identifies the particular key pressed by identifying the particular row and column lines that are at 5 V.

2.2.5.4 Firmware EPROM (U2). (Figure 11-13 ③): The firmware EPROM (see RANK Blocked Schematic), resides on a model 2716 EPROM device. It contains 2,048 bytes of nonvolatile storage for the RANK microcomputer firmware instructions and character code table. The firmware EPROM is enabled by PSEN/ which is automatically output by the microcomputer during an operation code fetch or whenever an EPROM read instruction is executed. Firmware EPROM addresses are output by the microcomputer. A0-A7 are output by the microcomputer via the address latch (U3). Operation codes, constants and character code table values, stored in the EPROM, are output to the microcomputer via the data bus (DB0-DB7).

2.2.5.5 Row Decoder (U1). (Figure 11-13 ④): The row decoder resides on a model 74LS145 device. The row decoder translates the 4-bit row code (output by the microcomputer) to one of ten mutually exclusive outputs. Each row decoder output activates one of the ten keyboard matrix rows (X0-X9).

2.2.5.6 Address Latch (U3). (Figure 11-13 ⑤): The address latch resides on a model 74LS373 (8-bit latch) device. The address latch temporarily stores the lower eight bits of the firmware EPROM address (A0-A7).

The microcomputer bus (DB0-7) is multiplexed and contains both data and address. When the firmware EPROM address is present on DB0-7, ALE goes high, latching the address on the bus. The latched address bits (A0-A7) are output to the firmware EPROM (U2).

2.2.5.7 TTL to RS-422 Driver (U2). (Figure 11-13 ⑥): The TTL to RS-422 driver resides on a model 75158 device. The driver converts the RANK serial output data from TTL logic levels (single ended, unbalanced) to RS-422 (two wire, balanced, differential) logic levels (+ 3.6 V).

2.2.5.8 RS-422 to TTL Receiver (U6). (Figure 11-13 ⑦): The RS-422 to TTL receiver resides on a model 75157 device. The receiver converts RANK serial input data from RS-422 (two wire, balanced, differential) logic levels to TTL (single ended, unbalanced) logic levels.

2.2.5.9 Lamp Driver (U22). (Figure 11-13 ⑧): The lamp driver resides on a model 75451B device. The lamp driver provides current required to illuminate the MWL.

2.2.5.10 Watchdog Timer (U5). (Figure 11-13 ⑨): The watchdog timer resides on a model 74LS123 (dual retriggerable, one shot) device. The watchdog timer resets the microcomputer (U4)

in the event that the microcomputer inadvertently halts. During normal microcomputer operation, the ALE pulse is output every 3 ms and retriggers the first one shot. If the microprocessor halts, ALE stays low, allowing the one shots to time out and reset the microcomputer.

2.2.5.11 Power Source. (Figure 11-13 (10)): The +5 V dc power to the RANK is provided by a Power One power supply. Power is provided to connector number 43 pins 1 and 2 for the keyboard logic circuits and key lamps. Pins 3 and 4 of connector number 43 provide power to the MWL.

2.2.4.2.2 Normal Operation.- The bus connector interfaces between its peripheral and its control unit.

2.2.4.2.3 Maintenance Channel.- Any bus connector can be used as a maintenance channel. Usage as a maintenance channel depends on the control unit type (RCU and PCU) and the bus connector's address (21 for RCU or 29 for PCU). When powered up as a maintenance channel, and attached to an RFSP, the bus connector sends the RFSP front panel enable sequence to the RFSP. (The actual command sequence has been purposely left out of this document according to FAA request.) The front panel enable sequence is ignored by RFSP FA 10095/11 and RFSP FA 10095/14. Otherwise, a maintenance channel bus connector is identical to any other bus connector in the system.

Figure 2-14 illustrates the following seven major functional circuits of the bus connector:

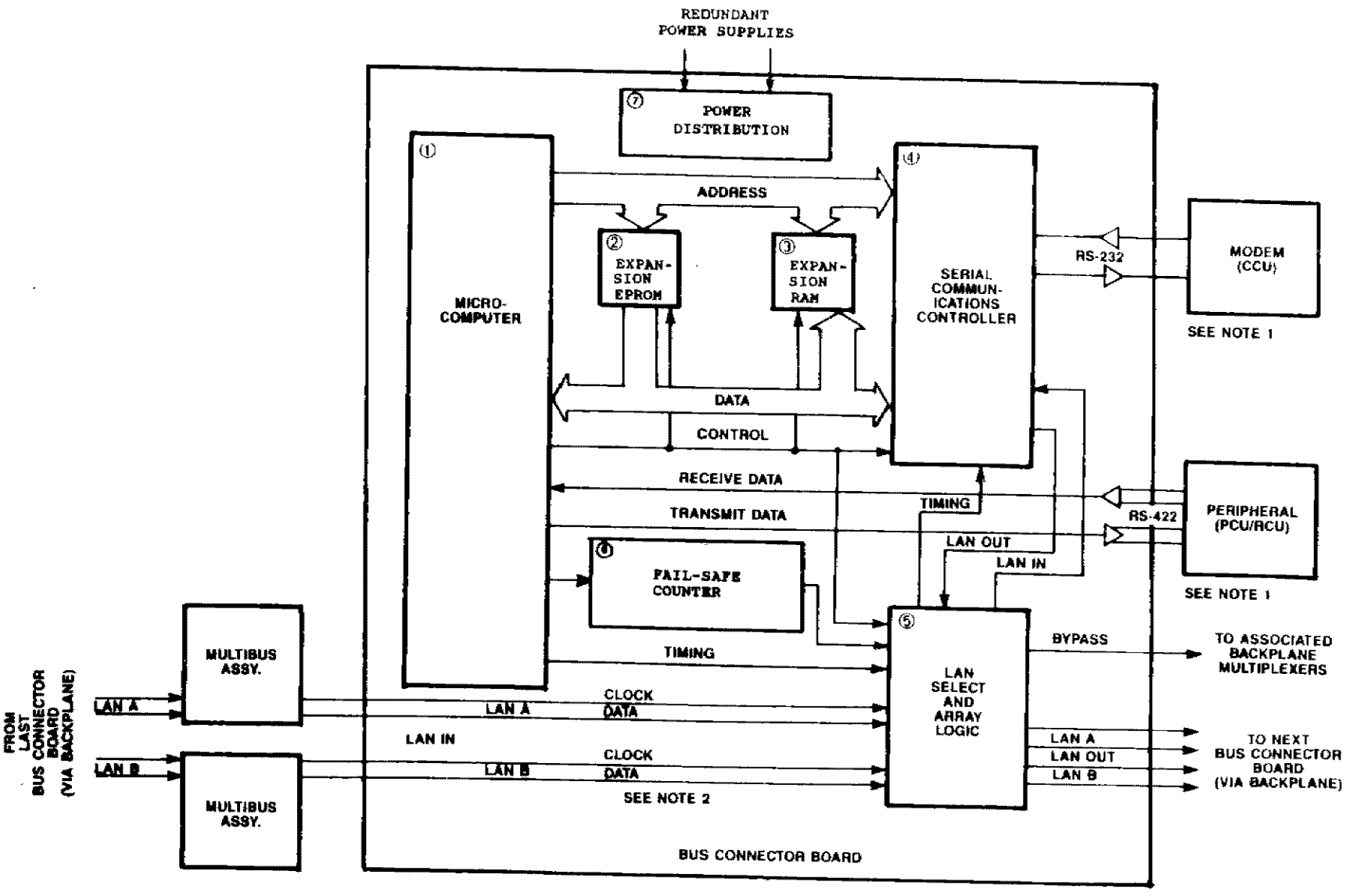
1) Microcomputer
2) Expansion EPROM
3) Expansion RAM
4) Serial communications controller
5) LAN select and array logic
6) Fail-Safe counter
7) Power distribution

Figure 11-12 (Sheets 1 through 3) is a detailed schematic diagram of the bus connector hardware with the major functional circuits designated by a circled number. The following subparagraphs describe each functional section.

2.2.4.2.4 Microcomputer.- (Figure 11-12, Sheets 2 and 3 of 3 1) The microcomputer contains the clock oscillator, 8031 microcomputer, address latch and LAN address switches. It fetches and executes instructions from the EPROM memory and performs other I/O and control operations.

2.2.4.2.4.1 Clock Circuit.- An external 11.059 MHz oscillator (Y1) provides a square wave TTL clock. This clock, presented to the XTAL2 input of the microcomputer chip (U1), becomes the time base for all internal clocking signals. The 11.059 MHz clock is fed to the Programmable Array Logic (PAL) device which divides the clock by 4 to produce a 2.76 MHz clock (U2). The 2.76 MHz clock is used by the Serial Communications Controller (SCC) for internal timing. Jumper E1 disconnects the oscillator from the rest of the circuit allowing injection of an external clock source during testing.

2.2.4.2.4.2 8031 Microcomputer.- The 8031 microcomputer (U1) is a functional microcomputer on a silicon chip. The microcomputer contains an 8-bit CPU, a read/write memory, a parallel I/O, two 16- bit timer/counters, a full duplex serial port, and a five-source interrupt structure. 128 bytes of internal RAM are partitioned into general purpose registers, special function registers, program stack, and general purpose memory for variable storage. The internal RAM is augmented by 8K bytes of off-chip expansion RAM (U6).



NOTE 1: EACH BUS CONNECTOR BOARD SUPPORTS ONE PERIPHERAL OR ONE MODEM.
NOTE 2: CCU/PCU REDUNDANT LAN SHOWN. RCU USES ONLY ONE LAN CHANNEL.

Figure 2-14. Bus Connector Major Function Diagram

The program for controlling the bus connector resides in 8K bytes of EPROM external to the 8031 chip.

On power up, a reset circuit consisting of R1 and C1 guarantees that the reset input (U1 pin 9) remains active until the power supply stabilizes and the 8031 microcomputer is able to begin operation.

The 8031 contains four 8-bit bidirectional I/O ports, P0 through P3, which perform the following functions:

Port 0: This port is used during the process of accessing expansion memory (RAM or EPROM). The port alternately contains actual data or the lower eight bits of the 16-bit external address. The actual data has been read from RAM, EPROM, or the SCC, or the actual data is to be written to RAM or the SCC. The address latch, U3, is used to latch the lower eight address lines (AD0 through AD7) emanating from port 0 of the 8031.

Port 1: The lower seven bits of port 1 are configured as inputs and are connected to the seven-position DIP switch (S2). S2 contains the LAN address. Bit 8 of port 1 is the output signal, LANEN/. LANEN/, when active (low), the bus connector is connected to the LAN bus.

Port 2: Port 2 contains the upper eight bits of the 16-bit address when accessing expansion RAM, EPROM, or SCC.

Port 3: Port 3 is configured as a special function port. Each bit position performs the following special function:

MSB							LSB
7	6	5	4	3	2	1	0

Bit	Description
0	RxD: Data received by the internal serial port from the RANK, CRT, or RFSP.
1	TxD: Serial data transmitted by the internal serial port to the RANK, CRT, or RFSP.
2	INT0/: External interrupt generated by the SCC due to a LAN, or modem character interrupt.
3	RESET/: Output signal used to reset the LAN clock detection logic.
4	TEST: Output signal that places the LAN select logic into loop back mode.
5	TRST/: Output signal that resets the fail-safe timer.
6	WR/: Output signal that is the external data memory write strobe.
7	RD/: Output signal that is the external data memory read strobe.

The 8031 contains an asynchronous interface for communicating with a RANK, CRT, or RFSP. An internal baud rate generator provides the 2400 Hz clock. The serial input signals from the peripheral device enter the bus connector from the BC backplane via P1 (PTXP and PTXN) and are converted from RS 422 to TTL by receiver chip U11. The converted signals enter the RxD input (port 3 bit 0) of the 8031. Serial output data to the peripheral device exits the 8031 microcomputer via the TxD output pin (port 3 bit 1). The data is then routed to driver chip U12 where the serial TTL signal is converted to RS 422. The RS 422 output signals (PRXP and PRXN) exit the bus connector via P1 to the bus connector backplane and then to the peripheral device.

2.2.4.2.4.3 LAN Address Switches.- The BC LAN address is encoded in the seven-bit DIP switch (S2) for 128 possible LAN (or bus connector) addresses. The individual switch elements are connected to the lower seven bits of port 1 and are pulled to a nominal TTL high logic level by the pull-up resistor (RN1). If the switch is closed, the logic level is forced to a TTL low level. Table 2-21 lists the switch settings necessary to configure the BC for addresses 1 through 29 as required for FDIO operation.

Table 2-21. LAN ADDRESS SWITCH SETTINGS

C = closed (ON = "0") O = open (OFF = "1")

Bus Connector Card Cage Slot	Recommended Bus Connector Address (decimal/hex)	Bus Connector Address Switches 1	2	3	4	5	6	7
upper cardcage 1	1 / 01	O	O	C	C	C	C	O
2	2 / 02	O	O	C	C	C	O	C
3	3 / 03	O	O	C	C	C	O	O
4	4 / 04	O	O	C	C	O	C	C
5	5 / 05	O	O	C	C	O	C	O
6	6 / 06	O	O	C	C	O	O	C
7	7 / 07	O	O	C	C	O	O	O
8	8 / 08	O	O	C	O	C	C	C
9	9 / 09	O	O	C	O	C	C	O
10	10 / 0A	O	O	C	O	C	O	C
11	11 / 0B	O	O	C	O	C	O	O
12	12 / 0C	O	O	C	O	O	C	C
13	13 / 0D	O	O	C	O	O	C	O
14	14 / 0E	O	O	C	O	O	O	C
15	15 / 0F	O	O	C	O	O	O	O
16	16 / 10	O	O	O	C	C	C	C

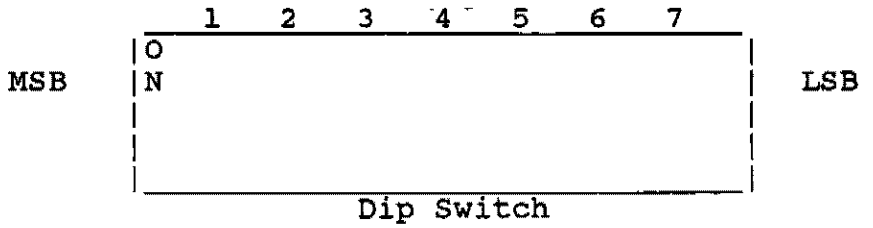


Table 2-21. LAN Address Switch Settings - Continued

Bus Connector Card Cage Slot	Recommended Bus Connector Address decimal/hex)	Bus Connector Address Switches 1	2	3	4	5	6	7
Lower Cardcage								
1	17 / 11	O	O	O	C	C	C	O
2	18 / 12	O	O	O	C	C	O	C
3	19 / 13	O	O	O	C	C	O	O
4	20 / 14	O	O	O	C	O	C	C
5	21 / 15	O	O	O	C	O	C	O
6	22 / 16	O	O	O	C	O	O	C
7	23 / 17	O	O	O	C	O	O	O
8	24 / 18	O	O	O	O	C	C	C
9	25 / 19	O	O	O	O	C	C	O
10	26 / 1A	O	O	O	O	C	O	C
11	27 / 1B	O	O	O	O	C	O	O
12	28 / 1C	O	O	O	O	O	C	C
13	29 / 1D	O	O	O	O	O	C	O

2.2.4.2.5 Expansion EPROM.- (Figure 11-12, Sheet 2 of 3 (2)) The 8031 microcomputer fetches and executes program instructions from off-chip expansion program memory EPROM. Although the 8031 microcomputer can address up to 64K bytes of program memory, the bus connector contains a 28-pin socket (U4) that can accommodate a 2764 (8K bytes) EPROM or a 27128 (16K bytes) EPROM. In order to access all locations, the 8K byte EPROM requires 13 address lines, and the 16K byte EPROM requires 14 address lines. When the 16K byte capability is to be used, jumper E2 connects the highest address line (pin 26 of U4) to address line A13; otherwise, jumper E3 connects pin 26 of U4 to a logical high via pullup resistor RN2.

See the EPROM Read Cycle Timing diagram, Figure 2-15, for a graphic depiction of the following description of an EPROM read cycle. The 8031 microcomputer uses ports 0 and 2 to access off-chip memory. During the first part of the read cycle, the lower eight bits of the address are output on port 0, and the upper eight bits are output on port 2. When the address lines are stable, the 8031 causes signal ALE to change from high to low. This causes the lower eight address bits from port 0 to be latched by transparent latch U3. The upper address bits do not require external latching, since the 8031 keeps them stable throughout the read operation.

The latched addresses are presented to the EPROM to select the desired location. When the required address setup time delay has elapsed, the 8031 causes signal PSEN/ to go active low. This connects the contents of the selected EPROM location to the port 0 lines. These lines have since become inputs. The 8031 reads the contents of the EPROM via port 0. When the operation is complete, PSEN/ is de-activated to disable the output of the EPROM, and a new memory address is setup on ports 0 and 2.

2.2.4.2.6 Expansion RAM.- (Figure 11-12, Sheet 2 of 3 3) Although the 8031 microcomputer can address up to 64K bytes of expansion RAM, the bus connector contains a single byte-wide 8K byte RAM (U6). See the RAM Read/Write Operations Timing diagram, Figure 2-15, for a graphic depiction of the following descriptions.

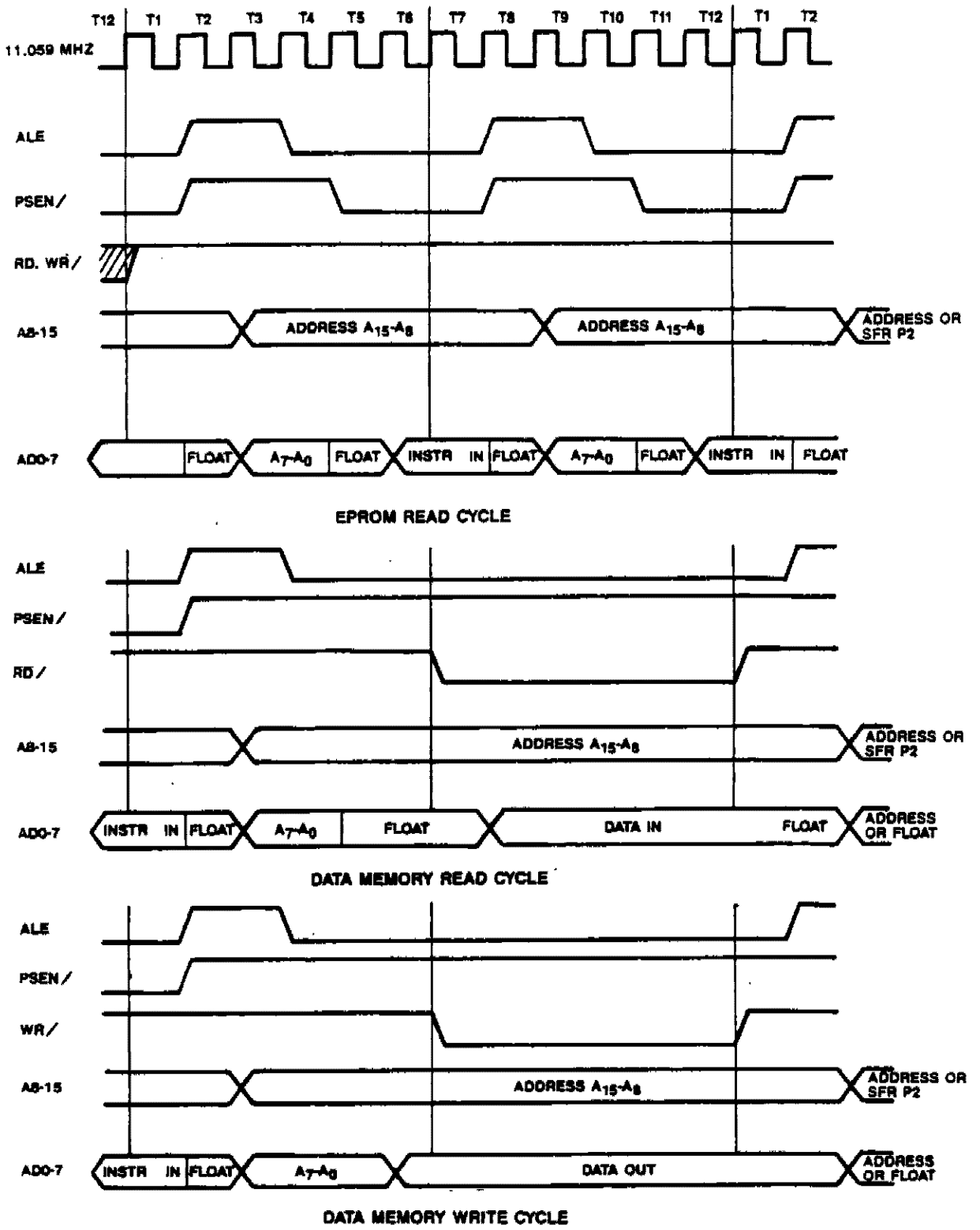


Figure 2-15. Microcomputer Timing Diagram

In order to access off-chip RAM, the 8031 microcomputer uses ports 0 and 2. During the first part of the read/write cycle, the lower eight bits of the address are output on port 0, and the upper eight bits are output on port 2. When the address lines are stable, the 8031 causes signal ALE to change from high to low. This causes the lower eight address bits from port 0 to be latched by transparent latch U3. The upper address bits do not require external latching, since the 8031 keeps them stable throughout the read/write operation.

Latched address bits A0 through A12 are presented to the RAM to select the desired location, and address bits A13 through A15 are decoded by the select logic contained in the PAL (U2). PAL output RAMEN/ is active low when input lines A13, A14, and A15 are each a logical low. This is shown in the following Boolean equation:

$$\text{RAMEN/} = \overline{\text{A13}} \text{ AND } \overline{\text{A14}} \text{ AND } \overline{\text{A15}}$$

When a read/write request is made of the lower 8K bytes of RAM, A13 through A15 are low. This activates RAMEN/ which is connected to the chip select input of the RAM (U6 pin 20).

If a RAM read operation is to be performed, the 8031 microcomputer causes signal RD/ to go active (low) after the required address and chip select setup delays have elapsed. This connects the contents of the selected RAM location to the port 0 lines which have become inputs. The 8031 reads the contents of the RAM via port 0. When the operation is complete, RD/ is de-activated to disable the output of the RAM.

When a RAM write operation is performed, the 8031 outputs the data to be written into RAM to port 0. After the required address data and chip select setup delays have elapsed, the 8031 strobes WR/ low. This causes the contents of port 0 to be written into the selected RAM location.

2.2.4.2.7 Serial Communications Controller.- (Figure 11-12, Sheets 2 and 3 of 3 (4)) The serial communications controller (SCC) circuit consists of an 82530 (U5) containing two separate serial channels. Channel A is used for communication with the LAN and channel B for communication with a modem. This circuit contains separate RS 232 drivers and receivers for the modem interface.

The SCC is controlled by the 8031 microcomputer in the same way external RAM is accessed. The SCC is a memory mapped I/O (MMIO) device which the processor views as a range of memory locations. Commands and data are sent to the SCC by performing an external memory write to the desired location; status and data are read from the SCC by performing an external memory read from the desired location. The MMIO addresses are as follows:

Address (hex)	SCC Port Selected
A000	Modem command/status port
A001	Modem data port
A002	LAN command/status port
A003	LAN data port

The read/write operational sequence is the same as the one described for expansion RAM operation except that the SCC requires address bits A0 and A1, and the chip select is enabled by signal COMEN/.

Latched address bits A0 and A1 are presented to the SCC for selection of the desired port (LAN, modem, command/status, or data), and address bits A13 through A15 are decoded by the select logic contained within the PAL (U2). PAL output COMEN/ is active low when input lines A13, A14, and A15 are at logic one, zero and one, respectively. This is shown in the following Boolean equation:

$$\text{COMEN/} = A13 \text{ AND } \overline{A14} \text{ AND } A15$$

When a read/write request is made within the address range A000 through BFFF (hex), COMEN/ is activated enabling the SCC for I/O operations via its chip select line (pin 33).

When a read operation of the SCC is performed, the 8031 microcomputer causes signal RD/ to go active (low) after the required address and chip select setup delays have elapsed. This connects the connects of the status or data register to port 0 lines. These lines have since become inputs. The 8031 then reads the information via port 0. When the operation is complete, RD/ is de-activated to disable the output of the SCC.

When a write operation to the SCC is to be performed, the 8031 outputs the control or data byte to port 0. After the required address data and chip select setup delays have elapsed, the 8031 pulses WR/ (low). This causes the contents of port 0 to be written into the SCC.

2.2.4.2.7.1 LAN Channel.- The LAN operates in synchronous mode at a 19,200 baud rate. The TTL data (RxDA) and clock (TxCA) signals are received from the iSBC 88/45 via the LAN select logic and enter the SCC at the receive data (RxDA) and receive clock (RTxCA/) pins, respectively. The LAN clock is provided by the LAN interface circuit on the iSBC 88/45 board and becomes the master LAN clock for receive and transmit operations of each bus connector. This is accomplished by connecting receive clock input pin RxCA to transmit clock output pin TxCA of the SCC. The transmit data (TxDA) and clock (TxCA) signals are passed to the LAN select logic where they are buffered, directed to the appropriate redundant LAN, and sent to the bus connector backplane via P1.

2.2.4.2.7.2 Modem Channel.- The modem operates in synchronous mode at a 2400 baud rate. The modem receive data (MTX) and clock (MTC) signals enter the bus connector from the bus connector backplane via connector P1 (pins 29 and 31). These signals are converted from RS 232 to TTL by receiver U7, becoming RxDB and TxCB. The signals then enter the SCC at the receive data (RxDB, pin 27) and receive clock (RxCB/, pin 28), respectively. The modem clock originates at the modem and becomes the master clock for both receive and transmit operations. This is accomplished by connecting receive clock input pin RxCB/ to transmit clock output pin TxCB/ (pin 26) of the SCC. The transmitted data (TxDB, pin 23) and clock (TxCB) lines are converted to RS 232 by drivers (U13), becoming MRX (pin 25) and MRC (pin 27) for transmission to the modem via the bus connector backplane via P1.

2.2.4.2.8 LAN Select and Array Logic.- (Figure 11-12, Sheet 3 of 3 (5)) This circuit consists of a Programmable Array Logic (PAL) device and other supporting circuitry and performs the following five major functions:

1. Four stage binary counter
2. MMIO decode logic
3. LAN source select and access control
4. LAN loop-back operation
5. Bus connector self-test operation

See the internal PAL logic equivalent circuit in Figure 2-16 while reading the following discussions.

2.2.4.2.8.1 Four Stage Binary Counter.- The PAL contains internal logic that operates as a four-stage binary counter. The PAL inputs and outputs are as follows:

Inputs	Outputs	Description
11.059 MHz		Input clock from crystal oscillator
	2.76 MHz	Output clock derived by dividing the input clock by 4, used as an input by the SCC
	TESTCLK	691 kHz output clock derived by dividing the input clock by 16, used during LAN loopback test

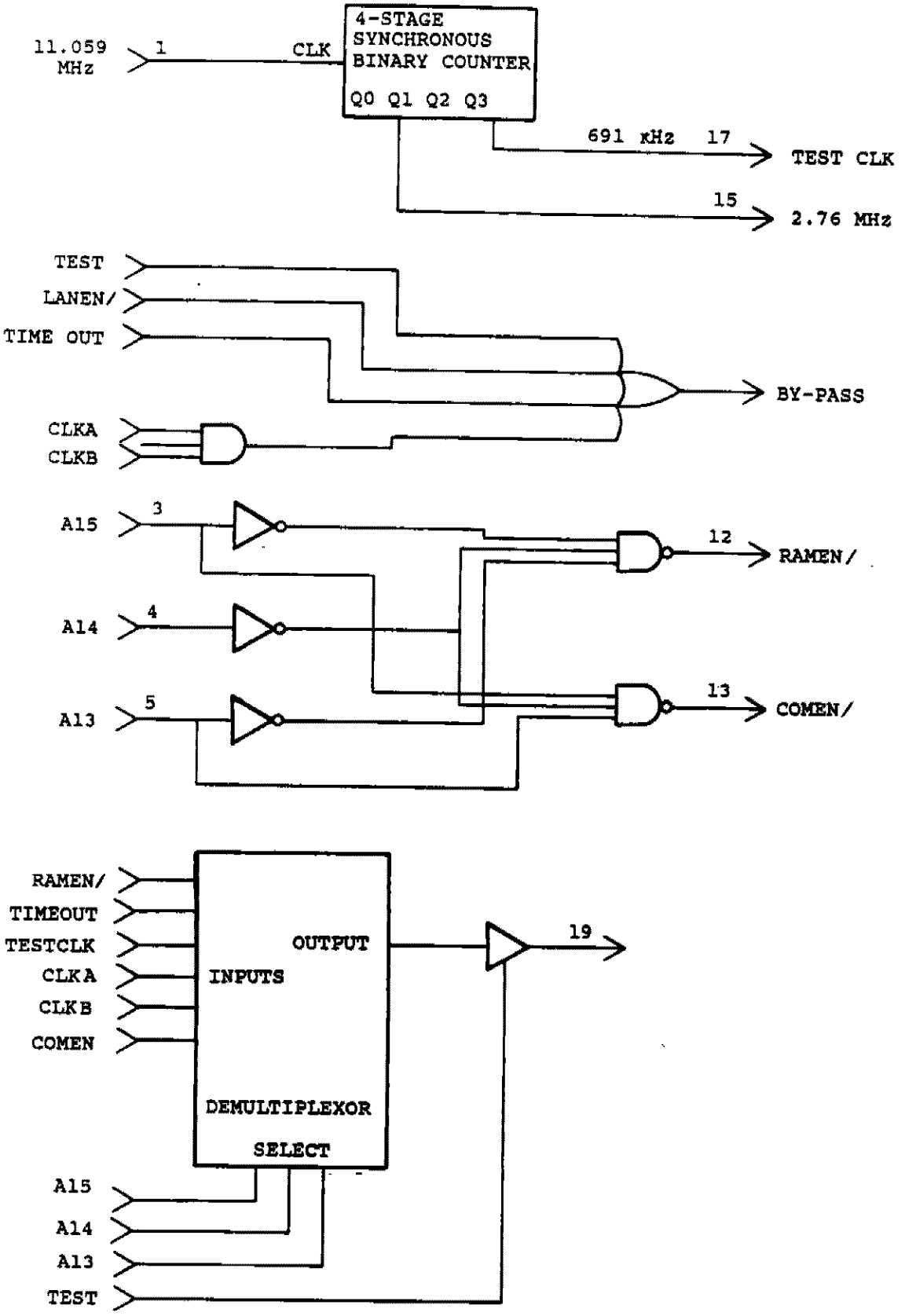


Figure 2-16. PAL Logic Diagram

2.2.4.2.8.2 Memory Mapped Input Output (MMIO) Decode Logic.- The PAL contains logic that performs unconditional decoding of the address inputs A13, A14, and A15. The two output chip select lines are for the RAM (RAMEN/) and the SCC (COMEN/).

Inputs	Outputs	Description
A13,A14,A15		Address inputs from the 8031 microcomputer to be decoded
	RAMEN/	Output line enabling the RAM for the correct address combination of the input address lines
	COMEN/	Output line enabling the SCC for the correct address combination of the input address lines

PAL output RAMEN/ is active low when input lines A13, A14, and A15 are a logical low. The following Boolean equation describes this:

$$\text{RAMEN/} = \overline{\text{A13}} \text{ AND } \overline{\text{A14}} \text{ AND } \overline{\text{A15}}$$

PAL output COMEN/ is active low when input lines A13, A14, and A15 are at logic one, zero, and one, respectively. The following Boolean equation describes this:

$$\text{COMEN/} = \text{A13 AND } \overline{\text{A14}} \text{ AND A15}$$

2.2.4.2.8.3 LAN Source Select and Access Control.- This circuit determines which one of two LAN buses is the active LAN and connects that LAN bus to the SCC. The LAN clock detect circuit consists of the dual mono-stable multivibrator circuits (U9). Only the LAN bus of the primary control unit will be operational and contain an active clock. The output of the LAN clock detect circuit selects the LAN bus to be connected to the SCC via demultiplexors U4 and U8. The active LAN information goes to the PAL where the decision to enable the bus connector onto the active LAN bus is made.

The two LAN clocks, CLOCKA and CLOCKB, enter the bus connector via P1. From P1 the clocks are routed to demultiplexor circuit U8 and to the "A" inputs of one of two identical LAN clock detect mono-stables (half of U9). Each mono-stable creates a positive pulse at the "Q" output when the clock signal present at the "A" input makes a logical high to low transition (the "B" input being at a logical high). The time constant of the mono-stables is defined by the attached resistor and capacitor combination (R3/C12 and R2/C11).

This yields an approximate 1 MSec pulse.

The mono-stables are retriggerable since the "Q" output remains high if the "A" input continues to transition from the high to low logical state within that 1 MSec period. The "Q/" output of each mono-stable exhibits the logical inverse signal of the "Q" output and is connected to the "B" input of the other mono-stable circuit. If one of the mono-stables is constantly being retriggered (due to a constant LAN clock at its "A" input) its "Q/" output is held low. This disables the other mono-stable by causing its "B" input to be low. Any noise or signal artifact coming in on the non-active LAN is filtered out and does not confuse the LAN clock detect circuit.

The outputs of the LAN clock detect circuit are the signals CLKA and CLKB. If the CLOCKA input is active (contains a square wave equal to the baud rate), clock detect line CLKA remains at an active high logical level and line CLKB remains at an inactive low logical level. If the CLOCKB input is active, signal CLKB remains at an active high level, and line CLKA is inactive. Signals CLKA/ and CLKB/ are buffered by U8 and illuminate green clock indicators I2 and I3. I2 is on if LAN A is active, and I3 is on if LAN B is active.

An active low signal on CLKA/ or CLKB/ results in bus connector backplane signal CLOCKA/ or CLOCKB/ being pulled low through diode CR2 or CR4. CLOCKA/ and CLOCKB/ are common to all bus connectors and can be activated by any active bus connector on the SCLC loop (i.e., BYPASS is low). These signals illuminate indicators on the bus connector backplane indicating the currently active LAN.

Signal CLKB is presented to the LAN select circuit consisting of U4, U8, and U15. If the active clock is from LAN B, CLKB will be high. When signal TEST is inactive (low), output U15 pin 6 will be low, and U15 pin 11 will be high. This enables the top four buffers of U4 and disables the top four buffers of U8. B LAN data and clock signals, DATA B and CLOCK B, are connected to the SCC via RxDA and TxCA. (RxDA and TxCA refer to channel A of the dual channel SCC handling the LAN interface.) Similarly, the LAN select circuit routs the SCC transmit data (TxDA) and clock (TxCA) signals to active LAN B bus output signals DATAB and CLOCKB.

When the A LAN is active, signal CLKB is low. This connects the A LAN data and clock signals, DATA A and CLOCK A, to the SCC via RxDA and TxCA. The SCC transmit data and clock signals drive the active LAN A bus signals DATA A and CLOCKA.

Another section of the PAL is responsible for determining whether the bus connector may access the LAN bus. The following signals are involved in the decision process:

Inputs	Outputs	Description
CLKA		LAN A clock detect signal
CLKB		LAN B clock detect signal
LANEN/		Signal under 8031 firmware control, set when bus connector becomes part of SDLC loop
TEST		Signal under 8031 firmware control, set to activate self test
TIMEOUT		Output of hardware timeout circuit, goes high if system fails and a time out occurs
	BYPASS	Output signal goes inactive (low) to enable the bus connector onto active LAN bus and become part of SDLC loop

When PAL output BYPASS is active (high), the bus connector backplane ignores bus connector output, causing the bus connector to be bypassed by the SDLC loop. When inactive (low), the bus connector backplane connects the bus connector output to the input of the next bus connector to propagate the signal around the SDLC loop. The following boolean equation shows this:

$$BYPASS = TEST \text{ OR } \overline{LANEN} \text{ OR } TIMEOUT \text{ OR } (CLKA \text{ AND } CLKB)$$

If the TEST or TIMEOUT signal is active, the bus connector is bypassed. If both LAN clocks are active, the bus connector is bypassed. If the above conditions are correct and the firmware enables LANEN/, the bus connector will exit the bypass state and become an active part of the SDLC loop.

When the bus connector is communicating with the LAN (BYPASS is low), green indicator I1 is illuminated.

2.2.4.2.8.4 LAN Loopback Operation.- The basic LAN operation is verified by enabling the LAN loopback feature. By enabling signal TEST, the 8031 microcomputer checks the operation of the SCC LAN channel without an operational LAN.

When activated, TEST causes the PAL to activate signal BYPASS to remove the bus connector from the SDLC loop and avoid any contamination of loop operations. This disables the top four buffers of U4 and U8, and enables the bottom two buffers of U4. The SCC LAN channel data output (TxDA) is effectively connected to its own input (RxDA) in order to verify the transmit and receive

operations of the SCC. The SCC interrupt operation is also verified in this manner.

2.2.4.2.8.5 Bus Connector Self-Test Operation.- See Figure 2-16 for the PAL Logic Diagram. The bus connector self-test operation. This operation is performed by the PAL (U2), and monitors some of the bus connector functions not directly accessible by the 8031. These functions include the outputs of two clock detectors, the Q3 output of the 4-stage binary counter, and the TIMEOUT signal. The PAL circuit permits the 8031 to monitor these internal signals during test mode by connecting pin 19 of the PAL to the signal LANEN/. When not in test mode, pin 19 is tri-stated and does not affect the operation of LANEN/. When self-test is enabled by turning on TEST, the bus connector is forced into bypass mode, and one of the internal signals is enabled onto pin 19 of the PAL. Since bypass mode is forced here, the 8031 microcomputer redefines LANEN/ as an input pin and facilitates signal reading.

By selecting the proper address on A13 through A15, the state of each input is sent back to the 8031 by reading signal LANEN/. The list below shows the monitored signals and the addresses required for each.

Address	Signal Enabled Onto LANEN/
0XXX (hex)	RAMEN
2XXX (hex)	TIMEOUT
4XXX (hex)	TESTCLK
6XXX (hex)	CLKA
8XXX (hex)	CLKB
AXXX (hex)	COMEN
CXXX (hex)	None - used to reset 4-stage counter

2.2.4.2.9 Fail-Safe Counter.- (Figure 11-12, Sheet 3 of 3 6) The fail-safe counter consists of a 14-stage CMOS counter (U10) and select jumpers E4 through E9. The clock input is connected to the active LAN clock (TxCA) which operates at 19,200 baud. The output stages of six of the counters are routed to jumper pins, allowing the user to select the time out period as follows:

Jumper	Output Term	Time Out Period (Note 1)
E6	Q9	13 MSec (divide by 256)
E5	Q10	27 MSec (divide by 512)
E4	Q11	53 MSec (divide by 1024)
E9	Q12	107 MSec (divide by 2048)
E8	Q13	213 MSec (divide by 4096)
E7	Q14	427 MSec (divide by 8192)

Note 1: These times assume a LAN baud clock of 19.2K Baud

The reset input of the fail-safe timer (U10 pin 11) is connected to signal TRST, which is controlled by the 8031 microcomputer. When TRST is brought low, the reset input is removed, and the counter begins to count. If TRST remains low, the selected time out eventually elapses, and signal TIMEOUT goes high. This forces the bus connector into bypass mode via the internal PAL logic. The microcomputer holds off the time out by periodically pulsing TRST high to reset the counter. The reset pulse must be issued before the time out period to prevent the time out from occurring. Typically, an internal counter or other periodic occurrence within the 8031 microcomputer or its environment will trigger the reset of the fail-safe timer. If the microcomputer fails to operate correctly, the fail-safe timer forces the bus connector off the LAN bus and avoids contamination of the entire LAN.

2.2.4.2.10 Power Distribution.- (Figure 11-12, Sheet 1 of 3 (7)) The bus connector requires three voltages for proper operation: +5 VDC for the logic circuits, microcomputer, and memory, and ±12 VDC for the RS 232 drivers and receivers required for the modem interface. If the bus connector is not part of the CCU LAN, the ±12 VDC sources are not required. These voltages are distributed to each bus connector through the bus connector backplane.

The bus connector backplane and bus connector are powered by redundant + 5 VDC power supplies. If one supply fails, the other can assume responsibility. The bus connector receives the two +5 VDC sources via P1, one on pins 1 and 2 and the other on pins 11 and 12. The input voltage at the P1 pins of the bus connector is higher than nominal, approximately +5.3 VDC. Schottky silicon diodes on the bus connector (CR5 and CR6) constitute a power steering circuit protected by picofuses (F1 and F2). The voltage drop across the diode is approximately .3 volts and results in applying a net voltage of 5 volts to power switch S1. When S1 is closed, this voltage is applied across filter capacitor C2 and to the logic circuits.

If either of the +5.3 VDC sources fails, its steering diode is reverse biased, and the redundant supply takes over. This prevents a short circuit of the output stage of either power supply, or a drop in its output voltage from affecting the bus connector logic operation.

2.2.5 Peripheral Devices.-

2.2.5.1 Replacement Alphanumeric Keyboard (RANK).- (Figure 11-13) The RANK enables an operator to compose, edit, and enter messages to the NAS 9020. The RANK consists of 71 illuminated keys, a space bar, and a message waiting light (MWL). RANK entries may be displayed on a CRT and edited on either a CRT or RFSP as specified by the RCU configuration. From one to five RANKs may interface with an RCU cabinet assembly. Each RANK is connected to the peripheral interface of one bus connector board.

The RANK contains the keyboard assembly, keyboard control microcomputer, support hardware, and a 5V power supply. The RANK interface is full duplex, RS-422 and asynchronous at 2400 baud. When a key is pressed, the RANK outputs the corresponding 8-bit ASCII code (seven data bits and one odd parity bit) to the bus connector board. The RANK also receives command bytes which initiate a diagnostic test, and turn the MWL lamp on and off.

2.2.5.2 Keyboard Switch Matrix.- (Figure 11-13 ①) The keyboard consists of 72, Hall-effect, push button switches wired together in an 8 X 10 (X, Y) matrix. There are two unlabeled keys for future application. Both are now not operable. When a key is pressed, continuity is established between the horizontal (X axis) and the vertical (Y axis) matrix lines. The X and Y lines are connected to the keyboard microcomputer (U4) which identifies each key entry. Figure 11-14 shows the codes output by the RANK when each key is pressed.

2.2.5.3 Microcomputer (U4).- (Figure 11-13 ②) The microcomputer consists of a model ADC 8039 device which functions as the keyboard controller and interface. The microcomputer operation is specified by a firmware program contained in the EPROM (U2). The microcomputer is programmed to perform the following functions:

- Detect and identify key depression(s).
- Generate 8 bit ASCII key codes.
- Buffer each key code and parity in an internal 8 X 8 FIFO.
- Assemble and output each key code in serial asynchronous format (one start bit, one stop bit).
- Perform EPROM checksum test when commanded by RCU.
- Turn Message Waiting Light (MWL) on and off when commanded: ON = 11
  OFF = 13

The detection and identification of key depressions are accomplished by a scanning technique described as follows:

- The RANK microcomputer continuously scans each of the 10 keyboard rows (X0 - X9) in sequence, by applying 5 volts to each row for approximately 10 milliseconds.

- During the time each row is scanned, the microcomputer reads all eight column lines (Y0 - Y7). Pressing a key, switches 5 volts from the key row line to the key column line. The microprocessor detects a key depression when a column line is at 5 volts. The microprocessor identifies the particular key pressed by identifying the particular row and column lines that are at 5 volts.

2.2.5.4 Firmware EPROM (U2).- (Figure 11-13 ③) The firmware EPROM (see RANK Blocked Schematic, resides on a model 2716 erasable programmable read only memory (EPROM) device. It contains 2,048

bytes of nonvolatile storage for the RANK microcomputer firmware instructions and character code table. The firmware EPROM is enabled by PSEN/ which is automatically output by the microcomputer during an operation code fetch or whenever an EPROM read instruction is executed. Firmware EPROM addresses are output by the microcomputer. A0-A7 are output by the microcomputer via the address latch (U3). Operation codes, constants and character code table values, stored in the EPROM, are output to the microcomputer via the data bus (DB0 - DB7).

2.2.5.5 Row Decoder (U1).- (Figure 11-13 ④) The row decoder resides on a model 74LS145 device. The row decoder translates the 4-bit row code (output by the microcomputer) to one of ten mutually exclusive outputs. Each row decoder output activates one of the ten keyboard matrix rows (X0 - X9).

2.2.5.6 Address Latch (U3).- (Figure 11-13 ⑤) The address latch resides on a model 74LS373 (8-bit latch) device. The address latch temporarily stores the lower eight bits of the firmware EPROM address (A0 - A7).

The microcomputer bus (DB0-7) is multiplexed and contains both data and address. When the firmware EPROM address is present on DB0-7, ALE goes high, latching the address on the bus. The latched address bits (A0-A7) are output to the firmware EPROM (U2).

2.2.5.7 TTL To RS-422 Driver (U2).- (Figure 11-13 ⑥) The TTL to RS-422 driver resides on a model 75158 device. The driver converts the RANK serial output data from TTL logic levels (single ended, unbalanced) to RS-422 (two wire, balanced, differential) logic levels (± 3.6V).

2.2.5.8 RS-422 To TTL Receiver (U6).- (Figure 11-13 ⑦) The RS-422 to TTL receiver resides on a model 75157 device. The receiver converts RANK serial input data from RS-422 (two wire, balanced, differential) logic levels to TTL (single ended, unbalanced) logic levels.

2.2.5.9 Lamp Driver (U22).- (Figure 11-13 ⑧) The lamp driver resides on a model 75451B device. The lamp driver provides current required to illuminate the message waiting light (MWL).

2.2.5.10 Watchdog Timer (U5).- (Figure 11-13 ⑨) The watchdog timer resides on a model 74LS123 (dual retriggerable, one shot) device. The watchdog timer resets the microcomputer (U4) in the event that the microcomputer inadvertently halts. During normal microcomputer operation, the ALE pulse is output every three microseconds and retriggers the first one shot. If the microprocessor halts, ALE stays low, allowing the one shots to time out and reset the microcomputer.

2.2.5.11 Power Source.- (Figure 11-13 10) The +5 VDC power to the RANK is provided by a Power One power supply. Power is provided to connector number 43 pins 1 and 2 for the keyboard logic circuits and key lamps. Pins 3 and 4 of connector number 43 provide power to the message waiting light.

3.0 OPERATION

The following paragraphs describe the operation of FDIO control units and peripherals.

3.1 INTRODUCTION

This section provides information and instructions for operating the FDIO control and peripheral elements. The FDIO system enables efficient communication between system operators and the ARTCC Host computer. The FDIO system provides the capability of printing flight strips from the Host to both the ARTCC and ATCT remote locations. It also provides timely weather information, general information messages, and editing features for composition of en route messages from the ATCT to the Host.

3.1.1 Operational Modes

Several elements of the FDIO equipment can operate in more than one mode. All control element CCUs, PCUs, and RCUs operate in main mode under normal conditions, which means the equipment has been configured and is online. Main mode enables warning messages to be displayed on the front panel. In addition to main mode, the CCU, PCU, and RCU control elements have a Diagnostic (DIAG) mode to test the system for operation, and Reconfiguration (RECN) mode to assign primary/secondary status, pairing, backups, and error logger device. The RFSP peripheral element has a self-test procedure that can be run independently of the system.

3.2 CONTROLS AND INDICATORS

Paragraphs 3.2.1 through 3.2.13 describe the controls and indicators of the Multibus front panel assembly, the BC card controls and indicators, the BC backplane board indicators, the ac power distribution assembly, the dc power distribution assembly, and the RFSP, RANK, and CRT peripheral elements.

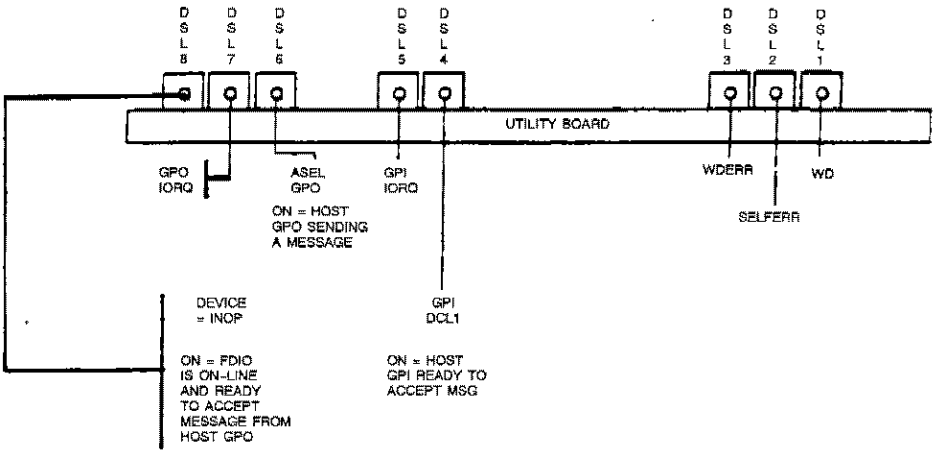
Each Multibus card cage assembly supports a 20-button keypad for operator initiated control. The RFSP (FA 10095/2) has a control panel with eight (8) push-button switches. RFSP (FA 10095/11) has a control panel with five (5) push-button switches. RFSP (FA 10095/14) has a control panel with four (4) push-button switches. The CRT has brightness and contrast controls: all other CRT operations are performed by the RANK. All control and peripheral elements in the FDIO system have an ON/OFF switch.

3.2.1 Multibus Assembly Controls

The Multibus assemblies (card cage and power supply) and the BC assemblies (card cage and power supply) use rocker type circuit breaker power switches. Individual BC boards use toggle switches. Fan assemblies are powered through an ac power distribution assembly.

3.2.1.1 iSBC 88/45 LED Indicators. Descriptions of the iSBC 88/45 LED indicators are located in the **iSBC 88/45 Advanced Data Communication Processor Board Hardware Reference Manual.**

3.2.1.2 Utility Board LED Indicators. There are eight LED indicators on the utility board (DSL1 - DSL8). The location and description of each are as follows:



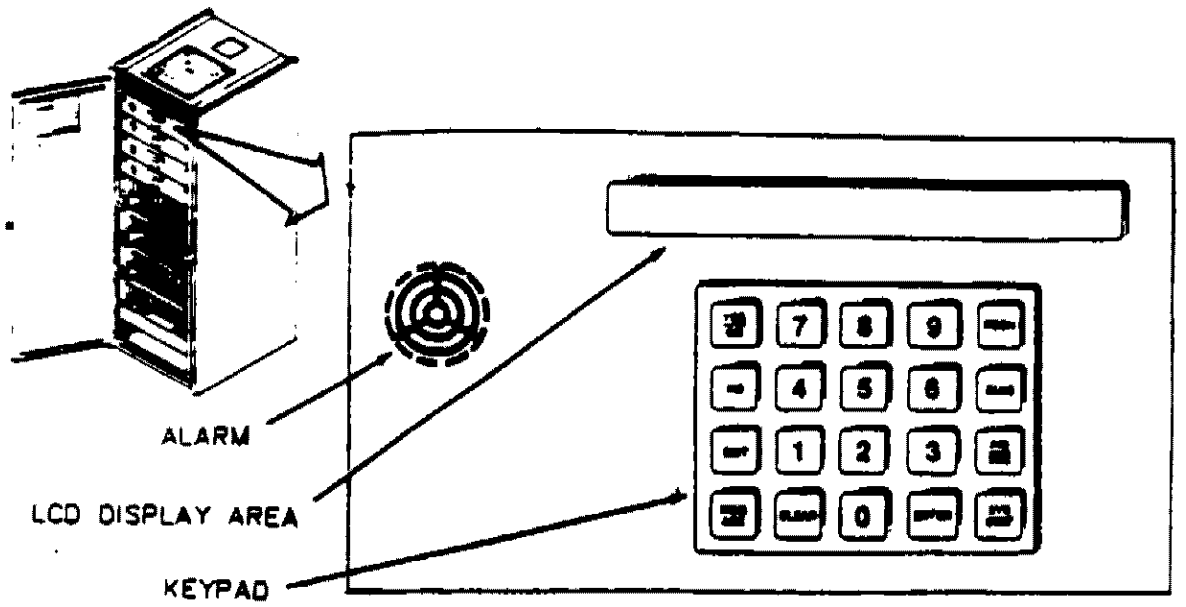
DSL1 = WD	Normal state — LED blinking indicating unit is online.
DSL2 = SELFERR	Normal state — LED OFF. When LED is ON, an internal error has been detected by FSE.
DSL3 = WDERR	Normal state — LED OFF. When LED is ON, a failure on the complementary unit has been detected.
DSL4 = GPIDCL1	When LED is ON, the Host GPI is ready to accept messages from FDIO.
DSL5 = GPIIORQ	When LED is blinking, a message transfer from FDIO to Host GPI is in progress.
DSL6 = ASEL	When LED is ON, the Host has a message ready for FDIO.
DSL7 = GPOIORQ	When LED is blinking, a message transfer from Host GPO to FDIO is in progress.
DSL8 = DEVICE INOP	When LED is ON, the FDIO unit is online. When LED is OFF, the FDIO unit is offline or the indicator circuit has failed. The LED must be ON before any communication can proceed between FDIO and NAS.

3.2.2 Multibus Front Panel Assembly Controls and Indicators

The Multibus front panel assembly features a 40-character LCD module display area, a 20-button keypad for operator initiated control, and a warning alarm for system error conditions.

In main mode, the LCD module is used to display system status or, if a system error condition exists, the entire LCD module will display the error message. When the front panel is performing a task, the LCD module will show task prompts.

The Multibus front panel keypad allows the technician to change primary/secondary assignments, clear error messages, and perform RECN or DIAG tasks. See figure 3-1 for Multibus front panel assembly controls and indicators.



CONTROL OR INDICATOR	FUNCTION
LCD DISPLAY AREA	SEE FIGURE 3-16 FOR FRONT PANEL STATUS FIELD DESCRIPTION.
ALARM	AUDIBLE MONETARY SIGNAL UPON ANY ERROR CONDITION CAUSING PERIPHERAL EQUIPMENT TO GO OFFLINE (RFSP OUT-OF-PAPER) OR AN ERROR IN THE SYSTEM.
NUMERIC KEYPAD (0-9)	INPUT TO DIAG, RECN, AND SEL DISPLAY PROMPTS. WHEN PRESSED, NUMBER APPEARS ON DISPLAY.
YES-GO	ALLOWS POSITIVE RESPONSE TO DIAG PROMPT.
RECN	ALLOWS ACCESS TO RECN OF UNIT ID AND STATUS, RANK PAIRING ERROR LOGGER, CRT PAIRING, TAB SETTING (AND FORMFEED TIME VALUE SETTING IN OCEANIC FIRMWARE).
NO	ALLOWS NEGATIVE RESPONSE TO DIAG PROMPT.
DIAG	ALLOWS ACCESS TO DIAG TASK.
EXIT	TO LEAVE OPERATOR INITIATED TASK (SEL, DIAG, OR RECN) AND RETURN TO NORMAL OPERATION.
PRI-SEC	TO SWITCH FROM PRIMARY TO SECONDARY CONTROL UNIT AT CCU AND PCU ONLY (ARTCC).
MSG-ACK	TO CLEAR ERROR MESSAGES SHOWN ON FRONT PANEL.
CLEAR	DURING RECN, SEL, AND DIAG, THIS KEY CLEARS NUMERIC DATA ENTERED BY THE OPERATOR PRIOR TO PRESSING ENTER.
ENTER	DURING RECN, SEL, AND DIAG, THIS KEY ENTERS NUMERIC DATA ON DISPLAY INTO MEMORY, THE NEXT PROMPT IN THE SEQUENCE IS THEN DISPLAYED.
SYS STAT	ALLOWS ACCESS TO SEL.

FIGURE 3-1. MULTIBUS FRONT PANEL ASSEMBLY CONTROLS AND INDICATORS

3.2.3 BC Card Controls and Indicators

Each BC card cage assembly will hold up to 16 board assemblies. Each BC board assembly is supplied with 5 V controlled by an individual toggle switch on the board. The switch will be set to the ON position at the time of installation. There are three indicator lights located immediately above the switch. One lamp indicates that the BC has acquired the LAN, one lamp designates clock A, and one lamp clock B. Clocks A and B indicate LAN activity of the primary or secondary CCU or PCU control elements. Remote sites always indicate clock A, because there is no secondary RCU. See figure 3-2 for BC board assembly controls and indicators.

3.2.4 BC Backplane Board Indicators

The BC backplane board is attached to the back of the BC card cage assembly and extends below the card cage. Eight LED lamps are mounted on the lower edge of the front face of the board. Six of these lamps indicate power supply output voltage nominal, and two indicate clock activity. See figure 3-3 for BC backplane board power indicator description.

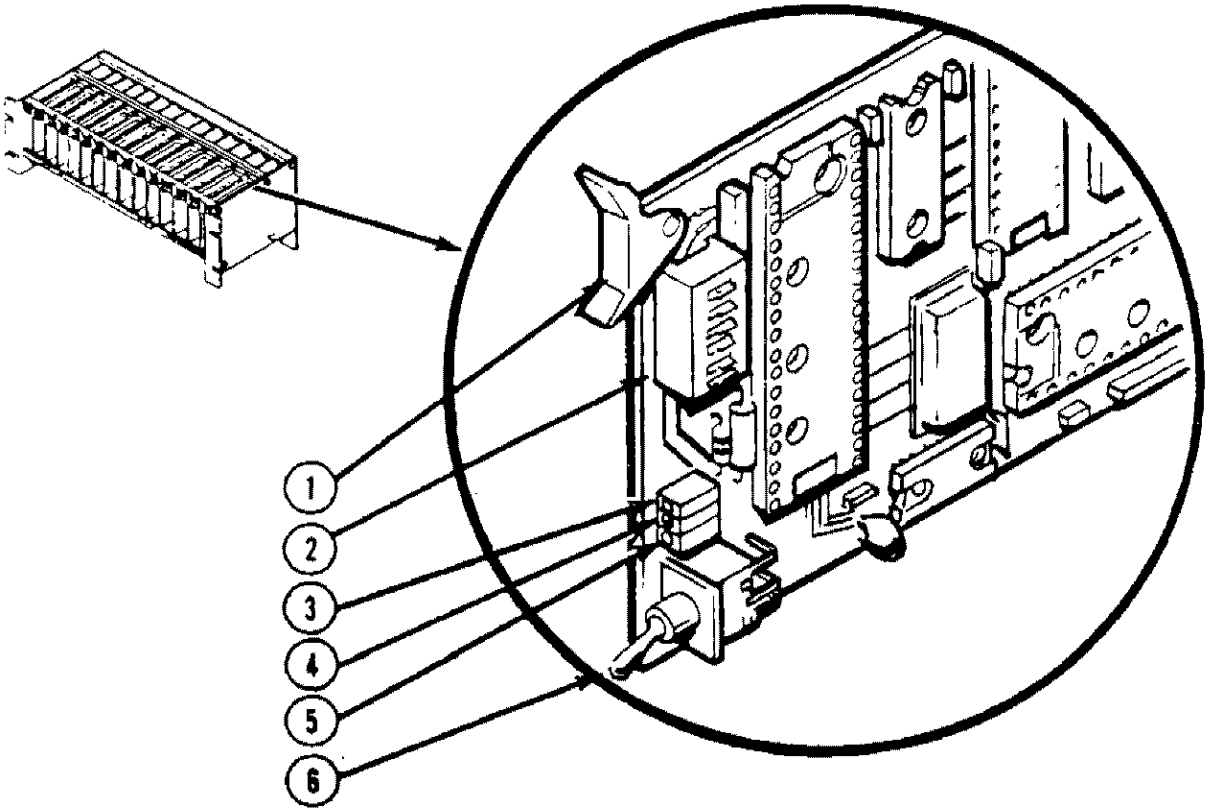
3.2.5 AC Power Distribution Assembly Controls and Indicators

Two ac power distribution assemblies are housed at the bottom level of each CCU, PCU, CCU/CCU, PCU/PCU, and CCU/PCU cabinet assembly. The RCU and RCU Expanded control cabinet assemblies each contain one ac power distribution assembly. Controls for power distribution assemblies are accessed through the back of the control cabinets located in the ARTCC facility and through the front of control cabinets located at the ATCT facility. The power circuit breaker is located on the left side of the assembly and labeled SYSTEM POWER. This switch controls power to the FDIO system control cabinet assembly (if configured with two ac power distribution assemblies, both power circuit breakers must be turned OFF). An adjacent yellow indicator light marked POWER ON will illuminate when system power is ON. The switch at the right of center controls two adjacent maintenance ac power outlets for use in testing equipment. See figure 3-4 for ac power distribution assembly controls and indicators.

3.2.6 DC Power Distribution Assembly Controls and Indicators

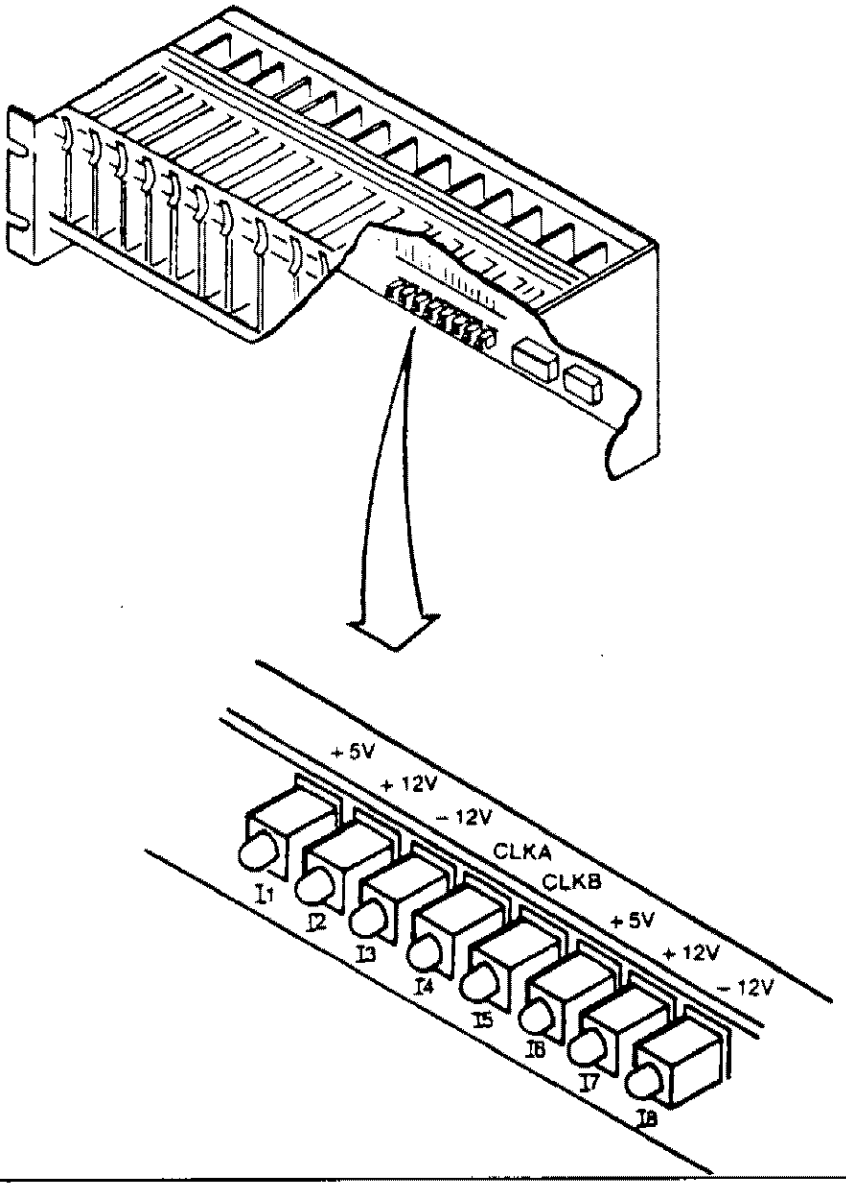
Up to six power distribution assemblies are housed in the control cabinet assemblies. The exact breakdown is: CCU, 3; PCU, 3; CCU/CCU, 6; PCU/PCU, 6; CCU/PCU, 6; RCU, 2; RCU Expanded, 2.

Refer to paragraph 1.3.5.3 for the power supply assembly breakdown within the power distribution assemblies. Controls for power distribution assemblies are accessed through the back of the control cabinets located in the ARTCC facility and through the front of control cabinets located at the ATCT facility. One 2 A circuit breaker is located on each side of the power supply assembly panel at all ARTCC control cabinets. At ATCT sites, the RCU control cabinet has only one circuit breaker located on the left side of the assembly. The RCU Expanded has two power supply assemblies the top assembly has one circuit breaker and the bottom assembly has two. These 2 A circuit breakers control power to the 5 V and +12 V power supplies located inside the assembly. Figure 3-5 shows an example of the dc power distribution assembly controls and indicators for a CCU BC card cage.



CONTROL or INDICATOR	REF DES	FUNCTION
BOARD EJECTOR	1	BOARD RELEASE CLIP
DIP SWITCHES	2	BUS CONNECTOR ADDRESSING
CLOCK A LAMP	3	SHOWS ONLINE
CLOCK B LAMP	4	SHOWS ONLINE
LAN ACQUISITION	5	LAMP ON SHOWS LAN ACQUIRED
TOGGLE SWITCH	6	CONTROLS POWER SUPPLY TO CARD

FIGURE 3-2. BC BOARD ASSEMBLY CONTROLS AND INDICATORS

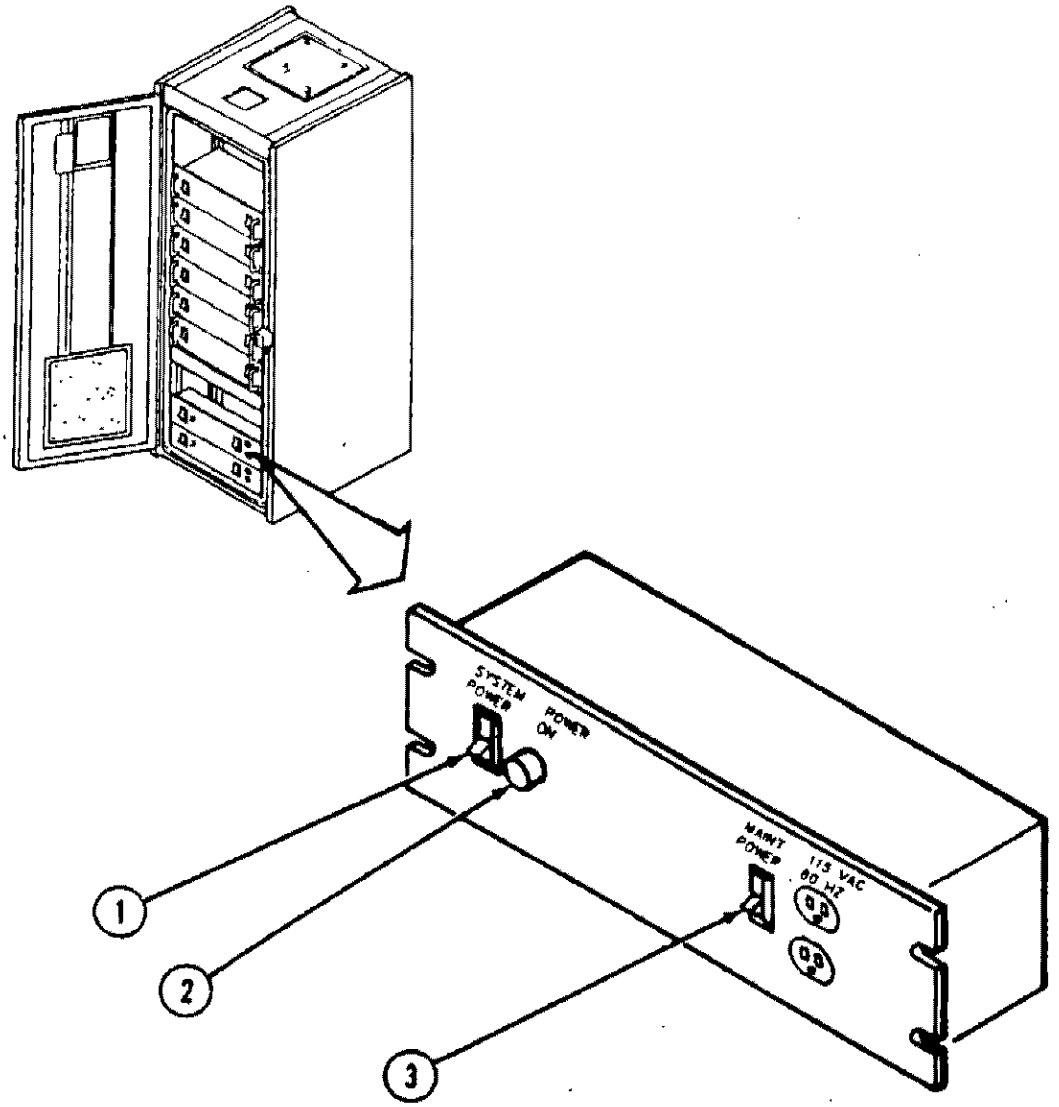


PURPOSE: TO VISUALLY DETERMINE POWER STATUS AVAILABLE TO BUS CONNECTOR CARDS		
INDICATOR LAMPS	I1	+ 5 V POWER SUPPLY
	I2	+12 V POWER SUPPLY
	I3	-12 V POWER SUPPLY
	I4	CLOCK A
	I5	CLOCK B
	I6	+ 5 V POWER SUPPLY
	I7	+12 V POWER SUPPLY
	I8	-12 V POWER SUPPLY

NOTE

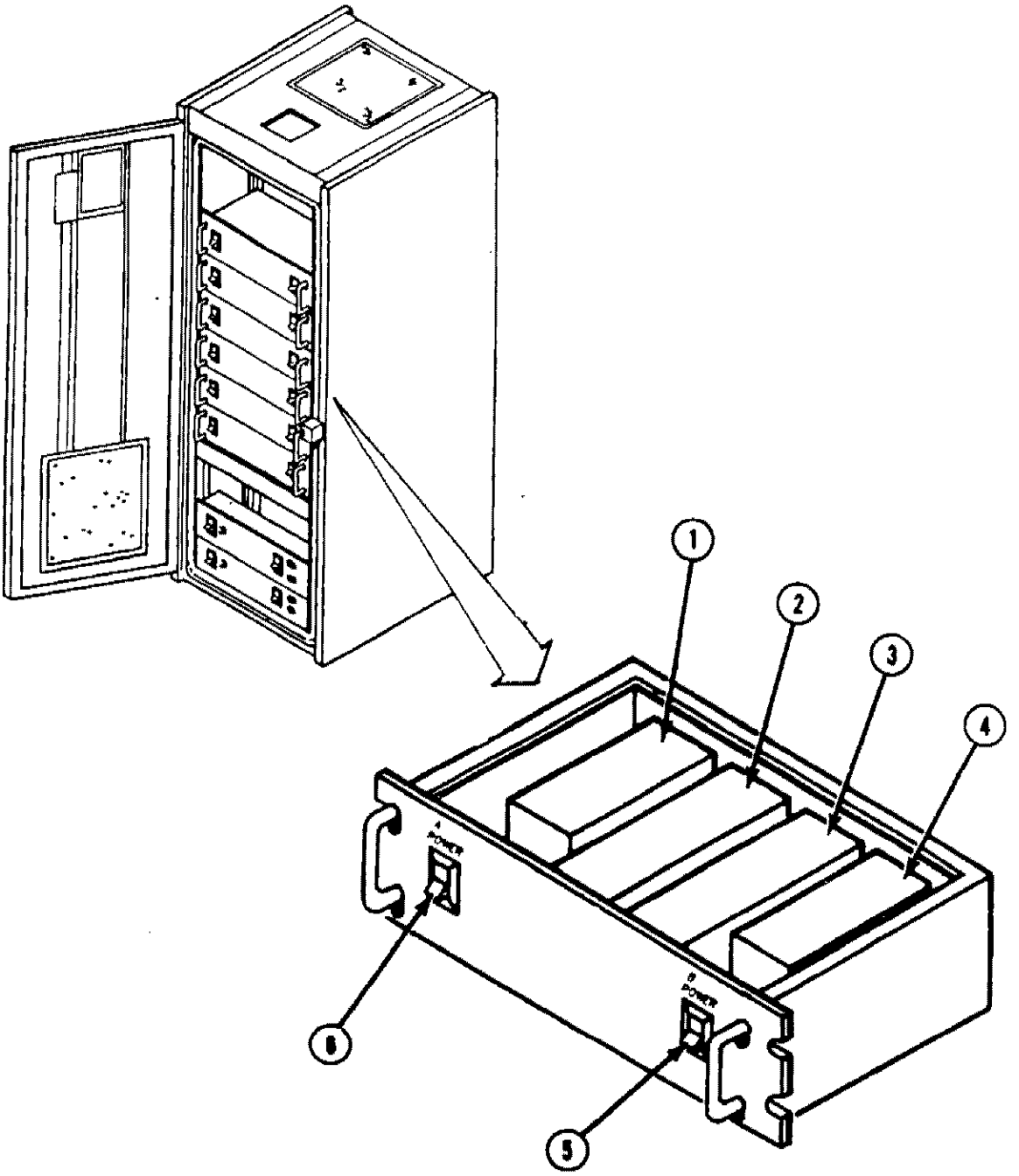
BUS CONNECTOR CARDS ARE TO BE SERVICED BY TECHNICIAN ONLY.
NORMAL OPERATING CONDITION: ON.

FIGURE 3-3. BC BACKPLANE BOARD POWER INDICATORS



CONTROL	REF DES	FUNCTION
SYSTEM POWER	1	POWER CIRCUIT BREAKER FOR AC DISTRIBUTION
POWER ON INDICATOR	2	YELLOW LAMP INDICATES CONTROL UNIT POWER TO SYSTEM IS ON
MAINTENANCE POWER	3	POWER CIRCUIT BREAKER FOR MAINTENANCE OUTLETS

FIGURE 3-4. AC POWER DISTRIBUTION ASSEMBLY CONTROLS AND INDICATORS



1. A1PS1 ±12 V dc POWER SUPPLY ASSEMBLY
2. A1PS2 5 V dc POWER SUPPLY ASSEMBLY
3. A2PS1 5 V dc POWER SUPPLY ASSEMBLY
4. A2PS2 ±12 V dc POWER SUPPLY ASSEMBLY
5. A2CB1 2 AMP CIRCUIT BREAKER
6. A1CB1 2 AMP CIRCUIT BREAKER

FIGURE 3-5. EXAMPLE DC POWER DISTRIBUTION ASSEMBLY CONTROLS AND INDICATORS

3.2.7 RFSP (FA 10095/2) Controls and Indicators

The ON/OFF power switch is located above the ac power cord connector on the back of the RFSP peripheral. The front control panel for the RFSP peripheral element features a green LED power indicator to signal power ON and a four-digit LCD module display area to indicate RFSP status and fault conditions. The printer must be offline to activate the vernier, LF, and test buttons. Three adjacent buttons marked 1, 2, and 3 are for use in configuring the RFSP and are to be used only by a technician.

The display area will signal fault conditions. The FAULT indicator lamp will flash alternately with the display indicating the fault condition. A warning bell will sound twice and the printer will automatically be set offline. The alarm at the Multibus front panel assembly in the cabinet assembly will also sound for any of the fault conditions. The fault error codes are listed in the Flight Strip Printer Operators Manual, Appendix B, Page B-1. See figure 3-6 for RFSP controls and indicators.

3.2.8 RFSP (FA 10095/11) Controls and Indicators

The ON/OFF power switch is located on the right hand side of the RFSP peripheral. The front control panel for the FA 10095/11 peripheral element features a green LED power indicator to signal power ON. The ON LINE LED turns ON to indicate that the printer is online. The LQ LED will always be ON to indicate letter quality mode. The other LEDs are not used in this application. The printer must be offline to activate LF button. Two adjacent buttons marked FONT and CPI are for use in configuring the RFSP and are to be used only by a technician.

The FAULT LED will flash indicating a fault condition. A warning bell will sound three times and the printer will automatically be set offline. The alarm at the Multibus front panel assembly in the cabinet assembly will also sound for any of the fault conditions. See figure 3-7 for RFSP FA 10095/11 controls and indicators.

3.2.9 RFSP (FA 10095/14) Controls and Indicators

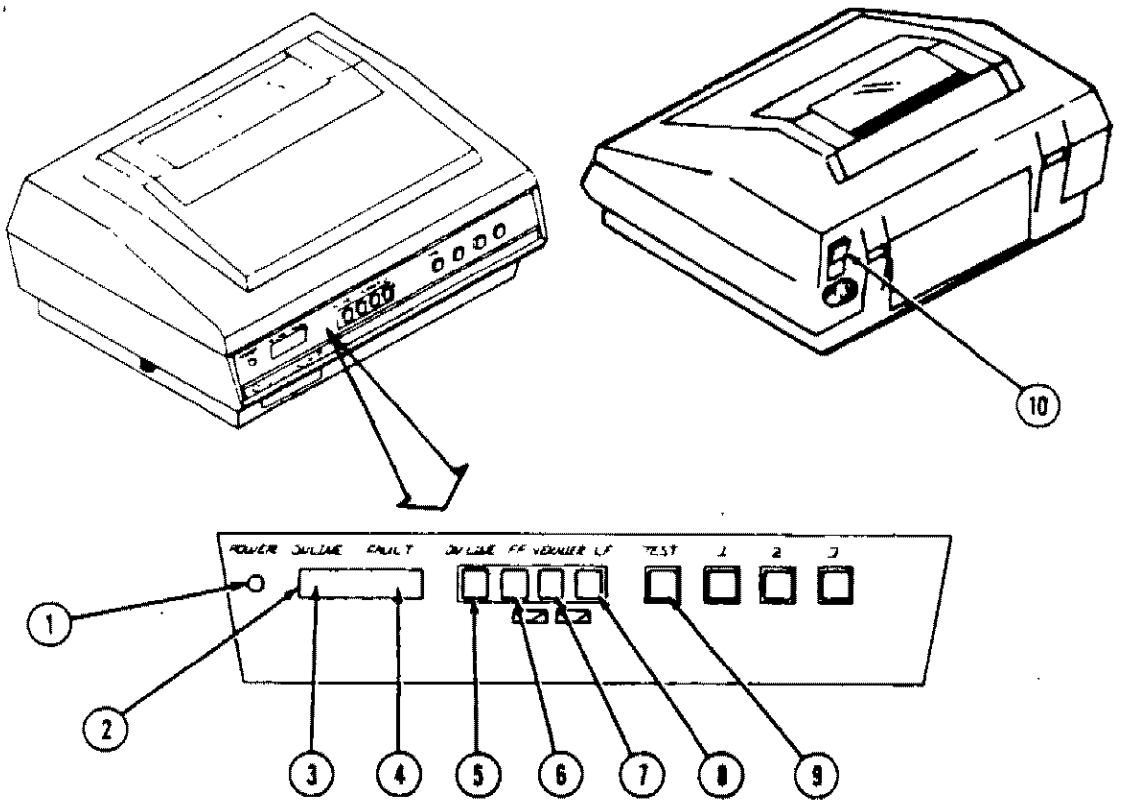
The ON/OFF power switch is located next to the ac power cord connector on the back of the RFSP peripheral. The front control panel for the FA 10095/14 peripheral element features a green LED power indicator to signal power ON. The ON/OFF LED turns ON to indicate that the printer is online. The RECEPTION LED will be ON whenever the printer receives data (flight strip or poll for status).

The ERROR LED will flash indicating a fault condition. A warning bell will sound and the printer will automatically be set offline. The alarm at the Multibus front panel assembly in the cabinet assembly will also sound for any of the fault conditions. See figure 3-8 for RFSP FA 10095/14 controls and indicators.

3.2.10 RANK (FA 10095/3) Controls and Indicators

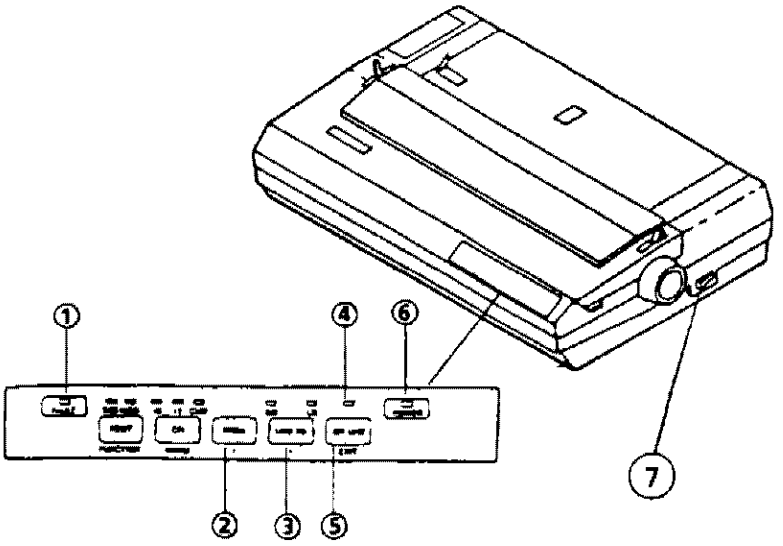
Figure 3-9 illustrates the RANK controls and indicators. The ON/OFF power switch is located on the back of the RANK peripheral element. A control knob located at the upper right on the top panel is used to control keyboard illumination. Increased brightness is obtained by turning the knob clockwise; a built-in stop prevents extinguishing keyboard illumination.

The RANK is designed for composing and editing messages. The keyboard is divided into two basic sections through color: the white section is for message entry, the blue section is for editing messages. There are two exceptions: the green ENTER key and the yellow MWL indicator.



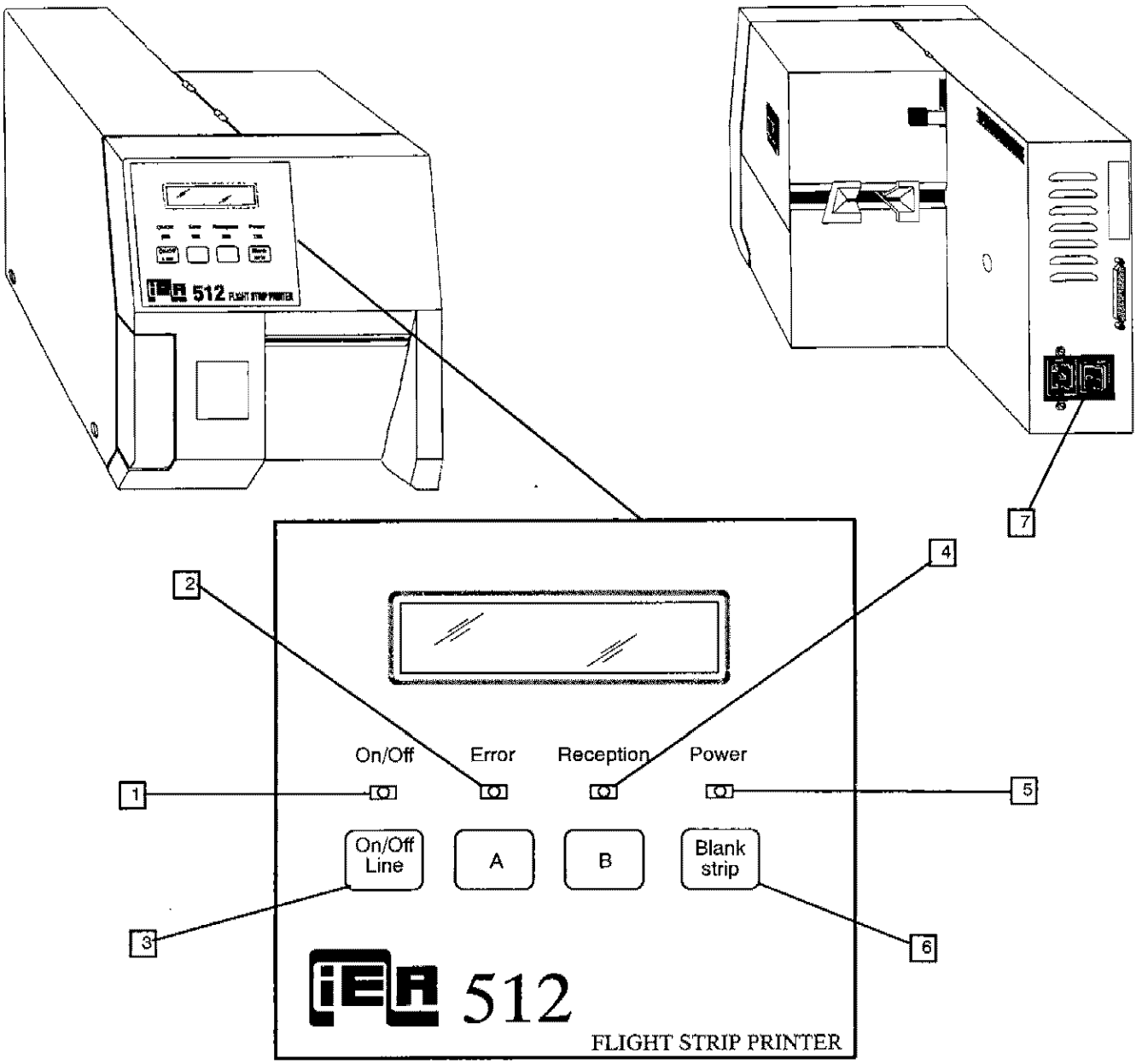
CONTROL INDICATOR	REF DES	FUNCTION
POWER INDICATOR	1	LAMP ILLUMINATES WHILE POWER IS ON
DISPLAY	2	4 SEVEN SEGMENT DIGITS PROVIDE OPERATION MESSAGES, FAULT CODE AND ONLINE STATUS
ONLINE	3	2 UPPER SEGMENTS ON LEFT OF DISPLAY AREA INDICATE ONLINE CONDITION
FAULT	4	2 UPPER SEGMENTS ON RIGHT OF DISPLAY AREA — LAMP FLASHES ALTERNATELY WITH DISPLAY WHEN FAULT CONDITION EXITS
ON/OFFLINE	5	TOGGLES PRINTER ON-OFFLINE MANUALLY
FORMFEED (FF)	6	ADVANCES PAPER TO TEAR POSITION
VERNIER	7	ENABLES LINE ADJUSTMENT
		WHEN PRESSED WITH FORMFEED, PAPER ADVANCES CONTINUOUSLY UNTIL RELEASED. WHEN PRESSED WITH LINEFEED, PAPER RETRACTS UNTIL RELEASED (MUST BE OFFLINE)
		SETS TOP OF FORM
		WHEN PRESSED WITH ONLINE, TOP OF FORM IS SET.
LINEFEED (LF)	8	ADVANCES PAPER ONE LINE (MUST BE OFFLINE)
TEST	9	INITIATED TO TEST PRINTER FUNCTIONALITY (MUST BE OFFLINE TO SELF-TEST)
POWER ON-OFF	10	ROCKER SWITCH CONTROLS PRINTER POWER

FIGURE 3-6. RFSP (FA 10095/2) CONTROLS AND INDICATORS



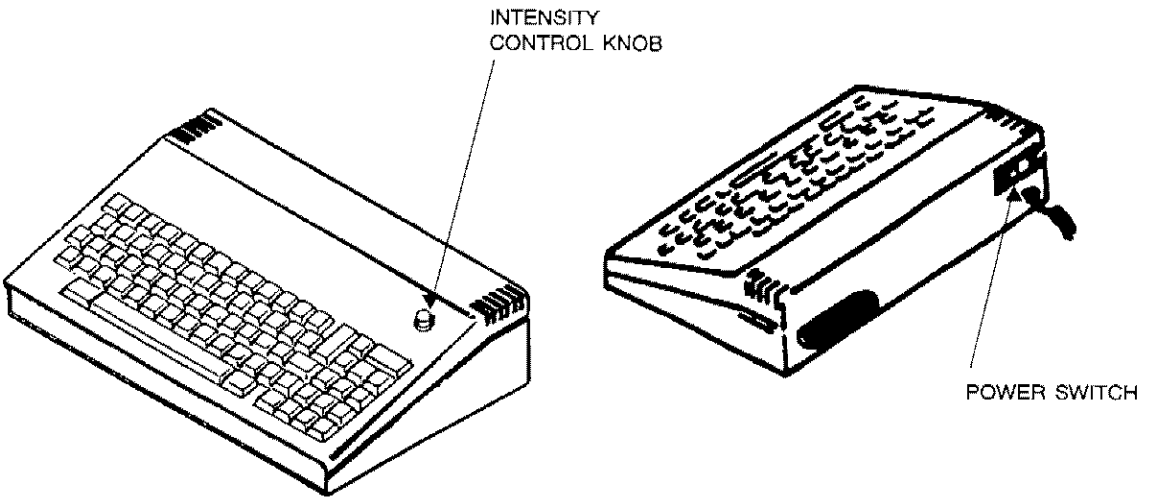
CONTROL INDICATOR	REF DES	FUNCTION
FAULT	1	LAMP WILL FLASH INDICATING FAULT CONDITION
FORMFEED (FF)	2	ADVANCES PAPER TO FIRST PRINT LINE OF NEXT FORM
LINEFEED (LINE FD)	3	ADVANCES PAPER ONE LINE (MUST BE OFFLINE)
ONLINE	4	LAMP ILLUMINATES WHILE ONLINE
ON/OFFLINE	5	TOGGLES PRINTER ON-OFFLINE MANUALLY
POWER INDICATOR	6	LAMP ILLUMINATES WHILE POWER IS ON
POWER ON-OFF	7	SWITCH CONTROLS POWER TO UNIT

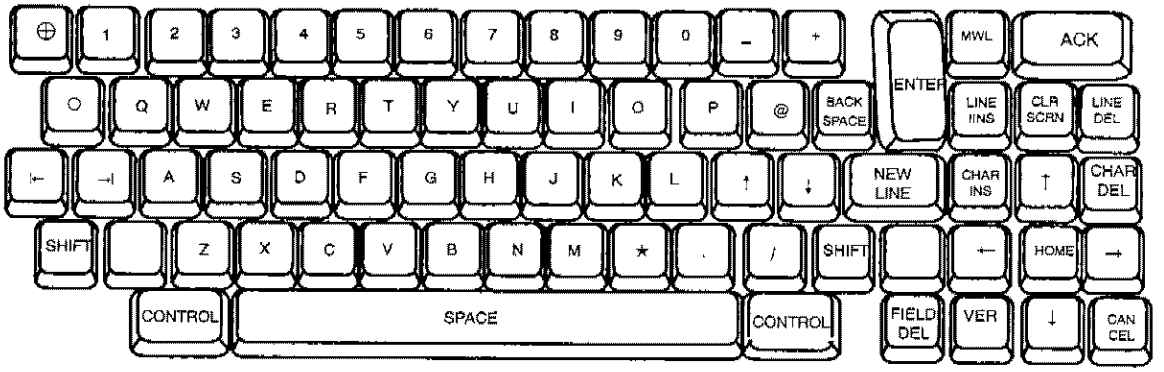
FIGURE 3-7. RFSP (FA 10095/11) CONTROLS AND INDICATORS



CONTROL INDICATOR	REF DES	FUNCTION
ONLINE	1	LAMP ILLUMINATES WHILE ONLINE
ERROR	2	WHEN ON INDICATES MECHANICAL ERROR
		WHEN FLASHING INDICATES ERROR IN RECEPTION OF MESSAGE
ON/OFFLINE	3	TOGGLES PRINTER ON-OFFLINE MANUALLY
RECEPTION	4	WHEN ON INDICATES RECEIVING OF MESSAGE
POWER	5	WHEN ON INDICATES PRINTER IS ON
BLANK STRIP	6	OPTION TO PRINT BLANK STRIP
POWER ON-OFF	7	SWITCH CONTROLS POWER TO UNIT

FIGURE 3-8. RFSP FA 10095/14 CONTROLS AND INDICATORS



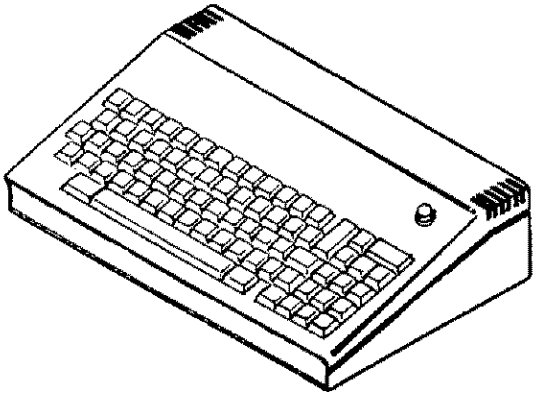


STANDARD TYPEWRITER FORMAT AND USAGE

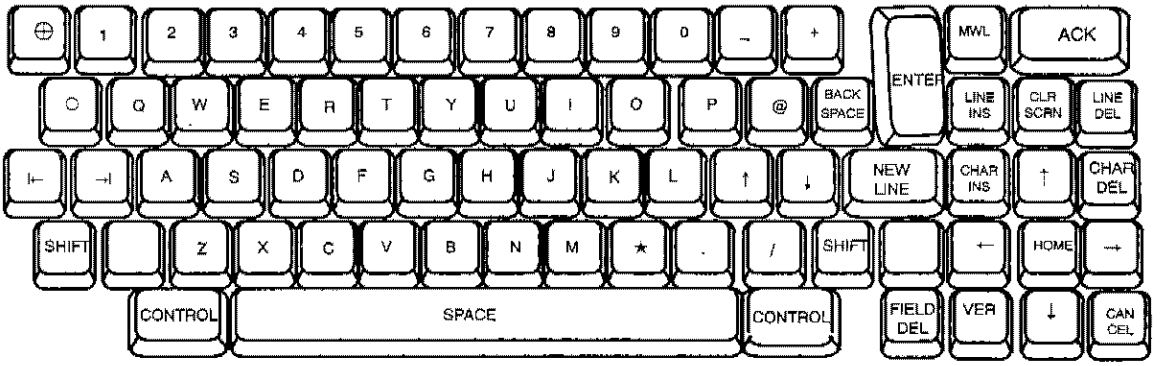
ALL KEYS AND SPACE BAR LIGHTED

ENTER	SENDS COMPLETED MESSAGE AS PRESENTED TO HOST. IF SYSTEM IS IN VERIFY MODE, MESSAGE WILL BE CHECKED PRIOR TO SENDING TO THE HOST.
MWL	MESSAGE WAITING LIGHT FLASHES WHEN A FLIGHT STRIP OR GENERAL INFORMATION MESSAGE FROM HOST IS WAITING TO BE DISPLAYED ON THE CRT; RANK IS UNAVAILABLE DURING THIS TIME.
NEWLINE	CAUSES CURRENT RANK MESSAGE TO BE OUTPUT TO ITS PAIRED PRINTER.

FIGURE 3-9. RANK (FA 10095/3) PERIPHERAL ELEMENT CONTROLS AND INDICATORS (SHEET 1)



WITH THE EXCEPTION OF THE ACKNOWLEDGE KEY, ALL KEYS AFFECT THE COMPOSITION SECTION ONLY



CONTROL	FUNCTION
⊕	SPECIAL CHARACTER INDICATING WEATHER PARTIALLY CLOUDY.
○	SPECIAL CHARACTER INDICATING WEATHER CLEAR.
|←	MOVES CURSOR TO THE BEGINNING OF PREVIOUS FIELD.
→|	MOVES CURSOR TO THE BEGINNING OF NEXT FIELD.
BLANK	NO FUNCTION AT PRESENT — FOR FUTURE USE.
ACK	TO ACKNOWLEDGE A FLIGHT STRIP OR GENERAL INFORMATION MESSAGE SENT TO THE CRT.
LINE INS	INSERTS LINE AT THE CURSOR. BOTTOM LINE IS DELETED.
CLR SCRN	CLEARS MESSAGE ENTRY AREA (SEE CANCEL DESCRIPTION).
LINE DEL	DELETES THE LINE AT THE CURSOR — ALL LINES BELOW CURSOR ARE MOVED UP ONE LINE. A BLANK LINE IS INSERTED AT BOTTOM.
CHAR INS	INSERTS BLANK SPACE AT CURSOR LOCATION (MOVES REMAINDER OF LINE ONE POSITION TO THE RIGHT).
↑	MOVES CURSOR UP ONE LINE.
CHAR DEL	DELETES CHARACTER AT CURSOR LOCATION (MOVES REMAINDER OF LINE ONE POSITION LEFT).
BLANK	NO FUNCTION AT PRESENT — FOR FUTURE USE.
←	MOVES CURSOR ONE POSITION TO THE LEFT.
HOME	MOVES CURSOR TO THE BEGINNING OF THE COMPOSITION AREA.
→	MOVES CURSOR ONE POSITION TO THE RIGHT.
FIELD DEL	DELETES FIELD AT CURSOR POSITION.
VER	TOGGLE SWITCH PUTS SYSTEM INTO VERIFY MODE; MUST BE TOGGLED BEFORE EACH "ENTER" TO ACTIVATE.
↓	MOVES CURSOR DOWN ONE LINE.
CANCEL	CANCELS ENTIRE ENTRY AND CLEARS MSG ENTRY AREA. RETURNS SYSTEM TO NON-VERIFY.

NOTE: CONTROL FUNCTIONS ALWAYS CONSTANT — NOT AFFECTED BY DEPRESSING SHIFT OR CONTROL KEYS

FIGURE 3-9. RANK (FA 10095/3) PERIPHERAL ELEMENT CONTROLS AND INDICATORS (SHEET 2 — END)

3.2.11 RANK (FA 10095/17) Controls and Indicators

Figure 3-10 illustrates the RANK controls and indicators. The ON/OFF power switch is located on the back of the RANK peripheral element. The DIM/BRIGHT keys located at the upper right on the keypad are used to control keyboard illumination. Increased brightness is obtained by pressing the BRIGHT key.

The RANK is designed for composing and editing messages. The keyboard is divided into three basic sections by functions: the alphanumeric section is for message entry, the keypad to the far right is for editing messages, and the top line of function keys will be defined at a later time.

3.2.12 CRT (FA 10095/4) Controls and Indicators

The power ON/OFF switch is located at the left front of the CRT peripheral element. When the CRT is initially powered up, an audible tone will momentarily sound. Controls located on the front right side undercarriage are used to adjust screen brightness and contrast. See figure 3-11 for CRT control locations.

3.2.13 CRT (FA 10095/12) Controls and Indicators

The power ON/OFF switch is located at the left front of the CRT peripheral unit. When the CRT is initially powered up, an audible tone will momentarily sound. Controls located on the right side are used to adjust screen brightness and contrast. See figure 3-12 for CRT control locations.

3.2.14 CRT (FA 10095/18) Controls and Indicators

The power ON/OFF switch is located at the right front of the CRT peripheral unit. When the CRT is initially powered up, an audible tone will momentarily sound. Controls located on the right side undercarriage are used to adjust screen brightness and contrast. See Figure 3-12A, CRT (FA 10095/18) Peripheral Element Controls, for CRT control locations.

3.3 TURN ON AND CHECKOUT

3.3.1 Determine Control Cabinet Configuration

The control cabinet assembly layout is denoted on the identification marker board mounted on the access doors of the control cabinet assembly. See figure 3-13 for marker board location.

3.3.2 Cabinet Assembly Power Switches

Power switches for CCU and PCU cabinet assemblies at the ARTCC are accessed through the back section of the cabinet. Each primary-secondary pair of Multibus front panel assemblies has its power supply combined in a Multibus power supply assembly with individual power switches for each Multibus unit. At the ATCT remote sites, power switches for the RCU cabinet assembly are accessed through the front section of the cabinet. RCU and RCU Expanded cabinet assemblies have one Multibus power supply assembly with one power switch.

All CCU and PCU BC power supply assemblies have two dedicated power supply switches to control ON/OFF operation. The RCU configuration has one BC power supply switch. The RCU Expanded configuration combines the BC power supplies for both card cage assemblies (as in the CCU and PCU configurations) and uses two switches. Each cabinet assembly has at least one ac power distribution assembly at the bottom level of the hardware cabinet. Each ac power distribution assembly has a power switch on the left side to control all incoming ac power to the cabinet assembly. The switch

at center right controls the two adjacent maintenance outlets. Power switch locations are shown in Figure 3-14, FDIO Control Cabinet Assembly Power-Up Procedures.

3.3.3 BC Board Power Switches

As stated in paragraph 3.2.3, system installers will turn ON the power to individual BC boards. The power supply to each board is easily verified by checking the lights immediately above the power toggle switch (refer to figure 3-2).

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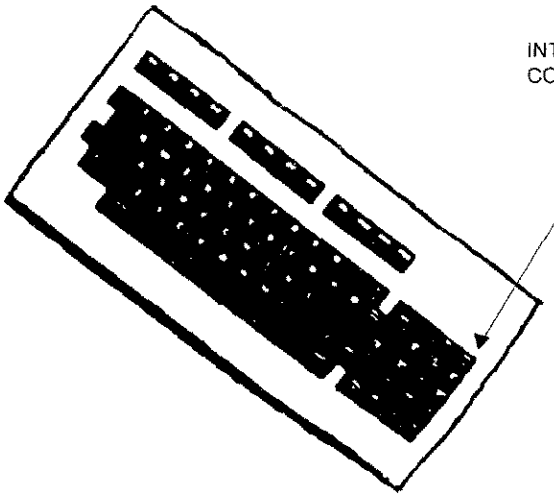
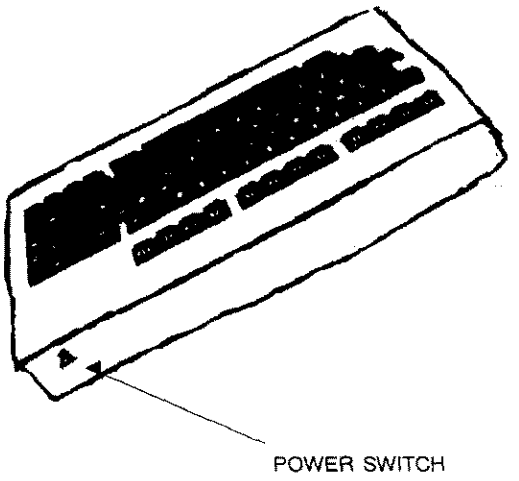
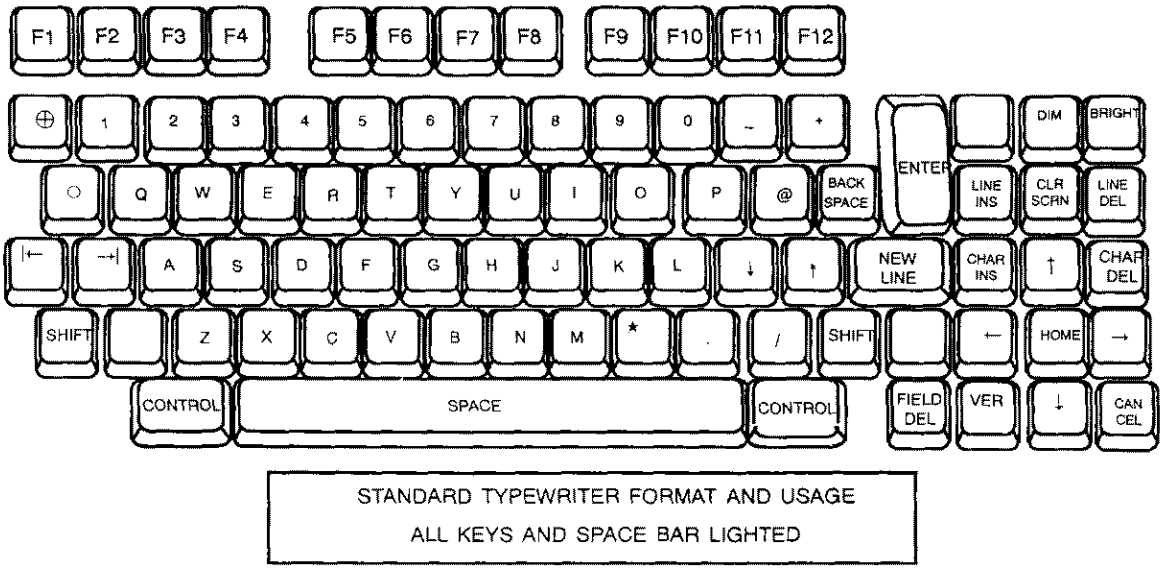


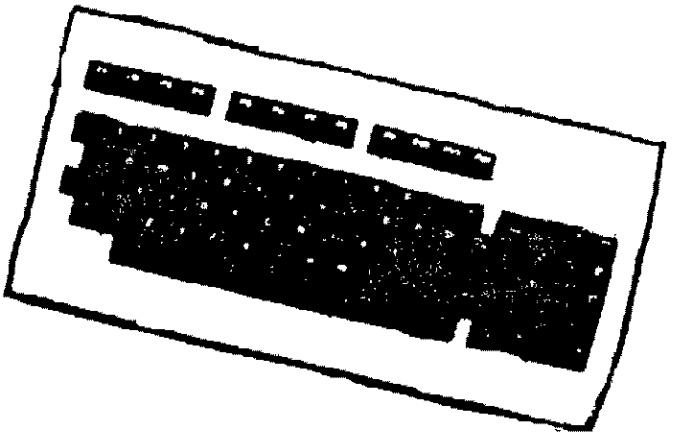


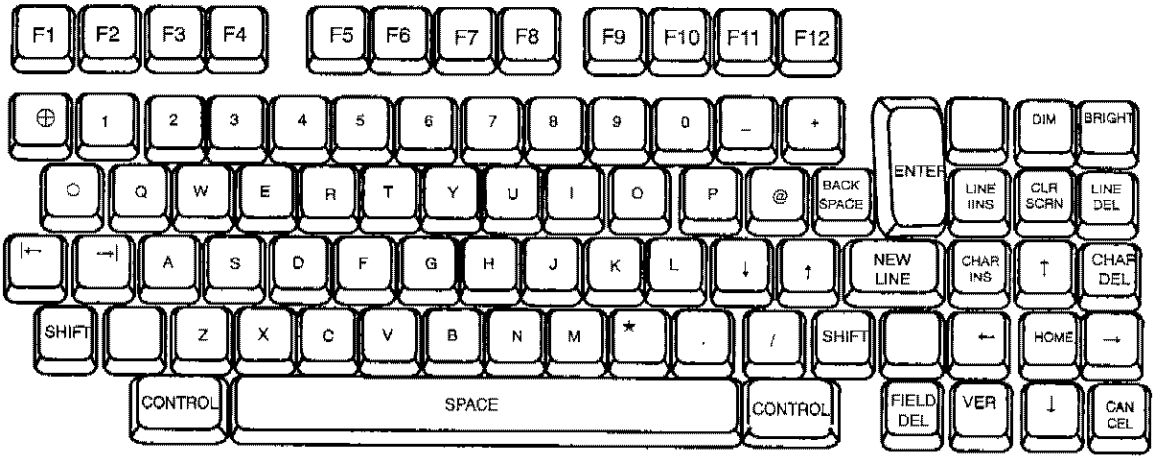


STANDARD TYPEWRITER FORMAT AND USAGE
ALL KEYS AND SPACE BAR LIGHTED

ENTER	SENDS COMPLETED MESSAGE AS PRESENTED TO HOST. IF SYSTEM IS IN VERIFY MODE, MESSAGE WILL BE CHECKED PRIOR TO SENDING TO THE HOST.
NEWLINE	CAUSES CURRENT RANK MESSAGE TO BE OUTPUT TO ITS PAIRED PRINTER.
FUNCTION (F1-F12)	NO FUNCTION AT PRESENT — FOR FUTURE USE.

FIGURE 3-10. RANK (FA 10095/17) PERIPHERAL ELEMENT CONTROLS AND INDICATORS (SHEET 1)

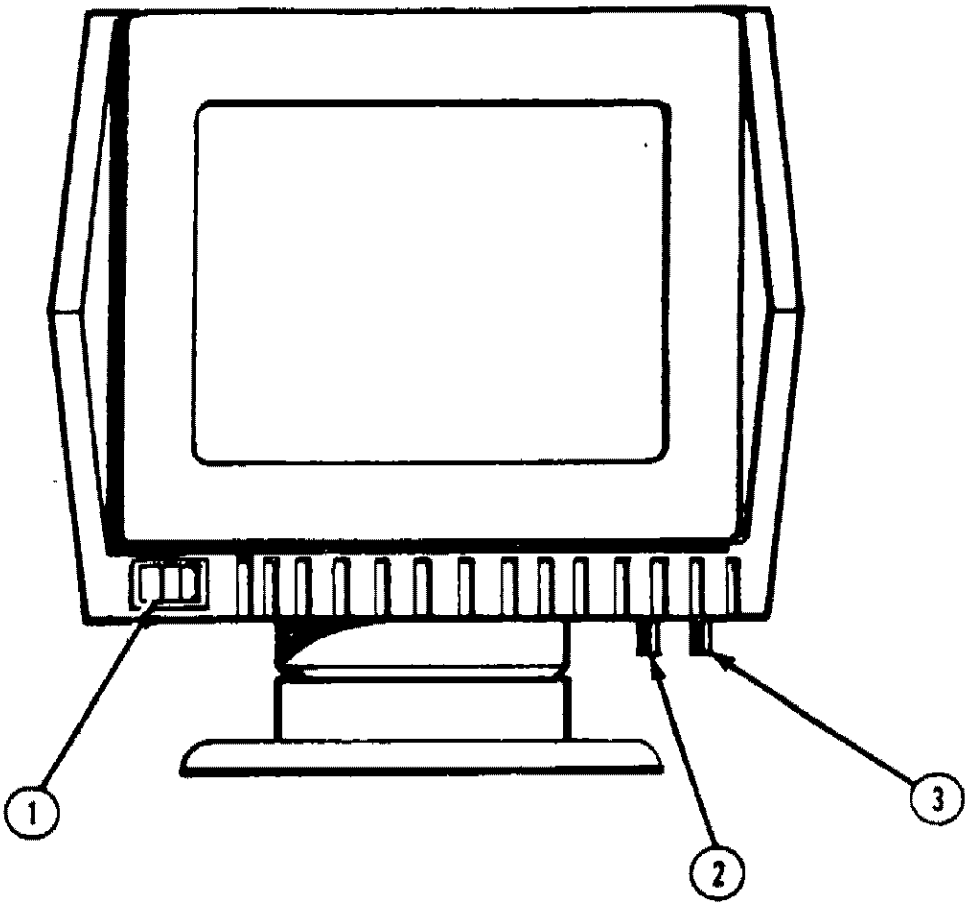




CONTROL	FUNCTION
⊕	SPECIAL CHARACTER INDICATING WEATHER PARTIALLY CLOUDY.
○	SPECIAL CHARACTER INDICATING WEATHER CLEAR.
|←	MOVES CURSOR TO THE BEGINNING OF PREVIOUS FIELD.
→|	MOVES CURSOR TO THE BEGINNING OF NEXT FIELD.
BLANK	NO FUNCTION AT PRESENT — FOR FUTURE USE.
DIM/BRIGHT	ADJUSTS BRIGHTNESS OF KEY CHARACTERS.
LINE INS	INSERTS LINE AT THE CURSOR. BOTTOM LINE IS DELETED.
CLR SCRN	CLEARS MESSAGE ENTRY AREA (SEE CANCEL DESCRIPTION).
LINE DEL	DELETES THE LINE AT THE CURSOR — ALL LINES BELOW CURSOR ARE MOVED UP ONE LINE, A BLANK LINE IS INSERTED AT BOTTOM.
CHAR INS	INSERTS BLANK SPACE AT CURSOR LOCATION (MOVES REMAINDER OF LINE ONE POSITION TO THE RIGHT).
↑	MOVES CURSOR UP ONE LINE.
CHAR DEL	DELETES CHARACTER AT CURSOR LOCATION (MOVES REMAINDER OF LINE ONE POSITION LEFT).
BLANK	NO FUNCTION AT PRESENT — FOR FUTURE USE.
←	MOVES CURSOR ONE POSITION TO THE LEFT.
HOME	MOVES CURSOR TO THE BEGINNING OF THE COMPOSITION AREA.
→	MOVES CURSOR ONE POSITION TO THE RIGHT.
FIELD DEL	DELETES FIELD AT CURSOR POSITION.
VER	TOGGLE SWITCH PUTS SYSTEM INTO VERIFY MODE; MUST BE TOGGLED BEFORE EACH "ENTER" TO ACTIVATE.
↓	MOVES CURSOR DOWN ONE LINE.
CANCEL	CANCELS ENTIRE ENTRY AND CLEARS MSG ENTRY AREA. RETURNS SYSTEM TO NON-VERIFY.

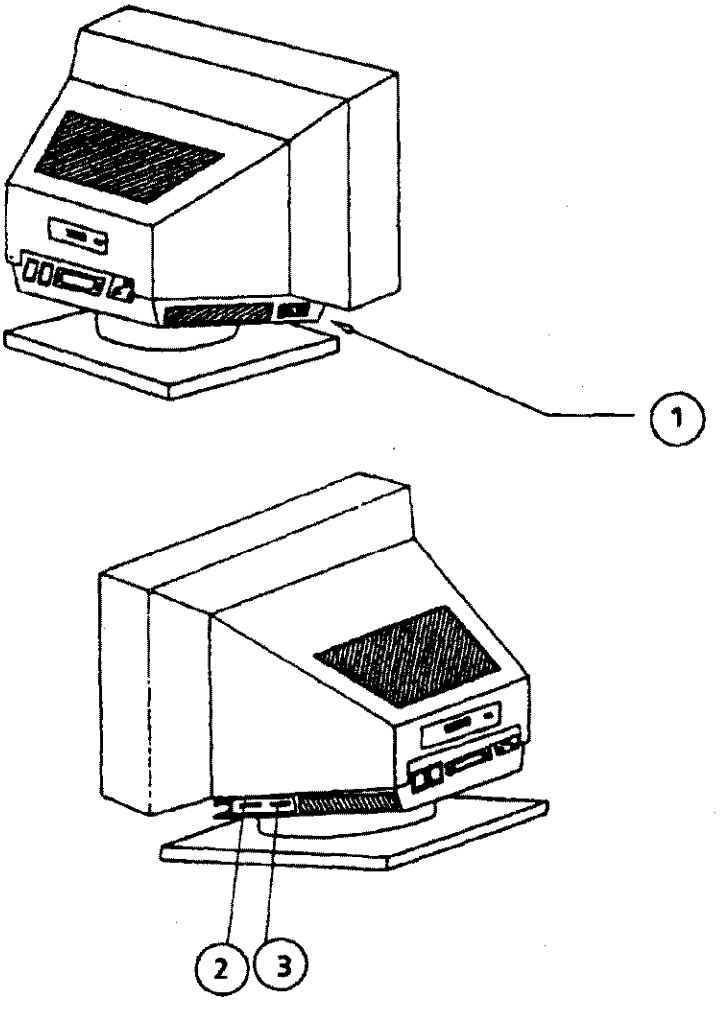
NOTE: CONTROL FUNCTIONS ALWAYS CONSTANT — NOT AFFECTED BY DEPRESSING SHIFT OR CONTROL KEYS.

FIGURE 3-10. RANK (FA 10095/17) PERIPHERAL ELEMENT CONTROLS AND INDICATORS (SHEET 2 — END)



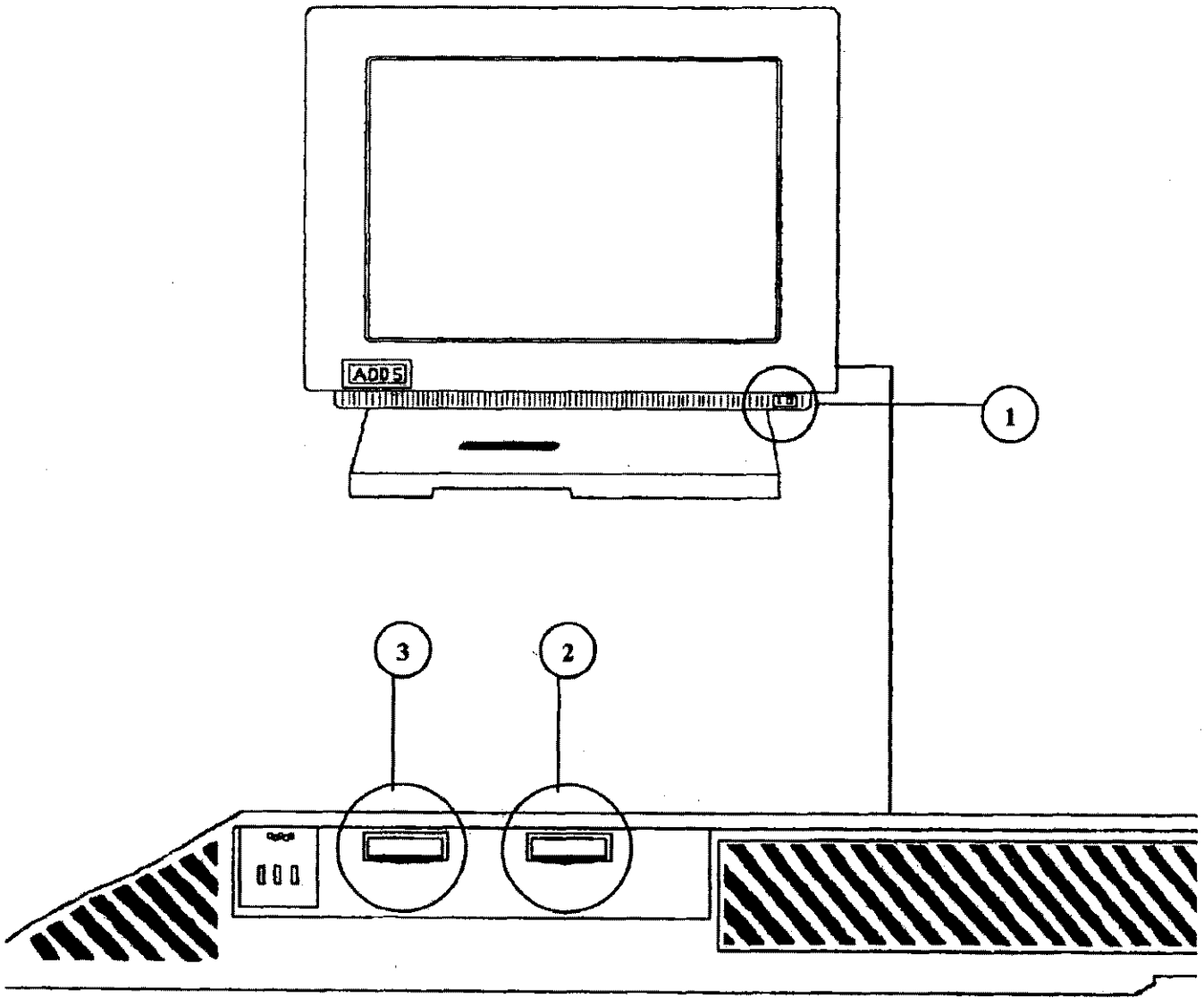
CONTROL	REF DES	FUNCTION
POWER ON-OFF	1	CIRCUIT BREAKER CONTROLS POWER TO UNIT
CONTRAST	2	VARIABLE RESISTOR KNOB CONTROLS SCREEN INTENSITY
BRIGHTNESS	3	VARIABLE RESISTOR KNOB CONTROLS SCREEN BRIGHTNESS

FIGURE 3-11. CRT (FA 10095/4) PERIPHERAL ELEMENT CONTROLS



CONTROL	REF DES	FUNCTION
POWER ON-OFF	1	CIRCUIT BREAKER CONTROLS POWER TO UNIT
CONTRAST	2	DUAL CONTROLS SCREEN INTENSITY
BRIGHTNESS	3	DUAL CONTROLS SCREEN BRIGHTNESS

FIGURE 3-12. CRT (FA 10095/12) PERIPHERAL ELEMENT CONTROLS



CONTROL	REF DES	FUNCTION
POWER ON-OFF	1	CIRCUIT BREAKER CONTROLS POWER TO UNIT
CONTRAST	2	VARIABLE RESISTOR KNOB CONTROLS SCREEN INTENSITY
BRIGHTNESS	3	VARIABLE RESISTOR KNOB CONTROLS SCREEN BRIGHTNESS

FIGURE 3-12A. CRT (FA 10095/18) PERIPHERAL ELEMENT CONTROLS

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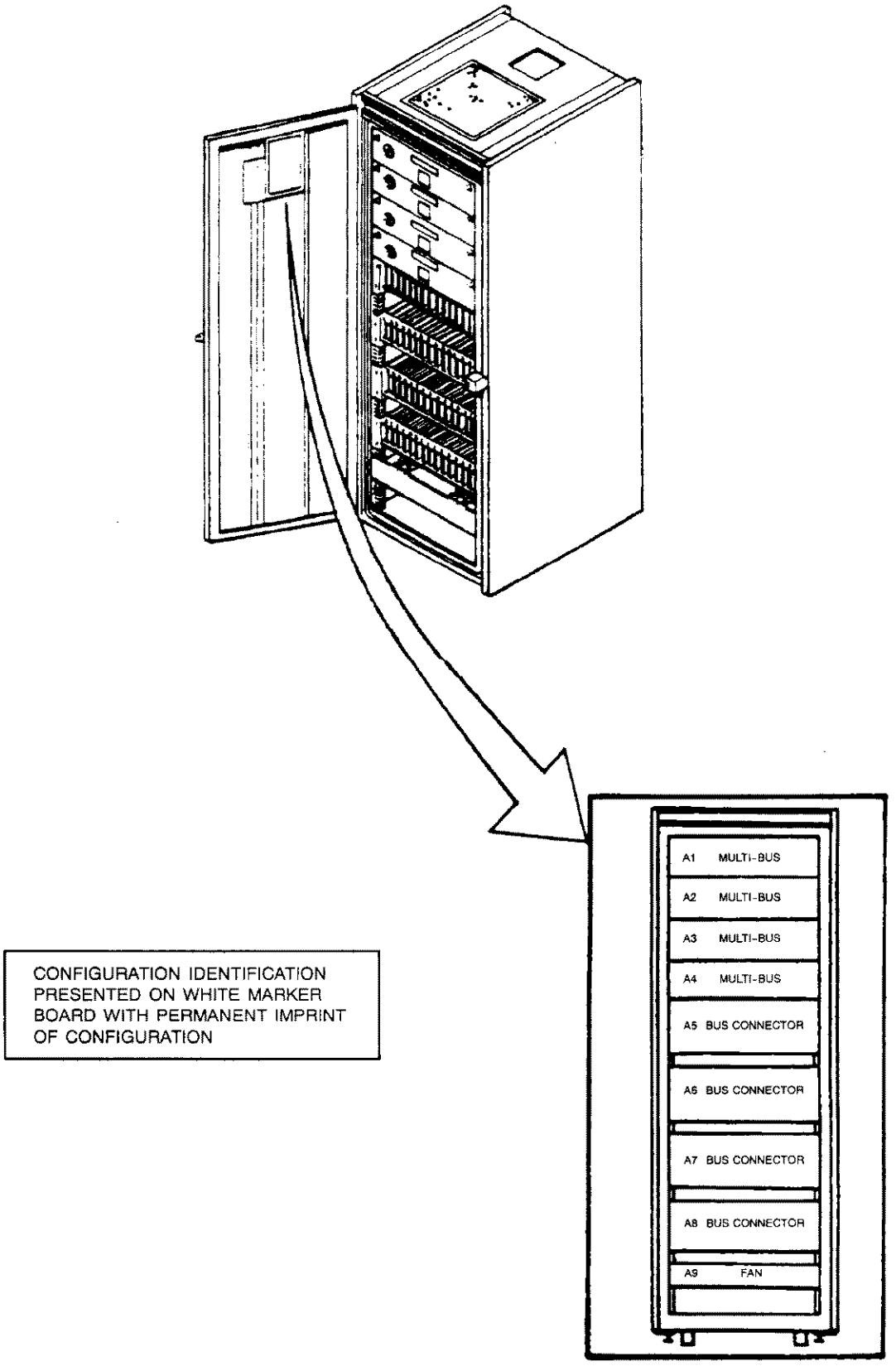

FIGURE 3-13. MARKER BOARD LOCATION AND EXAMPLE CONFIGURATION DESCRIPTION

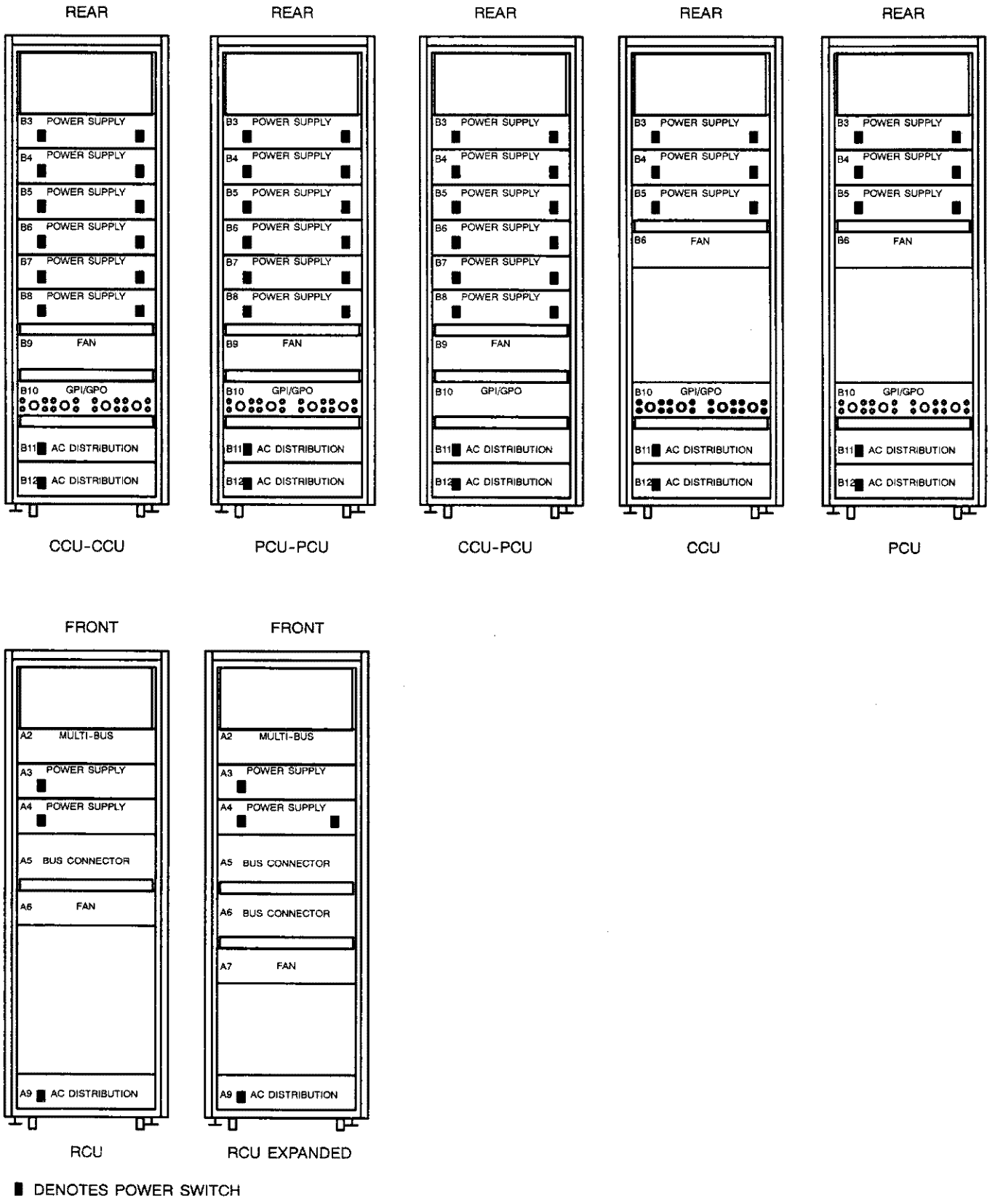

FIGURE 3-14. FDIO CONTROL CABINET ASSEMBLY POWER-UP PROCEDURES

3.3.4 Peripheral Power Switches

All peripherals have power ON/OFF switches: the CRT (FA 10095/4) power switch is located at the unit front on the left, the CRT (FA 10095/12) power switch is located on the left side of the unit, the CRT (FA 10095/18) power switch is located on the front right side of the unit, the RANK power switch is located on the back of the unit, the RFSP (FA 10095/2) power switch is located above the ac power cord connector on the back of the unit, the RFSP (FA 10095/11) is located on the right side of the unit and RFSP (FA 10095/14) is located next to the ac power cord connector on the back of the unit. Power switch locations are shown in Figure 3-15, FDIO Peripheral Power Switch Locations.

3.3.5 FDIO System Power Up

The procedures for power-up assume that all control cabinet assemblies and peripheral elements are set to OFF. Power up begins at the control cabinet assemblies. At the ARTCC locations, CCU or PCU ac power distribution assemblies are turned on first, followed by Multibus power supply assemblies, BC power supply assemblies, and RFSP peripheral elements. At the ATCT remote sites, the RCU ac power distribution assembly is powered up first, followed by the Multibus power supply assembly, the BC power supply assembly(s), and RFSP, RANK, and CRT peripheral elements. Fan assemblies turn on with the ac power distribution assembly.

At power up, all control elements perform initialization diagnostics (procedure requires approximately 1 minute) and are then ready for operation. Front panel will indicate system status.

CRTs and RANKs will be operational with no appreciable time delay. RFSPs will be operational after the units are placed online.

3.3.5.1 Multibus Front Panel Assembly Checkout. The Multibus front panel firmware is made up of a group of commands which exist in the primary and secondary control elements in CCU or PCU combinations and in the RCU (which operates as a primary only). It is through this firmware that technicians communicate with the FDIO system.

The Multibus front panel assembly entry keypad enables the technician, through firmware, to interface with the DIAG and RECN tasks, query system status, control the status of PRI/SEC, and acknowledge system errors. DIAG operations and system status are discussed in section 7.0. RECN is discussed in paragraphs 3.4.6.2 and 3.4.6.5. Primary and secondary hardware switching is discussed in paragraph 3.4.6.1, and acknowledgment of system errors is discussed in paragraph 3.4.4. Under normal conditions, the Multibus front panel assembly requires no operator intervention.

The Multibus front panel hardware is divided into two sections: LCD module display, and keypad. Communication with the Multibus front panel assembly is straightforward. As soon as a button is pressed on the keypad, the Multibus front panel firmware decodes the signal. Refer to figure 3-1 for functions available at the keypad.

The Multibus front panel assembly message buffer has a capacity for 10 error messages. When the buffer is at capacity, a new message will overwrite the oldest message in the buffer. The technician must acknowledge messages displayed on the front panel prior to selecting any front panel function. Refer to paragraph 3.4.4 for the procedure to clear the message buffer.

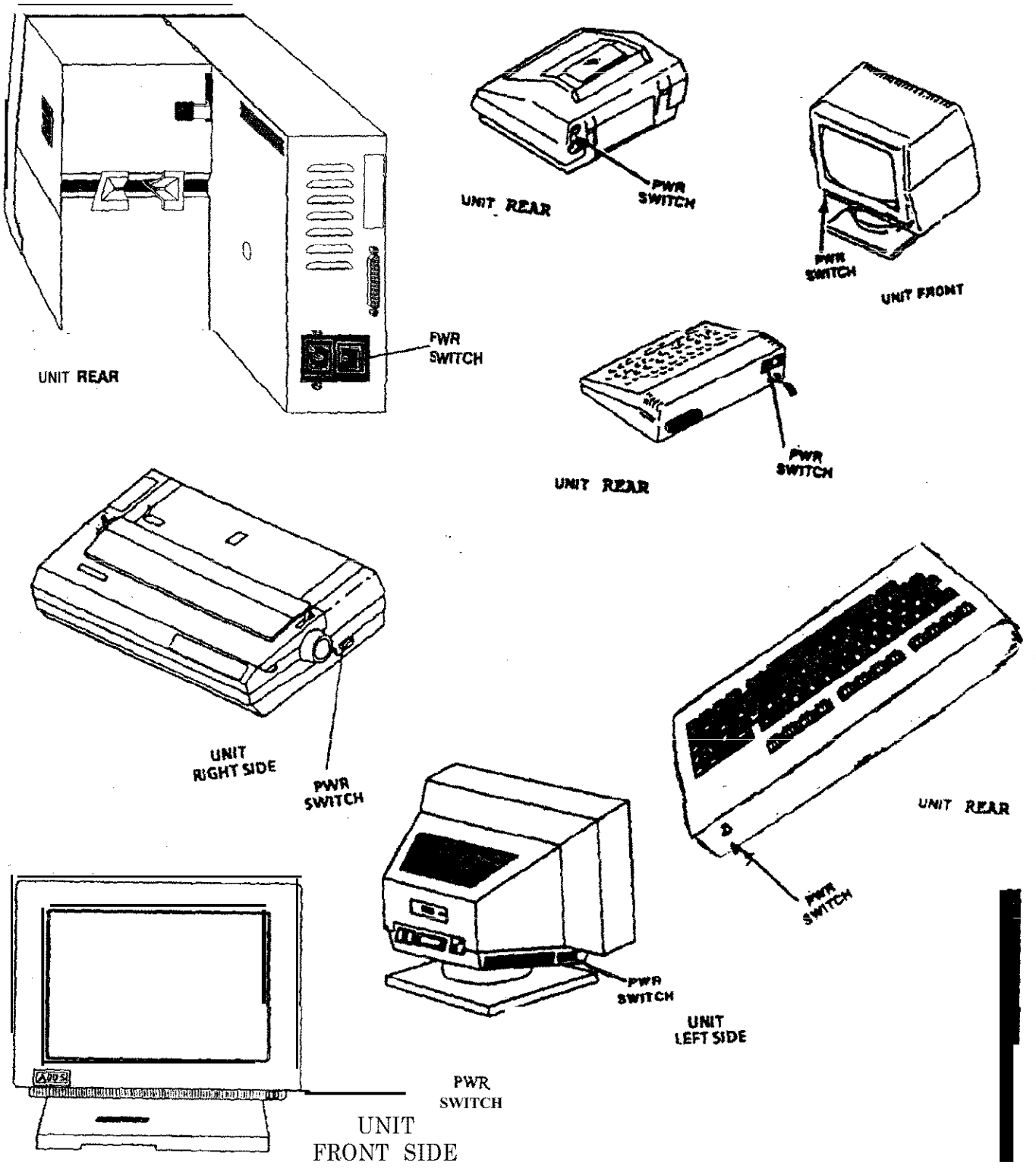

FIGURE 3-15. FDIO PERIPHERAL POWER SWITCH LOCATIONS

3.3.6 RFSP Turn ON and Checkout

The RFSP peripheral element is a 71 -column dot matrix printer with near letter quality printing. Procedures for Turn On and Checkout for FA 10095/2 are described in M2501010. Procedures for Turn On and Checkout for FA 10095/11 are described in 291814-001. Procedures for Turn On and Checkout for FA 10095/14 are described in section 3.3.6.10 of this manual. In the online condition, the peripheral is fully independent, receiving input from either the Host or the RANK and requires very little operator intervention.

At the ARTCC, the RFSP peripheral element receives input from the Host through the PCU control element. At remote site locations the communication path is from the Host through the CCU control element, through the modems, and into the RCU control element.

RFSP peripheral elements print flight strip data, pertinent flight information for the controllers, composed FDIO messages, and, if assigned as an error logger, error messages. The RFSP has a green LED power indicator to signal power ON. ON LINE and FAULT lamps are located at the top two segments of the front control panel display area. ON LINE signals the printer is available for communication with the Host or its paired RANK. FAULT blinks in conjunction with an audible warning sequence to signal a condition requiring operator attention. A light strip in the printer cover insert is provided for flight strip illumination only on the FA 10095/2.

3.3.6.1 RFSP Pairing and Backup. At ARTCCs, RFSP peripheral elements may have up to two RFSP backups (because RANK peripherals are not available at ARTCCs, pairing is not required). At ATCT sites, RFSPs have only one backup, another RFSP or a CRT RFSPs have pairing capability with RANKs at ATCT sites. The RFSP will always be the backup device for a CRT paired with a RANK. Refer to paragraph 3.4.6.5 for RCU RECN procedures.

3.3.6.2 RFSP Initial and Diagnostic Tests. When power is applied, the RFSP resets and runs a diagnostic test to verify that RAM read-write and ROM read operations are being performed without error. After this test, the operator must set top-of-form and switch the RFSP to online mode. When the RFSP is online and not accepting messages, proper operation is continually verified by Built-In Test Equipment (BITE).

3.3.6.3 RFSP Self-Test Procedure. The RFSP element may be self-tested. The RFSP must be physically disconnected from the control unit prior to running the self-test procedures. The procedures for FA 10095/2 are detailed in M2501010 section 3.7, procedures for FA 10095/1 1 are detailed in 291814-001 section 3.7, self test for 10095/14 is executed upon power up of the printer.

3.3.6.4 RFSP Fault Conditions. If a RFSP fault condition exists in an FA 10095/2, the FAULT lamp will flash alternately with the error code in the display area until the error is corrected, at which time the printer can be brought back online. For detailed information, refer to M2501010, section 4 and M2501010T, section 3. In an FA 10095/1 1 a fault condition may cause the FAULT lamp to flash or it may be on steady. Refer to 291814-001, section 8 for detailed information. In an FA 10095/14 a fault condition will cause the ERROR lamp to flash.

NOTE

RFSP (10095/14) may loose parameters that were saved in dynamic RAM. This happens when the printer is stored for long periods of time without being powered up. If this happens the following messages will appear when the printer is powered up:

bAD+rEAD followed by **PARAMETER RESET Press RESET.....** The following procedures will restore the lost parameters:

1. Press the **A** key (key below the ERROR lamp). The printer will cycle through its print head test and then go online.

2. Follow procedures in paragraphs 3.3.6.6 and 3.3.6.7 to reset the highlighting method, printer cut position, and horizontal print position parameters.

3.3.6.5 **RFSP Operator Maintenance.** Periodic maintenance will be performed by trained personnel. **FDIO** equipment may be taken offline as necessary for repair without reconfiguring the system (backup designations have previously been established by the Host [PCU] or EEPROM [RCU]). Detailed procedures may be found for FA **10095/2** in **M2501010,** sections 3 and 5, for FA **10095/11** refer to 291814-001, sections 2, 3, and 7, and for FA **10095/1** 4 refer to section 7.4 of this manual for related maintenance functions performed by the operator.

3.3.6.6 **RFSP (10095/14) Highlighting Adjustment Procedures.** Use the following 13 procedures and figure 7-35 to change the method of highlighting used by the IER Thermal Flight Strip Printer:

NOTE

If the user feels that they have accidentally changed any parameters during these procedures and would like to exit and cancel any changes that may have been made press the **On/Off Line** key twice. If no parameters were changed then the printer will exit out of configuration mode and will display **IER 512 OFF-LINE.** If parameters were changed the display will show the **VALIDATION? NO** prompt. Press the **On/Off Line** key again to exit and cancel any changes that might have been made.

1. Power ON printer.

2. After printer finishes its self-test cycle, load paper stock. This procedure can not be accomplished without paper loaded into the printer.

3. Press the **On/Off Line** key to select the Off Line mode. Allow alarm to stop.

4. Enter the configuration menu of the printer by pressing the front panel keys in the following order: **B — A — Blank Strip — B** (six times). Refer to figure 7-35 for the layout of the front panel keys.

NOTE

Do not pause for longer than 1 second between entering the **Blank Strip** key and the six successive **B** keys or the printer will enter one of the other test modes, i.e., printing of configuration strip, or printing one of the test documents.

5. After a short delay the display will read **PASSWORD? 00000.**

6. Press the **On/Off Line** key.

7. The display area shall display **EMULATION parameters.** Enter the **INTERNAL PARAMETERS MENU** by pressing the **A** key three times.

8. The display area will read **INTERNAL parameters.** Press the **B** key 5 times. The display will now read **Reverse Video?X. X** represents the current highlighting method: 0 for reverse video, 1 for dark gray shading, and 2 for light gray shading.

9. Use the **Blank Strip** key to change the highlighting method.

10. Once the desired highlighted method is selected, press the **On/Off Line** key twice.

11. The display shall read **VALIDATION? NO.** Press the **Blank Strip** key to save this change.

NOTE

If the parameter was not modified the printer will exit out of the configuration mode and display **IER 512 OFF-LINE.**

12. If the parameter was modified the display will read **VALIDATION PERMANENT.** Press the **On/Off Line** key to exit.

13. To view the new highlighting method on a test flight strip press the front panel keys in the following order: **B — A — Blank Strip — B** (5 times).

3.3.6.7 RFSP (10095/1 4) Printing Parameters Adjustment Procedures. Use the following 15 procedures and figure **7-35** to adjust cut position and to adjust print both horizontally and vertically on the IER thermal flight strip printer:

NOTE

If the user feels that they have accidentally changed any parameters during these procedures and would like to exit and cancel any changes that may have been made press the On/Off **Line** key twice. If no parameters were changed then the printer will exit out of configuration mode and will display **IER 512 OFF-LINE.** If parameters were changed the display will show the **VALIDATION?** NO prompt. Press the **On/Off Line** key again to exit and cancel any changes that might have been made.

1. Power ON printer.

2. After printer finishes its self-test cycle, load paper stock. This procedure can not be accomplished without paper loaded into the printer.

3. Press the **On/Off Line** key to select the Off Line mode. Allow alarm to stop.

4. Enter the configuration menu of the printer by pressing the front panel keys in the following order: **B — A — Blank Strip — B** (six times). Refer to figure **7-35** or layout of front panel keys.

NOTE

Do not pause for longer than 1 second between entering the **Blank Strip** key and the six successive **B** keys or the printer will enter one of the other test modes, i.e., printing of configuration strip, or printing one of the test documents.

5. After a short delay the display will read "PASSWORD? 00000".

6. Press the On/Off Line key.

7. The display area shall display EMULATION **parameters.** Enter the PRINTING PARAMETERS MENU by pressing the A key 7 times.

8. The display area will read **PRINTING parameters.** Press the B key once to adjust the printer cut position and proceed to step 9 of this paragraph. Press the B key 2 times to adjust the print position horizontally and proceed to step 10 of this paragraph. Press the B key 3 times to adjust the print position vertically and proceed to step 11 of this paragraph.

9. The display will now read **Cut position shift±XXX.** A negative adjustment will move the cut position to the left on the strip and a positive value will move the position to the right (a value of 8 roughly equals 1 millimeter (mm)). The ideal cut position for the IER printer is 1 mm **±0.5mm** behind the perforation on the trailing edge of the strip. This position keeps paper dust at a minimum and minimizes the chance of paper jams. DO NOT adjust the cut position to be directly on the perforation as this causes excessive paper dust which will degrade the operation of the printer. DO NOT adjust the cut position to be in front of the perforation on the leading edge as this may cause the paper to jam. Go to step 12 of this paragraph.

10. The display will now read **Print pos shift ±XXX.** A negative adjustment will move all print positions to the left on the strip, and a positive value will move the all positions to the right. The ideal print position setting should put the print at 1.41 mm from the left edge of the strip. Go to step 12 of this paragraph.

11. The display will now read **Vertical Shift ±XXX.** A negative value will move all print up from the bottom of the strip. A positive value will move all print down from the top of the strip. The ideal vertical position is one that will allow the user to read all lines of data on the strip while the strip is in a strip holder.

12. Change the value by using the **Blank Strip** key to change the value and the **A** key to advance the cursor.

NOTE

The sign field can not be adjusted if the value field is set to **000.** If the sign needs to be adjusted set the desired value first, then use the A key to wrap back around to the sign field, and change the sign with the **Blank Strip** key.

13. Once the desired value is selected, press the **On/Off Line key twice.**

14. The display shall read **VALIDATION? NO.** Press the **Blank** Strip key to save this change.

NOTE

If the values were not modified the printer will exit out of the configuration mode and display **IER 512 OFF-LINE.**

15. If parameters were changed the display will read VALIDATION PERMANENT. Press the **On/Off Line** key to exit.

3.3.6.8 **RFSP (10095/1 4) Flight Bar Code Enable/Disable.** The following procedures are used to Enable or Disable the printing of a bar code on all flight plans, based on the Computer Identification Number of the flight plan.

NOTE

If the user feels that they have accidentally changed any parameters during these procedures and would like to exit and cancel any changes that may have been made press the **On/Off Line** key twice. If no parameters were changed then the printer will exit out of configuration mode and will display **IER 512 OFF-LINE.** If parameters were changed the display will show the **VALIDATION?** NO prompt. Press the **On/Off Line** key again to exit and cancel any changes that might have been made.

1. Power ON printer.
2. After printer finishes its self-test cycle, load paper stock. This procedure can not be accomplished without paper loaded into the printer.
3. Press the **On/Off Line** key to select the Off Line mode. Allow alarm to stop.
4. Enter the configuration menu of the printer by pressing the front panel keys in the following order: **B — A — Blank Strip — B** (six times). Refer to figure 7-35 for the layout of the front panel keys.

NOTE

Do not pause for longer than 1 second between entering the **Blank Strip** key and the six successive **B** keys or the printer will enter one of the other test modes, i.e., printing of configuration strip, or printing one of the test documents.

5. After a short delay the display will read **PASSWORD? 00000.**
6. Press the **On/Off Line** key.
7. The display area shall display **EMULATION parameters.** Press the B key twice to adjust the flight bar code adjustment.
8. The display area will read **Flight Bar Code** and the current setting which can be **Enable,** which will allow the printing of a bar code, or **Disable,** which will disable this feature.
9. To change the value, press the **Blank Strip** key.
10. Once the desired value is selected, press the **On/Off Line** key twice.
11. The display shall read **VALIDATION? NO.** Press the **Blank Strip** key to save this change.

NOTE

If the values were not modified the printer will exit out of the configuration mode and display **IER 512 OFF-LINE.**

12. If the parameters were changed the display will read **VALIDATION PERMANENT.** Press the **On/Off Line** key to exit.

3.3.6.9 **RFSP (10095/14) Operating Mode Setup Procedures.** The following procedures are used to setup the Operating mode of the printer. When the printer is set to the **Emulation-FAA** setting, the printer will operate connected to the **FDIO** system. When the operating mode is set to **AEA** mode, the printer will operate connected to the EFSTS system. **Note:** Do not connect the printer to the **FDIO** system while the printer is configured for **AEA** mode. Also, when configuring the printer, be sure to have the printer disconnected from the host system.

NOTE

If the user feels that they have accidentally changed any parameters during these procedures and would like to exit and cancel any changes that may have been made press the **On/Off Line** key twice. If no parameters were changed then the printer will exit out of configuration mode and will display **IER 512 OFF-LINE.** If parameters were changed the display will show the **VALIDATION?** NO prompt. Press the **On/Off Line** key again to exit and cancel any changes that might have been made.

1. Power ON printer.
2. After printer finishes its self-test cycle, load paper stock. This procedure can not be accomplished without paper loaded into the printer.
3. Press the **On/Off Line** key to select the Off Line mode. Allow alarm to stop.
4. Enter the configuration menu of the printer by pressing the front panel keys in the following order: **B — A — Blank Strip — B** (six times). Refer to figure 7-35 or layout of front panel keys.

NOTE

Do not pause for longer than 1 second between entering the **Blank Strip** key and the six successive **B** keys or the printer will enter one of the other test modes, i.e., printing of configuration strip, or printing one of the test documents.

5. After a short delay the display will read **"PASSWORD? 00000".**
6. Press the **On/Off Line** key.
7. The display area shall display **EMULATION parameters.** Press the **B** key once to adjust the operating mode.
8. The display area will read **Emulation Mode** and the current setting which can be **Emulation-FAA,** which will allow operation connected to the **FDIO** system, or **AEA,** which will allow the printer to operate connected to the EFSTS system.
9. To change the value, press the **Blank Strip** key.
10. Once the desired value is selected, press the **On/Off Line** key twice.

11. The display shall read **VALIDATION? NO.** Press the **Blank Strip** key to save this change.

NOTE

If the values were not modified the printer will exit out of the Configuration mode and display **IER 512 OFF-LINE.**

12. If parameters were changed the display will read **VALIDATION PERMANENT.** Press the **On/Off Line** key to exit.

3.3.6.10 RFSP (10095/14) Power On And Checkout. Since the TFSP is a form, fit, and function replacement of the dot matrix printers, connection of the power and data cables is the same. Placement of the paper stack holder should be directly behind the printer. Upon power up, the printer will perform a self-test to verify correct operation of the printer. Procedures for loading of the paper are listed below.

1. To load the paper, raise the lever located above the paper path.
2. Insert a stack of thermal paper into the paper stack holder.
3. Insert paper into the paper guide of the printer, with the black mark on the under side of the paper facing toward the front. When the feed motor on the printer starts to spin, lower the lever and the paper will automatically be loaded.
4. The printer will then be online and ready to accept data. When the RFSP is online and not accepting messages, proper operation is continually verified by Built-in Test Equipment (BITE).

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3.3.7 RANK Turn ON and Checkout

RANK peripheral elements are located only in remote sites, RANKs are powered up by the circuit breakers at the rear of the unit. The correct operation of the RANKs is verified by following the RANK pairing procedure in paragraph 3.3.7.1.

3.3.7.1 **RANK Pairing.** RANKs are paired to either a CRT or an RFSP at ATCT sites. The backup echo device for a RANK paired with a CRT is always an RFSP. If the RANK is paired with a CRT, a visible cursor will indicate the next logical entry position in the message entry area. The RFSP is line buffered and as such. has no external cursor. When the RANK is paired with an RFSP, one line is echoed at a time, rather than one character at a time.

To verify proper RANK/CRT pairing, press several keys on the RANK. These characters should be echoed on the paired device. To verify proper RANK/RFSP pairing, press several keys on the RANK and then press NEW LINE on the keyboard. The characters should print at the paired RFSP.

After RANK pairing verification, press the CANCEL key on the RANK to delete the character(s) held in the buffer.

Changing the RANK pairing to a different CRT or RFSP device is accomplished via the RECN task at the Multibus front panel assembly. Refer to paragraph 3.4.6.5 for RANK pairing instructions.

3.3.7.2 **RANK Message Verify.** The VER key, located on the far right keypad of the keyboard, toggles the RCU control element into verify mode. Then, pressing ENTER causes the message to be individually checked for field range. The RANK will be unavailable for message entry for a period of 1 minute while the message is being verified prior to being sent to the NAS computer. If the NAS computer does not respond to the message, within this timeout, the echo device will display **MSG TIMED OUT, RANK CLEARED.**

If the message is not accepted during verify, a reject message with information concerning the error will be displayed at the RANK's echo device. The incorrect message will remain displayed on the RANK echo device to facilitate editing. Once the error is corrected, pressing ENTER wilt cause the message to be rechecked (the RANK will remain in verify mode until the message is accepted by the Host or RCU). After the message is accepted, the verify mode is turned OFF and the RANK is available for message entry.

3.3.7.3 **RANK Operator Control Adjustments.** RANK keys are illuminated. Light intensity is controlled by either a knob (FA 10095/3) or DIM/BRIGHT keys (FA 10095/1 7) located on the top panel (upper right). Turning the knob clockwise or pressing the BRIGHT key increases brightness to the key lamps.

3.3.8 CRT Turn ON and Checkout

The CRT peripheral element displays messages sent between the Host and ATCT remote sites. The CRT is fully independent and requires no controller operation after initial brightness and contrast adjustments. The CRT emits an audible tone when initially powered up. The CRT contains built-in, independent, self-test firmware that verifies proper operation when the peripheral is powered ON.

3.3.8.1 CRT Pairing. The CRT is paired with a RANK at most remote sites. It is used as an RFSP alternate to display flight strips, for operator requested weather reports, general information messages, en route FDIO, and other messages, Refer to paragraph 3.4.6.5.1 for RANK pairing instructions,

3.3.8.2 **CRT to Printer Pairing.** The CRT may be paired with a printer at a remote site. This pairing will cause the messages that are printed on the printer to be displayed on the CRT that is paired with the printer, Refer to paragraph 3.4.6.5.2 for CRT to printer pairing.

3.3.8.3 CRT Screen Display. Standard and Alternate.

3.3.8.3.1 Standard Screen Display. The CRT screen is a high resolution, 12.5-inch viewing screen (14-inch tube), displaying green phosphor characters on a dark green background in an 80-column by 25-line format. The screen is divided into two display areas. The first fifteen lines are used to scroll the message from the printer if the CRT to printer pairing has been established. Lines 17-24 are used for a composition and editing area.

See figure 3-16 for standard CRT peripheral element horizontal screen display.

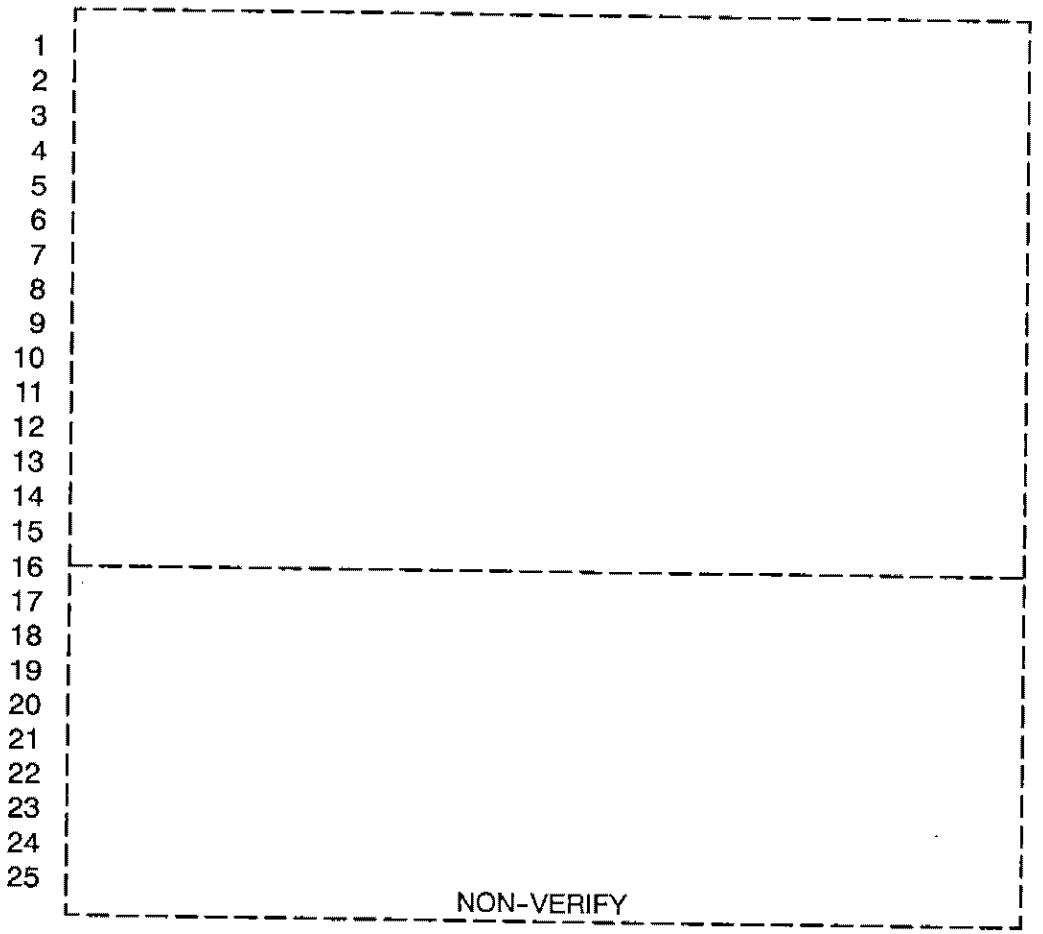


FIGURE 3-16. CRT PERIPHERAL ELEMENT HORIZONTAL SCREEN DISPLAY

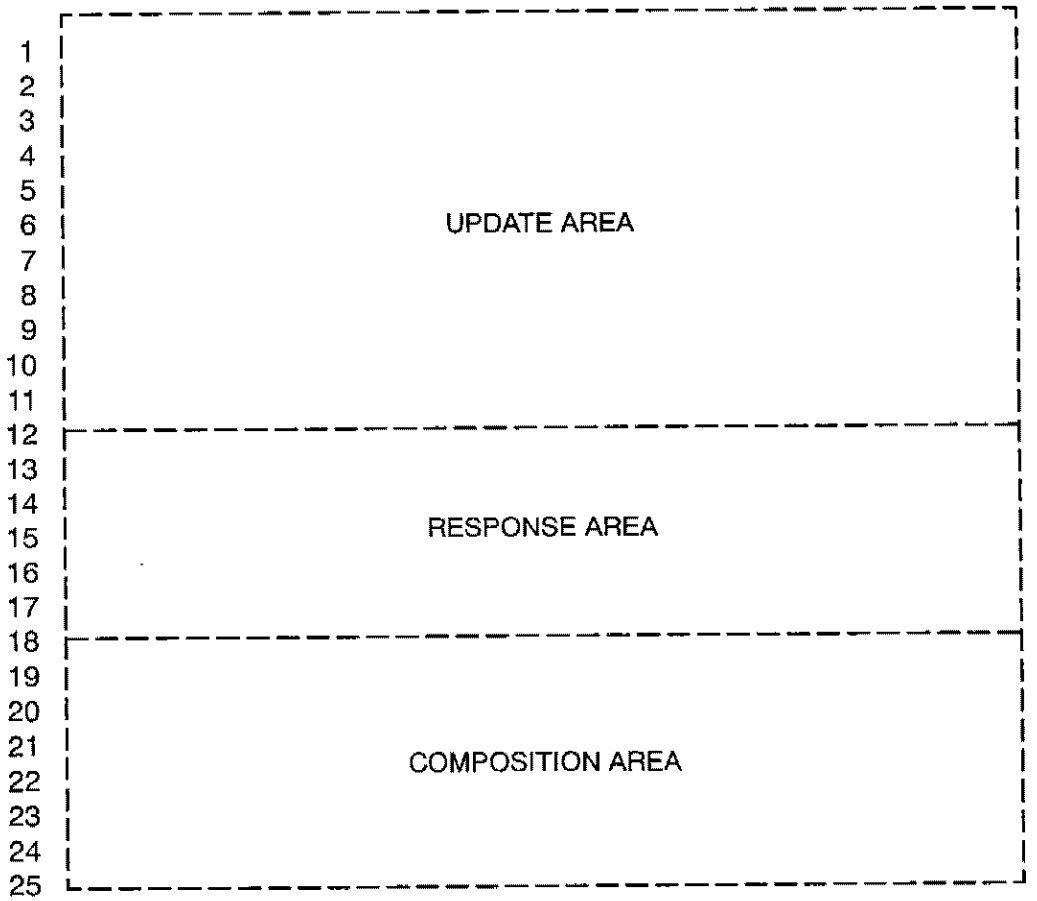
3.3.8.3.2 Alternate Screen Display. Utilized by systems other than FDIO, the CRT is the same as those listed in paragraph 3.3.8.3.1 with the exception of a three division horizontal display area as opposed to the standard's two division. There is one line of spacing between each area. The areas are:

Update Area-incoming message data (12 lines)

Response Area-response to RANK keyboard activity (6 Lines)

Composition Area-visual display of RANK messages (5 Lines)

See figure 3-17 for horizontal screen display.



***NOTE**

(Utilized by ODAPS, OFDPS for Example)

FIGURE 3-17. ALTERNATE CRT PERIPHERAL ELEMENT HORIZONTAL SCREEN DISPLAY

3.3.8.4 Alternate CRT Acknowledge. ACK processing timeout detection and message rerouting functions have been moved from the RCU to the application software.

When ODAPS sends a text message to the CRT (**update pending**), the RCU lights the MWL and displays text in the right half of CRT line 1.

When a controller hits the ACK key within the MWL acknowledgement timeout interval, the RCU sends an MWL acknowledgement message and ODAPS sends a type zero (00) message with the text of the update and the RCU extinguishes the MWL. Update pending is cleared and the text is displayed in the update message area of the CRT. If the message is not acknowledged within the allotted time, ODAPS reformats the update message and sends it directly to an RFSP. Subsequent update message are sent immediately to the RFSP until the ACK key is hit. The RCU then sends an MWL acknowledge message. ODAPS sends a type zero (00) message with the text **see printer**. The RCU extinguishes the MWL, clears **update pending** and displays the text in the update message area of the CRT.

3.3.8.5 CRT Operator Control Adjustments. Brightness and contrast are adjusted by independent control knobs located at the right of the unit front undercarriage.

3.4 REMOTE MONITORING AND CONTROL

3.4.1 BITE

Each FDIO system control element (CCU, PCU, and RCU) contains special BITE that allows testing and monitoring of critical control element operations.

DIAG tests initiated automatically at power up are incorporated into the BITE. When the control element is not directly communicating with the Host, some of the DIAG tests are invoked on a continual basis to verify the operation of the primary or secondary CCU or PCU. DIAG mode may be called manually at the Multibus front panel assembly, as well. These procedures are described in paragraph 7.2.1.2.3.

3.4.2 Multibus Front Panel Alarm

A momentary alarm built into the Multibus front panel assembly will sound if a system error occurs or the RFSP peripheral needs operator attention. Any condition causing the alarm to sound on the Multibus front panel assembly will be stored for printout on the RFSP selected as the error logger. The procedures for selecting the RFSP as the error logger are described in paragraph 7.2.7.1. Procedures for accessing systems status are described in paragraph 7.2.7.2.

3.4.3 Multibus LCD Display Area

The Multibus LCD display area has a 40-character field length. When the system is in main mode, system status will be displayed on the right side of the display area. If a system error should occur, the entire display area will be dedicated to the system error message. When the system is in DIAG or RECN mode, operator initiated task prompts are displayed. During RECN, the first 38 positions indicate the menu, current pairing, or prompts for assigning new devices. A two position field immediately following accepts RECN input. See figure 3-18 for Multibus LCD Display fields descriptions.

NOTE

The Host automatically locks out the Multibus front panel assembly for all assignments to prevent any alterations that might interfere with the FDIO system.

3.4.4 Front Panel Keyboard

The Multibus Front Panel Keyboard contains twenty (20) push button switches which allow the operator or technician to communicate directly with the control element.

To acknowledge errors and display the next subsequent error, if any, perform the following:

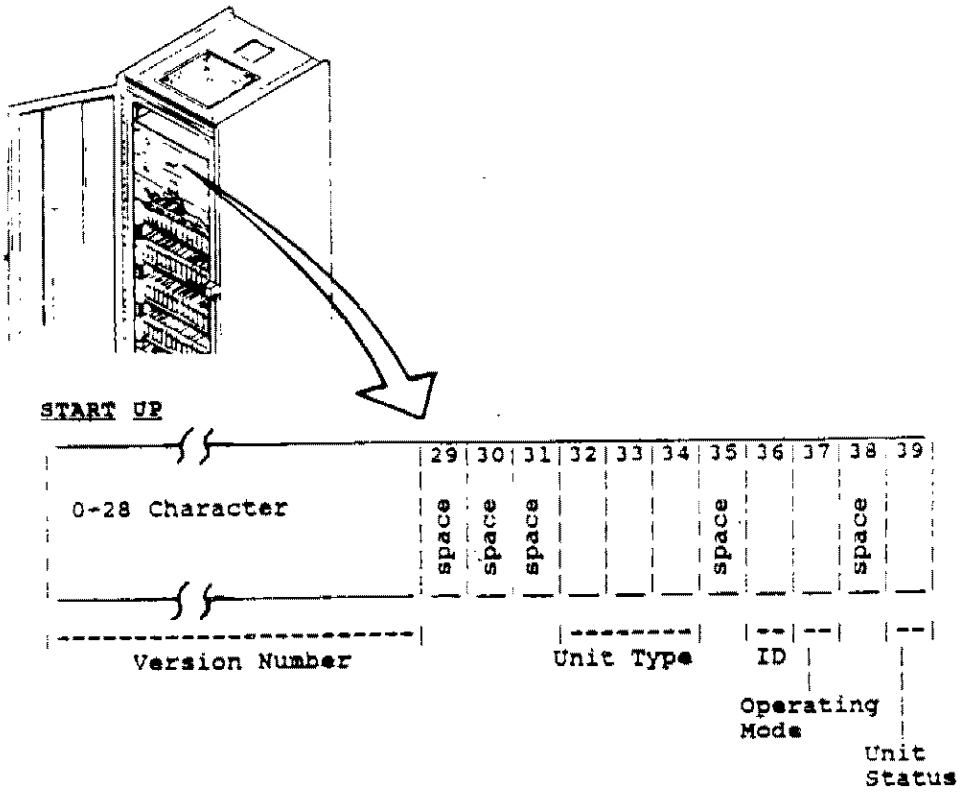
a. Press EXIT key to enter main mode (if system status indicates other than normal).

b. Transcribe the error message shown on display;

c. Press MSG ACK key to display the next message;

d. Cycle steps (b) and (c) of paragraph 3.4.4 until all messages in the buffer have been displayed.

The display will display main mode when the error buffer is empty. See SEL Operational Procedures, paragraph 7.2.7 for detailed procedures.



0 — 28	VERSION NUMBER
29 — 31	BLANK
32 — 34	UNIT TYPE (CCU, PCU, OR RCU)
35	BLANK
36	ID (A, B, C, OR D)
37	OPERATING MODE (N = NORMAL)
38	BLANK
39	UNIT STATUS (P = PRIMARY, S = SECONDARY)

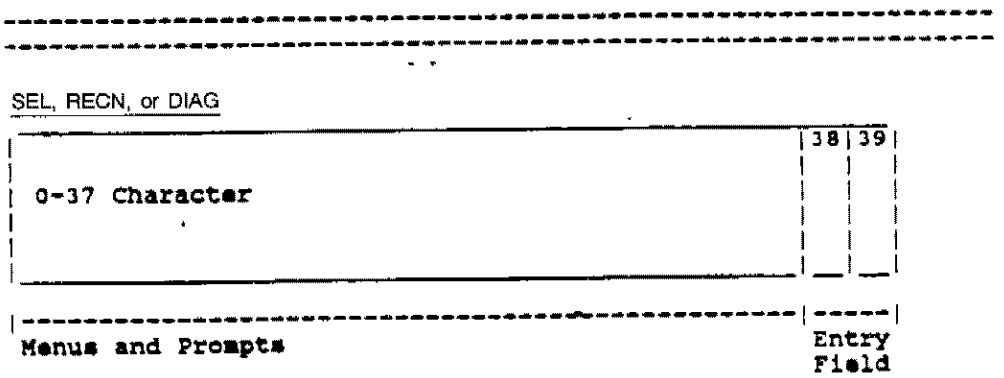


FIGURE 3-18. MULTIBUS LCD DISPLAY FIELDS

3.4.5 Error Conditions

A nonfatal error (e.g. RFSP out of paper) does not impair the processing capabilities of the control unit or interfere with the communication link between the Host and the primary processing unit. A nonfatal error is treated as a temporary problem to be corrected internally.

Error messages received reflect the specific error and severity of condition and will be displayed on the Multibus front panel assembly. See paragraph 7.2.1.2 for additional information on error messages displayed through the Multibus front panel assembly.

3.4.6 Primary and Secondary Control Units

Both the PCU and CCU cabinet assemblies have two identical Multibus control elements designated A and B. Control elements A and B are configured as a redundant pair such that one control element is primary and the other is secondary. Either A or B may be assigned as primary or secondary; however, only one may be the primary at any given time.

3.4.6.1 Multibus Front Panel Hardware Invoked Switch. In order to manually reverse assignments at the CCU or PCU control elements, the Host operator must send a Multibus front panel enable code to the control units (type 20 message). Then, by pressing PRI/SEC on the primary Multibus front panel while in main mode, the assignment will reverse. Internal errors will automatically initiate a switch sequence if the primary fails. If the secondary fails, the unit will be internally held in a reset state until power is cycled to that unit and an error message will be sent to the Host by the operational primary.

3.4.6.2 CCU or PCU Control Element RECN Task. The technician communicates with the RECN task through the Multibus front panel LCD module display. Prompts will appear at the display and responses will be issued through the keypad.

The RECN task at CCU and PCU control elements assign unit ID definitions (A or B). These assignments may be made through either the primary or secondary Multibus front panel. In addition, the PCU control element can assign an error logger device.

3.4.6.3 Assign PCU or RCU Error Logger Procedure. The procedures for assigning an error logger device at the PCU or RCU are located in paragraph 7.2.7.1.

3.4.6.4 CCU or PCU RECN Procedure. The seven step procedure for RECN at the CCU or PCU is as follows:

1. The technician will check the Multibus front panel LCD module display for message type. If a message other than an error message is in display, press EXIT to get to main mode.
2. Check for an error message in the LCD module display area. If an error message is present, refer to paragraph 3.4.4 for instructions on how to clear error messages.
3. Make sure the Host has sent a signal to unlock the Multibus front panel assembly. Press RECN to get into RECN mode.
4. The menu for RECN task will appear in the CCU display area as follows:

```
CONTROL ID = 1        PRIM/SEC = 2        :
```

The menu for RECN task will appear in the PCU display area as follows:

```
CNTRL ID=1        ERR LOG=2  PRIM/SEC=3:
```

5. At the RECN menu, control element designations may be made by pressing 1 and ENTER. The display will read:

UNIT: * 1=A 2=B 3=C 4=D 5=MENU:

* = Current unit ID status (A, B, C, or D)

The technician will enter the desired control element designation. The technician may return to the main menu by pressing 5 and ENTER or EXIT to terminate the task and return to main mode.

6. Repeat steps 1-5 of this paragraph for secondary unit.

NOTE

Only current unit ID statuses of A and B are recognized by Host. Current ID statuses of C and D must not be used for online control units. Normal configuration of control units is the top unit of the control unit redundant pair being configured as A with the bottom unit configured as B.

7. At the RECN menu, pressing the 2 key and ENTER key on a CCU or the 3 key and ENTER key on a PCU will allow the technician to change the status of a secondary unit to a primary unit, if no actual primary is present.

The secondary unit will become a primary unit and display the following:

1) UNIT SWITCHING STATUS STANDBY

2) FDIO INITIALIZATION VER * CCU BN P

* Current firmware version

If there is a valid primary or this function is attempted from a primary unit, the following error message will result:

INVALID OPERATION, PRESS ENTER

If the unit was a secondary when RECN was entered and there was an active primary, the display unit will read:

UNIT HAS A VALID SEC, PRESS ENTER :

Press ENTER to return to the RECN menu.
Press EXIT to return to main mode.

3.4.6.5 RCU RECN Procedure. The RECN task at the standard RCU assigns peripheral pairings and RFSP tab settings. The RECN task at the oceanic RCU assigns RANK pairings and formfeed timeout value setting.

3.4.6.5.1 RANK Pairing. The six step procedure for assigning RANK pairings at the RCU is as follows:

1. The technician will check the Multibus front panel LCD module display for message type. If a message other than an error message is in display, press EXIT to get to main mode.
2. Check for an error message in the display area. If an error message is present, refer to paragraph 3.4.4 for instructions on how to clear error messages.
3. Press RECN to get into RECN mode.
4. The menu for RECN task will appear in the display area.

   Standard:

RANK PAIR=1 ERR LOG=2 CRT PAIR=3 TAB=4

   Oceanic:

RANK PAIR=1 ERR LOG=2 FF TIMEOUT=3:

5. By pressing 1 and ENTER, pairing assignments may be viewed or changed. When assigning RANK pairing, valid responses are 1-10 for RFSP and 11-15 for CRT. A **0** indicates a null device.
6. The pairing routine will loop until the EXIT key is pressed. The technician will enter the value for a new device for pairing or backup through the numeric keypad. These pairing values will appear in the display area. To maintain present status, press ENTER after the pairing is shown. The following is an example of how the display area will read during RANK pairing (example shows primary pairing to a CRT (11) and the backup as an RFSP (1)):

RANK 16 PAIRED C11 16=MENU NEW DEVICE:

RANK 16 BACKUP P01 16=MENU NEW DEVICE:

   At any time during this routine the technician may press EXIT to return to main mode. After pairing is complete, the main menu will be displayed.

RANK PAIR=1 ERR LOG=2 CRT PAIR=3 TAB=4

3.4.6.5.2 CRT Pairing. Pairing a CRT with a printer will allow the CRT to display the messages that were printed on a printer. The six step procedure for this pairing is as follows:

1. The technician will check the Multibus front panel LCD module display for message type. If a message other than an error message is in display, press EXIT to get to main mode.
2. Check for an error message in the display area. If an error message is present, refer to paragraph 3.4.4 for instructions on how to clear error messages.

3. Press RECN to get into RECN mode.

4. The menu for RECN task will appear in the display area.

5. By pressing 3 and ENTER, pairing assignments may be viewed or changed. When assigning CRT pairing, valid responses are 11-15. A **0** indicates a null device.

6. The pairing routine will loop until the EXIT key is presssed. The technician will enter the value for a new device through the numeric keypad. These pairing values will appear in the display area. To maintain present status, press ENTER after the pairing is shown. The following is an example of how the display area will read during CRT pairing (example shows printer 1 being paired with CRT 11):

```
PRINTER 01 PAIRED C11 16=MENU NEW DEV:
```

At any time during this routine the technician may press EXIT to return to main mode. After pairing is complete the main menu will be displayed.

3.4.6.5.3 Tab Settings. The tab settings in the RECN task will allow the technician to determine which printers will be able to print half strips and which will print full strips. The six step procedure at the RCU is as follows:

1. The technician will check the Multibus front panel LCD module display for message type. If a message other than an error message is in display, press EXIT to get to main mode.

2. Check for an error message in the display area. If an error message is present, refer to paragraph 3.4.4 for instructions on how to clear error messages.

3. Press RECN to get into RECN mode.

4. The menu for RECN task will appear in the display area.

5. By pressing 4 and ENTER, the tab settings may be viewed or changed. When assigning the tab setting values, a **1** will indicate half strips will be printed and a **0** will indicate that full strips will be printed. The default will be a **0**.

6. The routine will loop until the EXIT key is pressed. The technician will enter the new value through the numeric keypad. These vaules will appear in the display area. To maintain present status, press ENTER after the value is shown. The following is an example of how the display area will read during tab setting:

```
PRT 01=1 FULL=0  HALF=1 16=MAIN MENU
```

The above example indicates that printer 1 will print half strips.

At any time during this routine the technician may press EXIT to return to main mode. After the settings are complete, the main menu will be displayed.

3.4.6.5.4 Formfeed Time Setting. The formfeed time setting allows the technician to determine the time period that the RFSPs will wait following the printing of a flight strip mesage before moving the flight strip to a position above tear bar. This option is only available through the oceanic RECN menu. The seven step procedure to set this time value is as follows:

1. The technician will check the Multibus front panel LCD module display for message type. If a message other than an error message is in display, press EXIT to get to main mode.

2. Check for an error message in the display area. If an error message is present, refer to paragraph 3.4.4 for instructions on how to clear error messages.

3. Press RECN to get into RECN mode.

4. The menu for the RECN task in the oceanic RCU will appear in the display area.

RANK PAIR=1 ERR LOG=2 FF TIMEOUT=3:

5. By pressing 3 and ENTER, the currect formfeed value will be displayed with a prompt to change.

FF TIMEOUT VALUE XXXX CHANGE? Y OR N:

NOTE

XXXX = 4-digit formfeed time value

6. By pressing YES and ENTER a prompt for the first two digits of the 4-digit value will be displayed.

ENTER FIRST TWO OF FOUR DIGIT VALUE:

7. By entering the first two digits and ENTER a prompt for the second two digits will be displayed. Due to constraints of the system firmware all 4-digits must be entered including leading zeros.

ENTER SECOND TWO DIGITS:

After entering the second two digits and ENTER, the system will display the new four digit value that was just entered. If this value is not correct press YES and begin the process over again. If the value displayed is the desired value, pressing NO will return the user to the RECN menu.

At any time during this routine the technician may press EXIT to return to main menu.

3.4.6.6 Control Unit DIAG Procedures. DIAG procedures for the control units are available through manipulation of the keys on the front panel. The DIAGs enable the technician to select and run specific tests that consist of RAM/ROM tests, BC query tests, canned message tests, display

tests (CCU and PCU only), and keypad tests. The step by step procedures for the DIAG tests are described in section 7.0.

3.5 EQUIPMENT SHUTDOWN

WARNING

Shutdown of the FDIO equipment will prevent the vital communications link between the Host central computer and ATCT remote sites. This could cause a threat to air safety. For this reason, it is recommended that shutdown due to any condition other than an emergency be approved through ARTCC management.

NOTE

FAA emergency procedures take precedence over FDIO emergency procedures. No harm will be done to the FDIO system in this emergency procedure override.

3.5.1 Fatal Failure

If the Host should go offline, messages sent from the remote sites to the ARTCC will be held in the CCU buffer until such time that the Host comes back online. If a fatal failure occurs at a remote site, the CCU will generate an error message to notify the Host. The CCU will detect the inability of the Host to communicate with the remote site after an attempt is made to send a message to that remote site. This protocol was chosen to eliminate extraneous/erroneous message traffic to the Host. System engineers at the ARTCC will contact the controllers at the remote site to determine the site condition.

3.5.2 Non-Emergency Shutdown

Any control or peripheral element in the FDIO system may be taken offline as necessary by setting its power switch to the OFF position. Control cabinet assemblies at the ARTCC may be shutdown for any required maintenance by using redundancy to continue uninterrupted operation. RCU control cabinet assemblies can not be shutdown without interrupting its ATCT operations. Peripheral elements may be taken off the system for maintenance without system interruption (a previously designated alternate will replace the peripheral). Peripheral devices must be powered OFF before being removed from or connected to the system.

Peripheral elements should be powered down before the control cabinet assemblies if it becomes necessary to take any or all of the FDIO equipment offline.

3.5.2.1 Non-Emergency Shutdown Procedures

1. Set the power switches at the RFSP, RANK, and CRT peripherals to OFF.
2. Set the power switch at the ac power distribution assembly to OFF. The entire FDIO system is now powered OFF.
3. The power supply and BC assemblies in the control unit may be turned OFF in any order before restart procedures.

3.5.3 Emergency Shutdown Procedures

The fastest way to shut down the FDIO system in an emergency is to disconnect the power at an outside source. This termination will not harm the FDIO system. The next most expedient way to power OFF the FDIO system is to turn OFF the ac power distribution assembly switches in each control cabinet assembly (ARTCC sites have two ac power distribution assemblies in each control unit. Remote sites have one ac power distribution assembly.).

Powering down the control cabinet assemblies automatically terminates communication with associated peripheral elements. Power to peripherals must then be turned OFF at the individual peripheral element.

3.5.4 Power Up After Emergency Shutdown

Once emergency conditions have subsided, the FDIO system may be brought back online, providing the equipment has not been damaged. The technician shall make sure all the power supply switches to FDIO equipment are set to OFF.

After all control and peripheral elements have been manually turned OFF, the technician shall check the equipment for damage by sight and smell, beginning with the control elements. If the technician determines that there is no physical damage to any element, power ON procedures may be implemented. Power ON procedures are described in Turn On and Checkout, paragraphs 3.3.2 and 3.3.4.

4.0 STANDARDS AND TOLERANCES

4.1 INTRODUCTION

All essential standards and tolerances related to the FDIO system are listed in table 4-1 and correspond with the applicable maintenance procedure paragraphs in section 6.0. The standards and tolerances prescribed in table 4-1 are based on equipment and monitor requirements, equipment and manufacturing specifications, use of standard test equipment, and standard measuring procedures. Equipment and monitor standards, tolerances, and limits are applicable to the equipment taken as a whole.

4.2 DEFINITION OF TERMS

Parameter, reference, standard, initial, and operating tolerance limit, as used in table 4-1, are defined in paragraphs 4.2.1 through 4.2.5.

4.2.1 Parameter

The parameter is each system performance element that can be measured or tested to a particular standard.

4.2.2 Reference

The reference lists the reference or, if applicable, check procedure reference paragraph for checking the parameter against the listed standard.

4.2.3 Standards

The standard is the optimum value assigned to an essential parameter of the equipment. It is compatible with the system as a whole and the design capability of the equipment involved.

4.2.4 Initial Tolerance Limit

The initial tolerance limit is the maximum deviation above and below the standard value of the parameter or the range that is permissible when the equipment is accepted for use in the NAS at the time of initial commissioning, or subsequent to any modification.

4.2.5 Operating Tolerance Limit

The operating tolerance is the maximum deviation, above and below the standard value, over which the equipment may continue to operate without adjustment or corrective maintenance, and beyond which remedial action is required.

TABLE 4-1. STANDARDS AND TOLERANCES

PARAMETER	REFERENCE	STANDARD	TOLERANCE LIMIT	
			INITIAL	OPERATING
CCU and PCU: GPI and GPO data	FDIO Firmware Software Interface Control Document (SICD)	8 Bits Plus Parity in Bit Parallel Byte Series	None	None
Data Flow Between Control Units	FDIO Firmware Software Interface Control Document (SICD)	Synchronous at 2400 bits per second (bps)	Minimum of 2400 bps	Same as Initial
Data Flow Between RCU and CRT	FDIO Firmware Software Interface Control Document (SICD)	Asynchronous at 2400 bps	Minimum of 2400 bps	Same as Initial
Data Flow Between RCU and RANK	FDIO Firmware Software Interface Control Document (SICD)	Asynchronous at 2400 bps	Minimum of 1200 bps	Same as Initial
CCU, PCU, and RCU Incoming and Outgoing Message Memory Buffer Capacity	FDIO Firmware Program Design Specification (PDS)	16 Kb	Minimum of 16 Kb	Same as Initial
CRT (FA 10095/4): Displayed Characters	FDIO (CRT) Manual	80	Minimum of 80	Same as Initial

TABLE 4-1. STANDARDS AND TOLERANCES (Continued)

PARAMETER	REFERENCE	STANDARD	TOLERANCE LIMIT	
			INITIAL	OPERATING
Displayed Lines	FDIO (CRT) Manual	25	Minimum of 25	Same as Initial
Composed Character Dot Matrix	FDIO (CRT) Manual	9x12	Minimum 9 wide by 12 high	Same as Initial
Dot Character	FDIO (CRT) Manual	7x9	Minimum 7 wide by 9 high	Same as Initial
Display Line Width	FDIO (CRT) Manual	< 0.02 in.	None	None
Ratio of Maximum to Minimum Line or Character Segment Width	FDIO (CRT) Manual	< 2 to 1	None	None
Display Linearity Error	FDIO (CRT) Manual	< 2% of display height	None	None
Physical Dimensions:				
Depth	FDIO (CRT) Manual	< 18 5/8 in.	None	None
Width	FDIO (CRT) Manual	< 17 11/16 in.	None	None
Height	FDIO (CRT) Manual	< 17 3/8 in.	None	None
Aspect Ratio	FAA letter 24 SEP 1985 Deviation Request Approval	0.35 to 0.6	None	None
Tilt Range	FDIO (CRT) Manual	Upward: 12° Downward: 10°	None	None

TABLE 4-1. STANDARDS AND TOLERANCES (Continued)

PARAMETER	REFERENCE	STANDARD	TOLERANCE LIMIT	
			INITIAL	OPERATING
Rotate Range	FDIO (CRT) Manual	≥ ±135	None	None
Tilt Rotate Base Height	FDIO (CRT) Manual	≤ 5 in.	None	None
Overall Height (Cabinet and Base)	FDIO (CRT) Manual	≤ 22 3/8 in.	None	None
Display Area	FDIO (CRT) Manual	≥ 12 in.	None	None
Power Consumption Per Unit	FDIO (CRT) Manual	≤ 250 W at 115 V ac	None	None
FDIO System Primary Power Source:				
Voltage		115 V ac	103.5 to 126.5 V ac	103.5 to 126.5 V ac
Frequency		60 Hz	57 Hz to 63 Hz	57 Hz to 63 Hz
CRT FA 10095/12:				
Displayed Characters	FDIO2 (CRT) Technical Manual	80	Minimum of 80	Same as Initial
Displayed Lines	FDIO2 (CRT) Technical Manual	25	Minimum of 25	Same as Initial
Composed Character Dot Matrix	FDIO2 (CRT) Technical Manual	9x12	Minimum 9 wide by 12 high	Same as Initial
Dot Character	FDIO2 (CRT) Technical Manual	7x9	Minimum 7 wide by 9 high	Same as Initial

TABLE 4-1. STANDARDS AND TOLERANCES (Continued)

PARAMETER	REFERENCE	STANDARD	TOLERANCE LIMIT	
			INITIAL	OPERATING
Physical Dimensions:				
Depth	FDIO2 (CRT) Technical Manual	< 14.25 in.	None	None
Width	FDIO2 (CRT) Technical Manual	< 14.25 in.	None	None
Height	FDIO2 (CRT) Technical Manual	< 14.50 in.	None	None
Display Area	FDIO2 (CRT) Technical Manual	≥ 12 in. and < 14 in.	None	None
Power Consumption Per Unit	FDIO2 (CRT) Technical Manual	250 W at 120 V ac	None	None
FDIO System Primary Power Source:				
Voltage	FDIO2 (CRT) Technical Manual	115 V ac	103.5 to 126.5 V ac	103.5 to 126.5 V ac
Frequency	FDIO2 (CRT) Technical Manual	60 Hz	57 Hz to 63 Hz	57 Hz to 63 Hz

TABLE 4-1. STANDARDS AND TOLERANCES (Continued)

PARAMETER	REFERENCE	STANDARD	TOLERANCE LIMIT	
			INITIAL	OPERATING
RFSP (FA 10095/2):				
Printing Rate	FDIO Printer M2501010T	29	Minimum of 29 characters per second	Same as Initial
Printed Character Appearance	FDIO Printer M2501010T	Legible at 5 feet by people with vision corrected to 20-20	None	None
Character Size:				
Upper-case Height	FDIO Printer M2501010T	0.164 in.	0.155 to 0.173 in.	0.155 to 0.173 in.
Upper-case Width	FDIO Printer M2501010T	0.100 in.	0.095 to 0.105 in.	0.095 to 0.105 in.
Lower-case Height	FDIO Printer M2501010T	0.110 in.	0.105 to 0.115 in.	0.105 to 0.115 in.
Lower-case Width	FDIO Printer M2501010T	0.085 in.	0.081 to 0.089 in.	0.081 to 0.089 in.
Vertical Spacing	FDIO Printer M2501010T	≤ 5 lines per inch	None	None
Physical Unit Width	FDIO Printer M2501010T	< 17.25	None	None
Physical Unit Depth	FDIO Printer M2501010T	< 13.25 in.	None	None
Power Consumption Per Unit	FDIO Printer M2501010T	350 W at 115 V ac	None	None
Physical Unit Weight	FDIO Printer M2501010T	< 60 lbs.	None	None

TABLE 4-1. STANDARDS AND TOLERANCES (Continued)

PARAMETER	REFERENCE	STANDARD	TOLERANCE LIMIT	
			INITIAL	OPERATING
RFSP FA 10095/11:				
Printing Rate	291814-001	29	Minimum of 29 characters per second	Same as Initial
Printed Character Appearance	291814-001	Legible at 5 feet by people with vision corrected to 20-20	None	None
Character Size:				
Upper-case Height	291814-001	0.133 in.	0.128 to 0.138 in.	0.128 to 0.138 in.
Upper-case Width	291814-001	0.081	0.076 to 0.086 in.	0.076 to 0.086 in.
Lower-case Height	291814-001	0.094 in.	0.089 to 0.099 in.	0.089 to 0.099
Lower-case Width	291814-001	0.072 in.	0.067 to 0.077 in.	0.067 to 0.077 in.
Vertical Spacing	291814-001	6 lines per inch	None	None
Physical Unit Width	291814-001	< 19.00 in.	None	None
Physical Unit Depth	291814-001	< 16.00 in.	None	None
Physical Unit Height	291814-001	< 9.00 in.	None	None
Power Consumption Per Unit	291814-001	< 250 W at 120 V ac	None	None
Physical Unit Weight	291814-001	< 35 lbs.	None	None

TABLE 4-1. STANDARDS AND TOLERANCES (Continued)

PARAMETER	REFERENCE	STANDARD	TOLERANCE LIMIT	
			INITIAL	OPERATING
RFSP FA 10095/14:				
Printed Character Appearance	N07102A	Legible at 5 feet by people with vision corrected to 20-20	None	None
Character Size:				
Upper-case Height	N07102A	0.164 in.	0.174 to 0.184 in.	0.174 to 0.184 in.
Upper-case Width	N07102A	0.100 in.	0.110 to 0.090 in.	0.110 to 0.090 in.
Lower-case Height	N07102A	0.125 in.	0.135 to 0.115 in.	0.135 tp 0.115 in.
Lower-case Width	N07102A	0.090 in.	0.080 to 0.100 in.	0.080 to 0.100 in.
Vertical Spacing	N07102A	6 Lines per inch	None	None
Power Consumption Per Unit	N07102A	< 250 W at 120 V ac	None	None
RANK: FA 10095/3				
Physical Size:				
Width	TI 6130.6, Section 1.0	< 14.5 in.	None	None
Depth	TI 6130.6, Section 1.0	< 10.5 in.	None	None
Height	TI 6130.6, Section 1.0	< 5 in.	None	None

TABLE 4-1. STANDARDS AND TOLERANCES (Continued)

PARAMETER	REFERENCE	STANDARD	TOLERANCE LIMIT	
			INITIAL	OPERATING
Power Consumption Per Unit	TI 6130.6, Section 1.0	< 250 W 115 V ac	None	None
RANK: FA 10095/17				
Physical Size:				
Width	TI 6130.6, Section 1.0	< 14.5 in.	None	None
Depth	TI 6130.6, Section 1.0	< 8.0 in.	None	None
Height	TI 6130.6, Section 1.0	< 2.5 in.	None	None
Power Consumption Per Unit	TI 6130.6, Section 1.0	< 46 W at 115 V ac	None	None
CCU, PCU, and RCU:				
+5 V dc Multibus Adjustment Procedures	TI 6130.6, Paragraph 6.3.2.3.1	+5 V dc	5.00 to 5.10 V dc	5.00 to 5.10 V dc
+12 V dc Multibus Adjustment Procedures	TI 6130.6, Paragraph 6.3.2.3.2	+12 V dc	-11.4 to -12.6 V dc	-11.4 to -12.6 V dc
-12 V dc Multibus Adjustment Procedures	TI 6130.6, Paragraph 6.3.2.3.3	-12 V dc	5.00 to 5.10 V dc	5.00 to 5.10 V dc
+5 V dc BC Adjustment Procedures (CCU and PCU)	TI 6130.6, Paragraph 6.3.2.3.4	+5 V dc	5.00 to 5.10 V dc	5.00 to 5.10 V dc

TABLE 4-1. STANDARDS AND TOLERANCES (Continued)

PARAMETER	REFERENCE	STANDARD	TOLERANCE LIMIT	
			INITIAL	OPERATING
+12 V dc BC Adjustment Procedures (CCU only)	TI 6130.6, Paragraph 6.3.2.3.5	+12 V dc	+11.75 to +12.25 V dc	+11.75 to +12.25 V dc
-12 V dc BC Adjustment Procedures (CCU only)	TI 6130.6, Paragraph 6.3.2.3.6	-12 V dc	-11.75 to -12.25 V dc	-11.75 to -12.25 V dc
+5 V dc BC Adjustment Procedures (RCU only)	TI 6130.6, Paragraph 6.3.2.3.7	+5 V dc	5.00 to 5.10 V dc	5.00 to 5.10 V dc
Power Consumption Per Cabinet Assembly	TI 6130.6, Section 1.0	< 500 W at 115 V ac	None	None

5.0 PERIODIC MAINTENANCE

5.1 INTRODUCTION

This section lists all maintenance activities which are performed on a recurring basis to ensure optimum performance, minimize interruption, and avoid breakdown. This section is divided into three parts: performance checks, other onsite maintenance tasks, and offsite maintenance tasks. Performance checks provide for maintenance activities on a regular basis. Part of this maintenance activity is contained in the system operational software, which performs confidence check diagnostics during normal operation. These diagnostics are designed to indicate current system malfunctions. The performance checks which should be accomplished on a routine basis are listed in table 5-1. Other onsite maintenance tasks prevent the deterioration of equipment and ensure reliable operation of the system and equipment. These maintenance tasks are listed and described in table 5-2. Offsite maintenance tasks are tasks of a periodic nature that cannot be performed onsite and require removal of equipment to a central repair facility.

5.2 PERFORMANCE CHECKS

Table 5-1 lists all required tests, measurements, and observations of normal operating controls and functions necessary to determine if the equipment is operating within established tolerances or limits.

5.3 OTHER ONSITE MAINTENANCE TASKS

Table 5-2 lists tasks necessary to prevent deterioration and ensure reliable operation of the FDIO equipment.

5.4 OFFSITE MAINTENANCE TASKS

There are no offsite maintenance tasks of a periodic nature on the FDIO System that require removal to a central repair facility.

TABLE 5-1. PERFORMANCE CHECKS

PERFORMANCE CHECK	REFERENCE	PARAGRAPH
	STANDARDS AND TOLERANCES	MAINTENANCE PROCEDURES
a. **CCU, PCU, and RCU CABINETS**		
• Operation	None	6.2.1
• Observe the front panel for correct operation.		
b. **CRT**		
• Operation	Table 4-1	6.2.2
1. Observe the contrast of CRT.		
2. Observe the brightness of CRT.		

TABLE 5-1. PERFORMANCE CHECKS (Continued)

PERFORMANCE CHECK	REFERENCE STANDARDS AND TOLERANCES	PARAGRAPH MAINTENANCE PROCEDURES
c. **RANK**		
• Operation	Table 4-1	6.2.3
1. Inspect for extinguished lamps.		
2. Observe the brightness of RANK keys.		
d. **RFSP**		
• Operation	Table 4-1	6.2.4
1. FA 10095/2 and FA 10095/11		
(a) Inspect for print degradation.		
(b) Observe lamp illumination.		
(c) Check for ribbon mechanical wear.		
(d) Check for frayed or worn belts.		
2. FA 10095/14		
• Inspect for print degradation.		

TABLE 5-2. OTHER ONSITE MAINTENANCE TASKS

ONSITE MAINTENANCE TASKS	REFERENCE STANDARDS AND TOLERANCES	PARAGRAPH MAINTENANCE PROCEDURES
a. **POWER SUPPLIES**		
• CCU, PCU, RCU Power Supplies Adjustments	Table 4-1	6.3.2
1. +5 V dc Multibus	Table 4-1	6.3.2.3.1
2. +12 V dc Multibus (RCU)	Table 4-1	6.3.2.3.2
3. -12 V dc Multibus (RCU)	Table 4-1	6.3.2.3.3

TABLE 5-2. OTHER ONSITE MAINTENANCE TASKS (Continued)

ONSITE MAINTENANCE TASKS	REFERENCE STANDARDS AND TOLERANCES	PARAGRAPH MAINTENANCE PROCEDURES
4. +5 V dc BC for CCU and PCU	Table 4-1	6.3.2.3.4
5. +12 V dc BC for CCU only	Table 4-1	6.3.2.3.5
6. -12 V dc BC for CCU only	Table 4-1	6.3.2.3.6
7. (+5 V dc for RCU only)	Table 4-1	6.3.2.3.7
8. CCU and RCU Ripple Test	None	6.3.2.3.8
c. **FRONT PANEL MULTIBUS REDUNDANCY OPERATION**		
• Redundant Operation Check	Table 4-1	6.3.3
• Perform CCU or PCU switch to verify operation.		
c. **VERIFY FAN OPERATION**		
• Observe Operation		6.3.4
d. **CCU, PCU or RCU CABINETS**		
1. Clean Cabinets	None	6.4.1
(a) Clean Exterior		
(b) Clean Interior		
2. Clean Cabinet Fan Assembly	None	6.4.2
3. Conductive Paint	None	6.4.3
• Touch-up as required		
4. Exterior Paint	None	6.4.4
• Touch-up as required		
e. **CRT**		
• Clean	None	6.4.5
1. Clean Exterior		
2. Clean Screen		

TABLE 5-2. OTHER ONSITE MAINTENANCE TASKS (Continued)

ONSITE MAINTENANCE TASKS	REFERENCE STANDARDS AND TOLERANCES	PARAGRAPH MAINTENANCE PROCEDURES
f. **RANK**		
• Clean	None	6.4.6
• Clean Exterior		
g. **RFSP**		
• Clean		
1. FA 10095/2 and FA 10095/11:	None	6.4.7.1
(a) Clean Exterior		
(b) Vacuum Interior		
2. FA 10095/14	None	6.4.7.2
(a) Clean Printhead and platen		
(b) Clean Cutter Blade and Interior		

6.0 MAINTENANCE PROCEDURES

6.1 INTRODUCTION

This section consists of procedures required for accomplishing the various maintenance activities listed in tables 5-1 and 5-2. This section is divided into four parts: performance check procedures, other maintenance tasks procedures, cleaning/paint touch-up procedures, and special maintenance procedures. No condition exists that will expose the controller to a safety hazard in the normal operating conditions of the FDIO hardware.

6.2 PERFORMANCE CHECK PROCEDURES

6.2.1 CCU, PCU, and RCU Operations

Observe the front panel of the Multibus for correct operation indications. If a message is reported on the front panel refer to Table 7-1, System Error Table.

a. The correct indication of front panel text upon initialization is as follows:

CCU

FDIO INITIALIZATION VER X.X CCU XN P

FDIO INITIALIZATION VER X.X CCU XN S

PCU

FDIO INITIALIZATION VER X.X PCU XN P

FDIO INITIALIZATION VER X.X PCU XN S

RCU

FDIO INITIALIZATION VER X.X RCU XN P

Where X.X is the revision level of the firmware currently used in the FDIO system, and X is A, B, C, or D.

b. The correct indication of normal front panel operation is as follows:

CCU

CCU XN P

CCU XN S

PCU

PCU XN P
PCU XN S

RCU

RCU XN P

Where X.X is the revision level of the firmware currently used in the FDIO system, and X is A, B, C, or D.

6.2.2 CRT Operations

a. Contrast Control

3. Turn control clockwise and observe the change in contrast.
4. Turn control counterclockwise and observe change in contrast.
5. Set at desired level.

b. Brightness Control

1. Turn control clockwise and observe brightness change in screen.
2. Turn control counterclockwise and observe brightness change in screen.
3. Set control to desired level.

NOTE

If the screen is persistently too bright or character definition is blurred, refer to the vendor's manual.

6.2.3 RANK Operations

a. Observe keyboard to verify that all key lamps are illuminated except MWL on FA 10095/3.

b. Adjust the controls and observe the change in brightness. The brightness controls location is shown in figures 3-9 and 3-10.

6.2.4 RFSP Operations

a. Run self test to check for print degradation (refer to vendor's maintenance manual for proper procedures and print degradation symptoms).

b. Verify interior lamp is illuminated (FA 10095/2 only).

c. Visually inspect for ribbon mechanical wear. Refer to vendor's maintenance manual for proper procedure (FA 10095/2 and FA 10095/11 only).

d. Visually inspect for frayed or worn belts. Refer to vendor's maintenance manual for proper procedure (FA 10095/2 and FA 10095/11 only).

6.3 OTHER MAINTENANCE TASK PROCEDURES

6.3.1 Tools Required to Perform the Maintenance Task

The following tools are required to perform the maintenance task:

- 12-inch long insulated screwdriver, 1/8-inch blade,
- Digital volt meter with leads,
- 1/4-inch nut driver,
- 10-inch long Phillips screwdriver #2, and
- 12-inch long standard screwdriver, 3/8-inch blade.

6.3.2 CCU, PCU, and RCU Power Supplies

The purpose of this procedure is to provide a qualified technician a method of verification and adjustment for the power supplies within the FDIO system.

There are two types of power supplies contained in the FDIO system: + 5 V dc and ± 12 V dc.

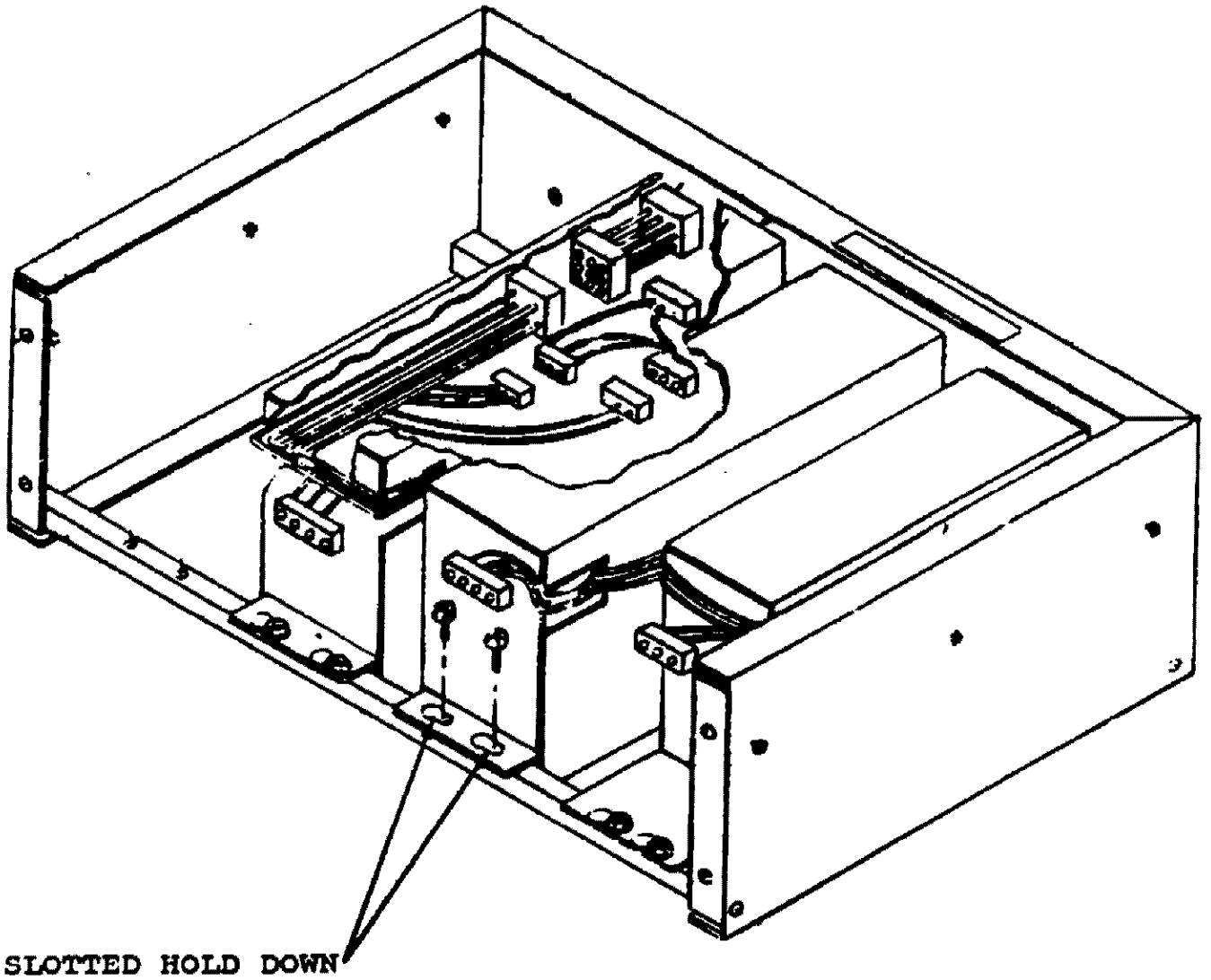
Section 1.0 depicts the location and type of power supply used in each control unit, and should be referred to prior to any maintenance task.

6.3.2.1 General Requirements Pertaining to All Power Supplies. General remarks that pertain to all types of power supplies are:

- The power supplies are covered by a wire screen which acts as a protective shield against foreign objects, for example, washers, nuts, fingers, etc., from coming in contact with the components of the power supply. See figure 6-1.
- All adjustments are to be made with the screen removed.
- Remove the power supply prior to performing the adjustment.

WARNING

115 V ac exists on the black and white primary input wires to the transformer. This voltage can be lethal. Observe all standard safety precautions.



NOTE

The drawing shows the front panel of power supply removed.

FIGURE 6-1. MULTIVOLT POWER SUPPLY (CUT AWAY VIEW)

6.3.2.2 Removal/Replacement Procedures for All Power Supplies. Removal/replacement procedures for all power supplies are as follows:

a. Turn OFF all power to the chassis under adjustment.

b. Remove the four Phillips head screws that hold the chassis in the cabinet, and pull the chassis out. See figure 6-2.

NOTE

The chassis slide does not have a locking device to hold the chassis out. When the chassis slide is extended another technician is required to hold the chassis in the open position.

c. Disconnect the plugs/jacks for the power supply to be adjusted.

d. On the power supply to be adjusted, loosen but do not remove the four screws that hold it in place. See figure 6-1.

e. Slide the power supply to the right until the slotted hold-down permits the power supply to be lifted upwards and removed.

f. Place power supply on top of the other power supplies for support, and reconnect the plugs/jacks removed in paragraph 6.3.2.2d.

g. Remove the power supply screen cover.

h. Adjustments can now be made to the power supply after power is applied.

i. After adjustment is made, reverse the procedure used for removal to re-install power supply.

6.3.2.3 Power Supply Adjustment Procedures

6.3.2.3.1 +5 V dc Multibus Adjustment Procedures. The procedures for adjusting the +5 V dc Multibus are as follows:

a. Turn OFF all power to the chassis under adjustment.

b. Refer to paragraph 6.3.2.2 for power supply removal, if required.

c. Open the front panel on the Multibus chassis under alignment.

d. Connect a Digital Volt Meter (DVM) across A(N)A1A2C101 (front panel control board) with the positive lead to the plus side of the capacitor (C101), and the negative lead to the other side. See figure 6-3.

e. Apply power to the Multibus.

f. Observe and record the reading on the DVM.

g. If the voltage is outside of tolerance (5.00 to 5.10 V dc) proceed to paragraph 6.3.2.3.1h. If the voltage is within tolerance proceed to paragraph 6.3.2.3.1i.

h. While observing the DVM, adjust the voltage adjustment pot on the power supply until the correct voltage reading is obtained.

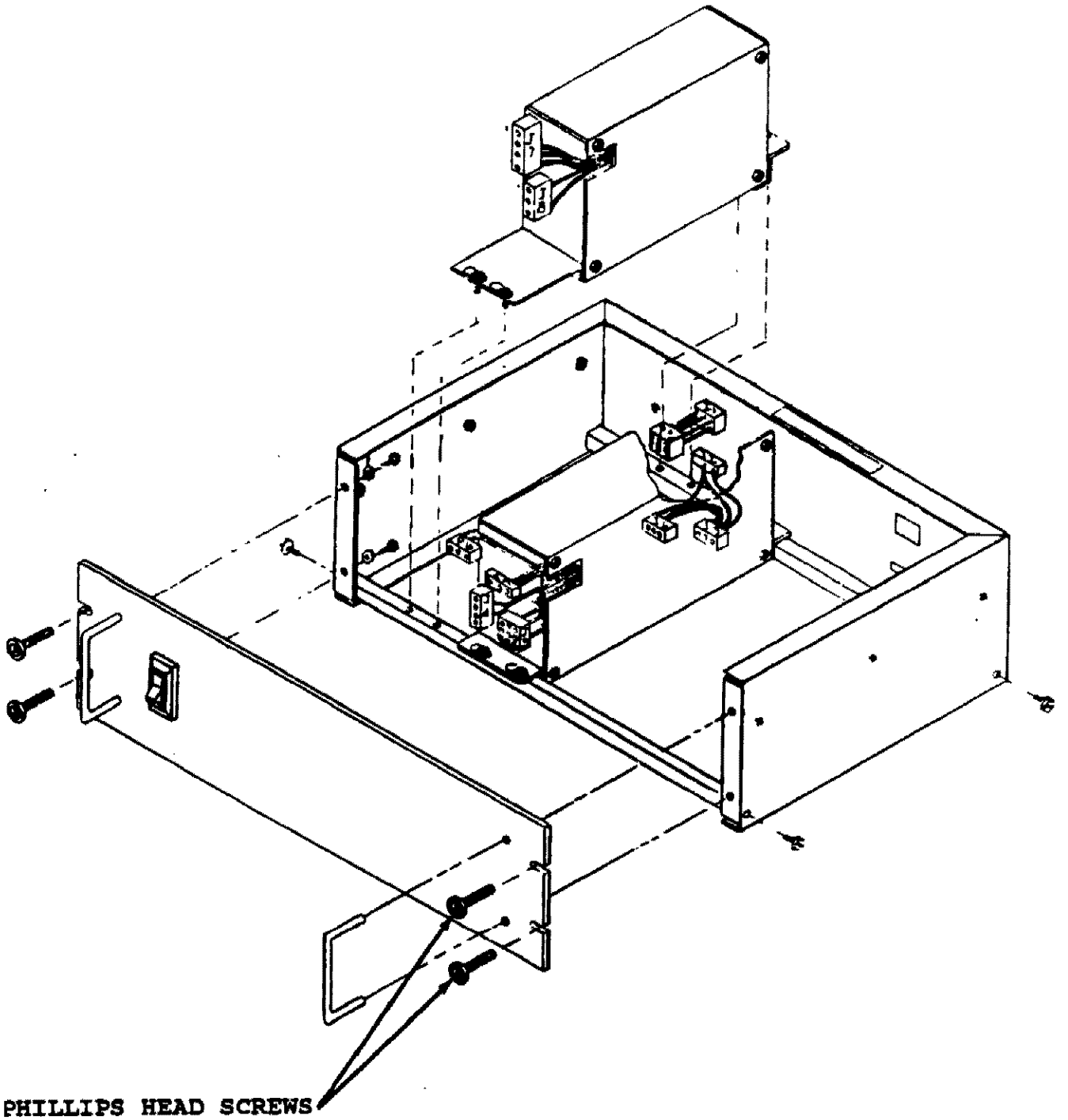


FIGURE 6-2. CHASSIS REMOVAL AND REPLACEMENT

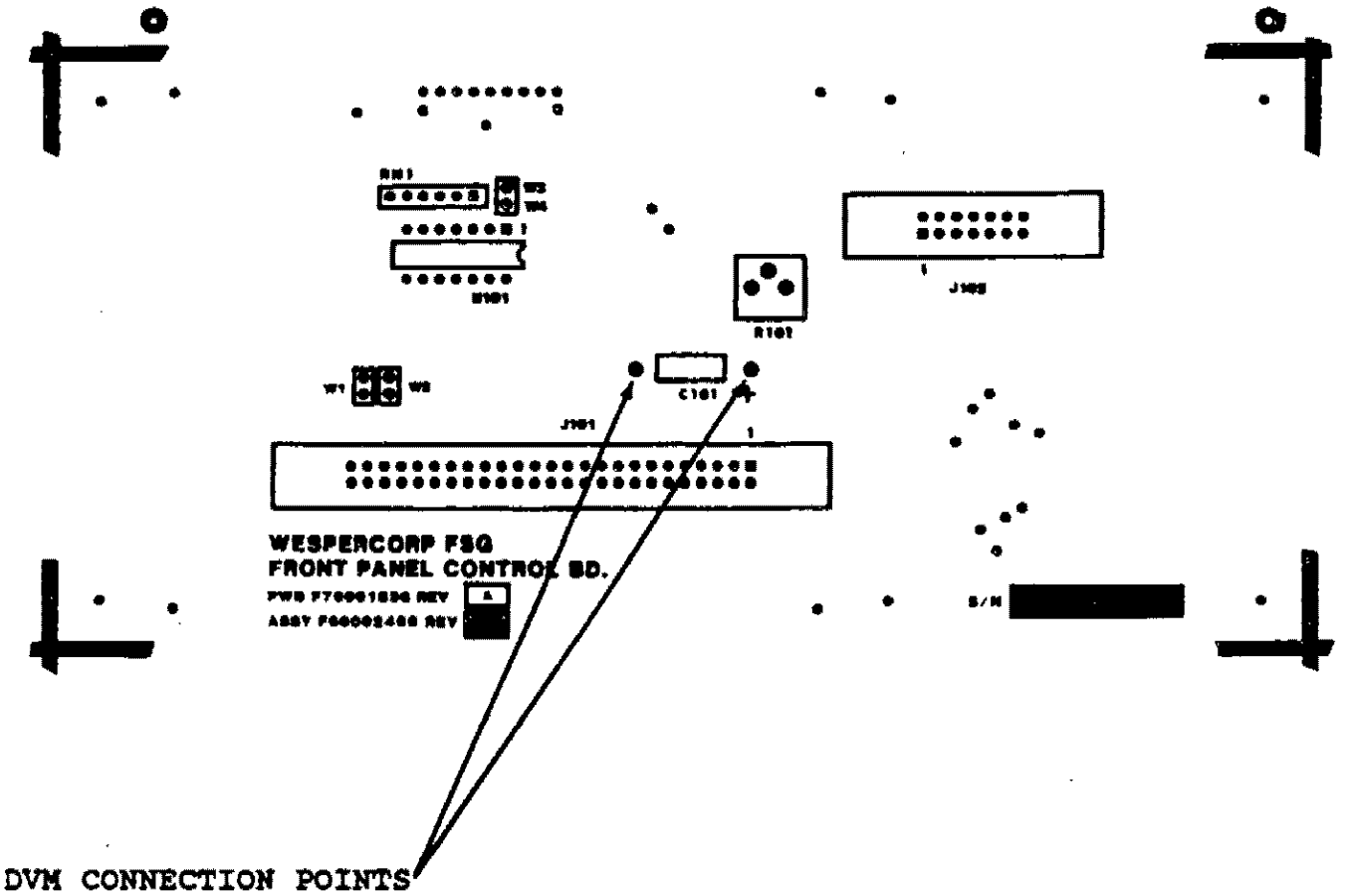


FIGURE 6-3. + 5 V DC MULTIBUS ADJUSTMENT PROCEDURES

NOTE

A clockwise turn on the voltage adjustment pot increases the voltage.

i. Turn OFF all power to the chassis under alignment.

j. Remove the DVM leads.

k. Perform steps in paragraph 6.3.2.2, if required, for power supply re-installation.

l. Return equipment to normal operating condition.

6.3.2.3.2 +12 V dc Multibus Adjustment Procedures (for RCU). The adjustment procedures for the +12 V dc Multibus are as follows:

a. Turn OFF all power to the chassis under adjustment.

b. Refer to the steps in paragraph 6.3.2.2 for power supply removal if required.

c. Connect a DVM to J8 pin 1 (ground) and J8 pin 4 (positive) on the Multibus backplane board. See figure 6-4.

d. Apply power to the Multibus.

e. Observe and record the reading on the DVM.

f. If the voltage is outside of tolerance (11.4 to 12.6 V dc) proceed to paragraph 6.3.2.3.2g. If the voltage is within tolerance proceed to paragraph 6.3.2.3.2h.

g. While observing the DVM, adjust the positive voltage adjustment pot on the power supply until the correct voltage reading is obtained.

NOTE

A clockwise turn ON the positive voltage adjustment pot increases the voltage.

h. Turn OFF all power to the chassis under alignment.

i. Remove the DVM leads.

j. Perform the steps in paragraph 6.3.2.2, if required, for power supply re-installation.

k. Return equipment to normal operating condition.

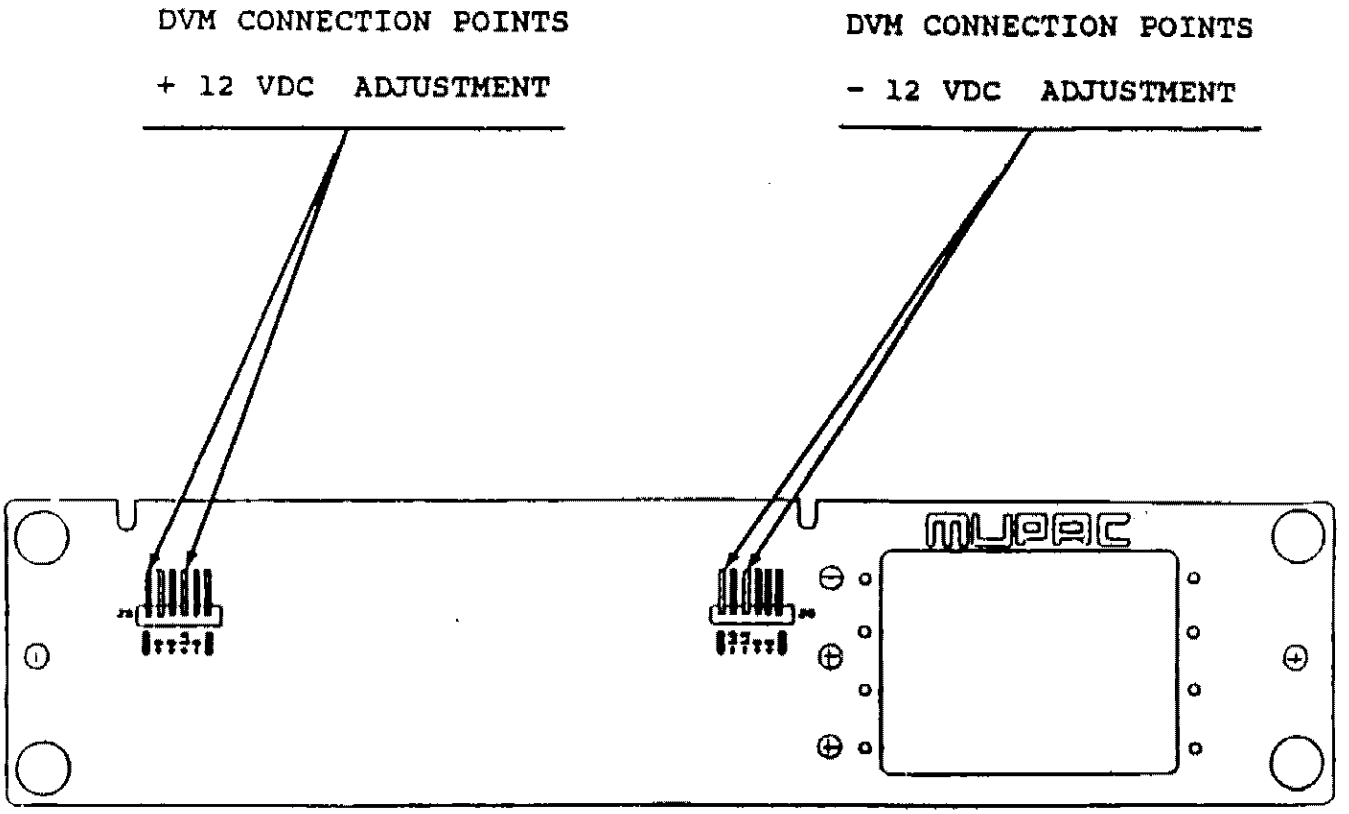
6.3.2.3.3 -12 V dc Multibus Adjustment Procedures (for RCU). The adjustment procedures for the -12 V dc Multibus are as follows:

a. Turn OFF all power to the chassis under adjustment.

b. Refer to the steps listed in paragraph 6.3.2.2 for power supply removal, if required.

c. Connect a DVM to J6 pin 1 (ground) and J6 pin 3 (negative) on the Multibus backplane board. See figure 6-4.

d. Apply power to the Multibus.



Multibus Chassis (Rear View)

FIGURE 6-4. ± 12 V DC MULTIBUS ADJUSTMENT PROCEDURES

e. Observe and record the reading on the DVM.

f. If the voltage is outside of tolerance (-11.4 to -12.6 V dc) proceed to paragraph 6.3.2.3.3g. If the voltage is within tolerance, proceed to paragraph 6.3.2.3.3h.

g. While observing the DVM, adjust the negative voltage adjustment pot on the power supply until the correct voltage reading is obtained.

NOTE

A clockwise turn on the negative voltage adjustment pot increases the voltage.

h. Turn OFF all power to the chassis under alignment.

i. Remove the DVM leads.

j. Perform the steps in paragraph 6.3.2.2, if required, for power supply re-installation.

k. Return equipment to normal operating condition.

6.3.2.3.4 +5 V dc BC Adjustment Procedures (CCU, and PCU). The adjustment procedures for the +5 V dc BC are as follows:

a. Turn OFF all power to the power supply assembly under adjustment.

b. Refer to the steps listed in paragraph 6.3.2.2 for power supply removal, if required.

NOTE

This adjustment has a twofold purpose: to set the operating range of the power supplies in the assembly and balance the two power supplies within the assembly.

c. Remove a center BC card from the BC cardcage; for example, the card in slot A6 or A7 if there are 12 BC cards. Connect a DVM to the BC board at the ground side of R1 and at the positive side of C1. See figure 6-5.

d. Re-install BC card into the slot from which it was removed.

e. Apply power to the BC cardcage, and turn ON all BCs in the BC cardcage.

f. Turn OFF circuit breaker B for the power supply assembly.

g. Adjust the voltage adjustment pot on the **A** +5 V dc power supply to 4.90 to 5.10 V dc.

h. Turn ON circuit breaker B for the power supply assembly.

i. Turn OFF circuit breaker A for the power supply assembly.

j. Adjust the voltage adjustment pot on the **B** +5 V dc power supply to 4.90 to 5.10 V dc.

k. Turn ON circuit breaker A for the power supply assembly.

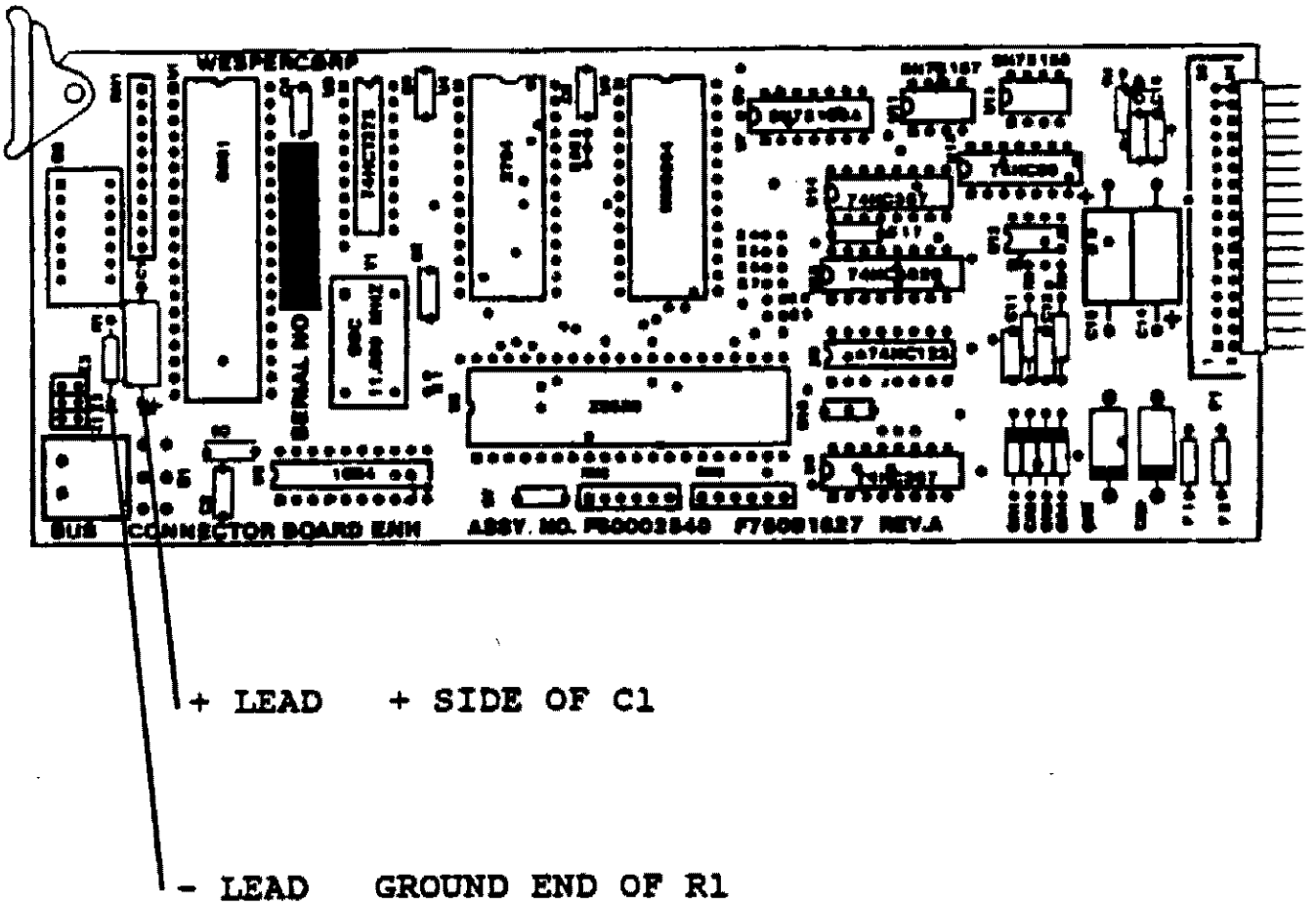


FIGURE 6-5. + 5 V DC BC ADJUSTMENT PROCEDURES

l. Observe the DVM. The combined +5 V dc power supply reading should not exceed +5.1 V dc. If the reading exceeds +5.1 V dc go to paragraphs 6.3.2.3.4f and g, and re-adjust the power supply slightly lower.

m. Turn OFF all power to the chassis under alignment.

n. Remove the DVM leads, and replace the removed BC.

o. Perform the steps in paragraph 6.3.2.2, if required, for power supply re-installation.

p. Return equipment to normal operating condition.

6.3.2.3.5 +12 V dc BC Adjustment Procedures for CCU. The adjustment procedures for the +12 V dc BC in the CCU only are as follows:

a. Turn OFF all power to the chassis under adjustment.

b. Refer to paragraph 6.3.2.2 for power supply removal, if required.

NOTE

This adjustment has a twofold purpose: to set the operating range of the power supplies in a chassis and balance the two power supplies within the chassis.

c. Connect the DVM positive lead to the positive side of CR3 or CR4 on the BC backplane. See figure 6-6.

d. Connect DVM negative lead to signal ground located on U36 pin 4 on the backplane. See figure 6-6.

e. Apply power to the BC cardcage.

f. Turn OFF circuit breaker B for the power supply chassis.

g. Adjust the positive voltage adjustment pot on the **A** +12 V dc power supply to 11.75 to 12.25 V dc.

h. Turn ON circuit breaker B for the power supply chassis.

i. Turn OFF circuit breaker A for the power supply chassis.

j. Adjust the positive voltage adjustment pot on the **B** +12 V dc power supply to 11.75 to 12.25 V dc.

k. Turn ON circuit breaker A for the power supply chassis.

l. Observe the DVM. The combined +12 V dc power supply reading should not exceed +12.25 V dc. If the reading exceeds +12.25 V dc, go to paragraphs 6.3.2.3.5f and g, and re-adjust the power supply slightly lower.

m. Turn OFF all power to the chassis under alignment.

n. Remove the DVM leads.

o. Perform steps in paragraph 6.3.2.2, if required, for power supply re-installation.

p. Return equipment to normal operating condition.

BUS CONNECTOR BACKPLANE

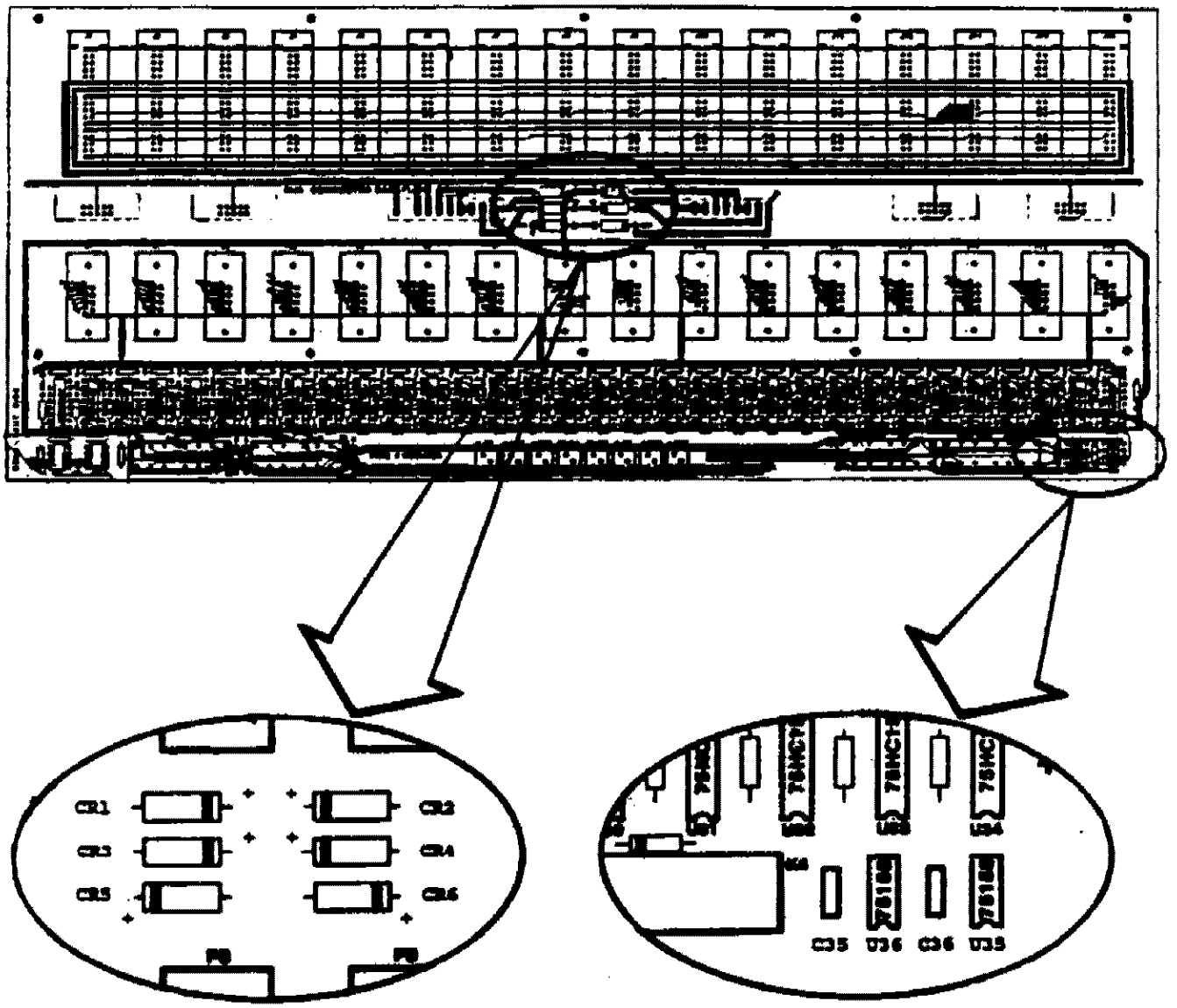


FIGURE 6-6. ± 12 V DC BC ADJUSTMENTS

6.3.2.3.6 -12 V dc BC Adjustment Procedures for CCU. The adjustment procedures for the -12 V dc BC in the CCU only are as follows:

a. Turn OFF all power to the chassis under adjustment.

b. Refer to paragraph 6.3.2.2 for power supply removal, if required.

NOTE

This adjustment has a twofold purpose: to set the operating range of the power supplies in a chassis and balance the two power supplies within the chassis.

c. Connect the DVM positive lead to the negative side of CR5 or CR6 on the BC backplane. See figure 6-6.

d. Connect the DVM negative lead to signal ground located at U36 pin 4 on the backplane. See figure 6-6.

e. Apply power to the BC cardcage.

f. Turn OFF circuit breaker B for the power supply chassis.

g. Adjust the negative voltage adjustment pot on the **A** -12 V dc power supply to -11.75 to -12.25 V dc.

h. Turn ON circuit breaker B for the power supply chassis.

i. Turn OFF circuit breaker A for the power supply chassis.

j. Adjust the negative voltage adjustment pot on the **B** -12 V dc power supply to -11.75 to -12.25 V dc.

k. Turn ON circuit breaker A for the power supply chassis.

l. Observe the DVM. The combined -12 V dc power supply reading should not exceed -12.25 V dc. If the reading exceeds -12.25 V dc, go to paragraphs 6.3.2.3.6f and g, and re-adjust the power supply slightly lower.

m. Turn OFF all power to the chassis under alignment.

n. Remove the DVM leads.

o. Perform steps in paragraph 6.3.2.2, if required, for power supply re-installation.

p. Return equipment to normal operating condition.

6.3.2.3.7 +5 V dc BC Adjustment Procedures for RCU. The adjustment procedures for the +5 V dc BC in the RCU only are as follows:

a. Turn OFF all power to the power supply chassis under adjustment.

b. Refer to paragraph 6.3.2.2 for power supply removal, if required.

c. Remove a center BC card from the BC cardcage; for example, the card in slot A6 or A7 if there are 12 BC cards. Connect a DVM to the BC board at the ground side of R1 and at the positive side of C1. See figure 6-5.

d. Re-install BC card into the slot from which it was removed.

e. Apply power to the BC cardcage.

f. Adjust the voltage adjustment pot on the +5 V dc power supply to 5.00 to 5.10 V dc.

g. Turn OFF all power to the chassis under alignment.

h. Remove the DVM leads, and replace the removed BC.

i. Perform the steps listed in paragraph 6.3.2.2, if required, for power supply re-installation.

j. Return equipment to normal operating condition.

6.3.2.3.8 CCU and RCU Power Supply Ripple Test Procedures

NOTE

The following procedures are applicable for all power supplies that are in the CCU and RCU (+5 V, +12 V, and –12 V).

NOTE

All ripple checks will be accomplished using the MOLEX 9-pin connector (J5) on the +5 V power supply in the power supply chassis. The ±12 V power supplies go through this jack also. Refer to Figure 11-16 for power supply pin outs.

a. Set up Oscilloscope adjustments as follows:

Channel Voltage — 100 mv
Channel ac/dc Coupling — ac
Horizontal Time — 1 ms
Trigger — ac Coupling

NOTE

It is recommended to use a needlepoint probe on the end of the scope lead and the associated ground wire.

b. Remove the four screws holding the power supply chassis to be checked.

c. Pull the power supply chassis out to gain access to power supply cable harnesses.

d. Locate J5 MOLEX connector that is connected to the +5 V power supply. J5 connector is the only 9-pin connector located in the chassis. A second one will exist if a second +5 V power supply exists in the chassis.

NOTE

Looking at the J5 end of the connector, position the connector with the locking clip at the bottom. Pin-1 will be located at the top left of the connector. A

single ridge on the left side of the plug will designate row 1. Row two will have 2 ridges and row 3 will have 3 ridges. Pins are read from left to right. Row 1 has pins 1, 2, and 3. Row 2 has pins **4,** 5, and 6. Row 3 has pins 7, ***8,*** and 9.

e. Insert scope ground lead into pin 1 of the connector.

f. Insert scope lead into the following pins to check for ripple:

1. +5 V Pin — 9
2. +12 V Pin — 2
3. –12 V Pin — 5

NOTE

If ±12 V power supplies do not exist in the chassis being tested, only scope pin-9.

g. Verify that the ac ripple does not exceed 250mv peak to peak.

h. Repeat steps d. through f. if a second +5 V power supply exists in the chassis.

i. Follow power supply removal and replacement procedures in section 6.3.2.2 if the ripple exceeds 250 mv.

j. Push down any cable harnesses that may have extended above the power supply chassis.

k. Slide chassis back into the rack.

l. Install four screws that were removed in step b.

m. Repeat steps b. through k. for remaining power supply chassis.

6.3.3 Multibus Front Panel Redundancy Operation

The procedures for checking the front panel multibus redundancy operation are as follows:

a. Check to see if any error message exists.

b. If error message exists, press MSG ACK to clear.

c. Verify both primary and secondary units are operating in normal mode:

(CCU XNP, PCU XNP).
(CCU XNS, PCU XNS).

Where X is A or B.

d. Press PRI/SEC key at primary unit.

e. Observe status change from S to P.

f. Press PRI/SEC key at primary unit.

g. Observe status change from S to P.

6.3.4 Verify Fan Operation

To verify fan operation, observe that the fan is rotating.

6.3.5 RFSP (10095/14) Maintenance Counter Operation

The maintenance counter of the IER-512 TFSP is used to instruct the technician of the need to perform periodic maintenance on the printer. There are two values associated with the maintenance counter. First there is the maintenance counter which records the number of strips printed from the printer. Second there is the maintenance interval. When the maintenance counter reaches the maintenance interval, the front panel display of the printer will display **SERVICE** every eight seconds for a short duration.

The printer will toggle between this display and the current status of the printer. When the technician sees this displayed, periodic maintenance should be carried out as specified in section 6.4.7.2 of this document. After maintenance is performed, the counter should be reset to zero. Section 6.3.5.2 gives procedures for resetting the maintenance counter after maintenance is performed. Section 6.3.5.1 gives the procedures for setting the maintenance interval.

6.3.5.1 RFSP (10095/14) Maintenance Counter Setup Procedure

The following procedures are used for setting the maintenance interval. The default value for the maintenance interval is ***50000.*** It is the site's prerogative to set the interval to what it deems necessary for the specific operating environment. The interval should not be set above ***50000*** as this will allow the printer to operate longer without a cleaning. **NOTE:** The maintenance interval can not be set below **10**.

NOTE

If the user feels that they have accidentally changed any parameters during these procedures and would like to exit and cancel any changes that may have been made press the On/Off Line key twice. If no parameters were changed then the printer will exit out of configuration mode and will display IER 512 OFF-LINE. If parameters were changed the display will show the VALIDATION? NO prompt. Press the On/Off Line key again to exit and cancel any changes that may have been made.

1. Power ON printer.
2. After printer finishes its self-test cycle, load paper stock. This procedure can not be accomplished without paper loaded into the printer.
3. Press the **On/Off Line** key to select the Off Line mode. Allow the alarm to stop.
4. Enter the configuration menu of the printer by pressing the front panel keys in the following order: **B - A - Blank Strip - B** (six times). Refer to figure 7-35 for layout of front panel keys.

NOTE

Do not pause for longer than 1 second between entering the **Blank Strip** key and the six successive **B** keys or the printer will enter one of the other

test modes, i.e., printing of configuration strip, or printing of the test documents.

5. After a short delay the display will read **"PASSWORD? 00000".**
6. Press the On/Off Line key.
7. The display area shall display **EMULATION parameters.**
8. Enter the **Hardware Parameters Menu** by pressing the A key **4** times.
9. Press the B key 4 times. The display will read **Platen Interval.**
10. Change the value of the maintenance Interval to the desired setting by using the **Blank Strip** key to change the value and the **A** key to advance the cursor.
11. Once the desired setting is selected, press the **On/Off Line** key twice.
12. The display shall read **VALIDATION? NO.** Press the **Blank Strip** key to save this change.

NOTE

If the values were not modified the printer will exit out of the configuration mode and display **IER 512 OFF-LINE.**

13. If parameters were changed the display will read **VALIDATION PERMANENT.** Press the **On/Off Line** key to exit.

6.3.5.2 RFSP (10095/14) Maintenance Counter Setup Procedure

The following procedures are used for resetting the maintenance counter. **The** resetting of this counter will not affect the master printer counter.

NOTE

If the user feels that they have accidentally changed any parameters during these procedures and would like to exit and cancel any changes that may have been made press the **On/Off Line** key twice. If no parameters were changed then the printer will exit out of configuration mode and will display **IER 512 OFF-LINE.** If parameters were changed the display will show the **VALIDATION? NO** prompt. Press the **On/Off Line** key again to exit and cancel any changes that might have been made.

1. Power ON printer.
2. After printer finishes its self-test cycle, load paper stock. This procedure can not be accomplished without paper loaded into the printer.
3. Press the **On/Off Line** key to select the Off Line mode. Allow the alarm to stop.
4. Enter the configuration menu of the printer by pressing the front panel keys in the following order: **B - A - Blank Strip - B** (six times). Refer to figure 7-35 for layout of front panel keys.

NOTE

Do not pause for longer than 1 second between entering the **Blank Strip** key and the six successive **B** keys or the printer will enter one of the other test modes, i.e., printing of configuration strip, or printing of the test documents.

5. After a short delay the display will read **"PASSWORD? 00000".**

6. Press the **On/Off Line** key.

7. The display area shall display **EMULATION parameters.**

a. Enter the **Events Counters Menu** by pressing the **A** key 8 times.

9. Press the **B** key one time. The display should read **Plat Maintenance.**

10. Change the value of the maintenance counter to zero by using the **Blank Strip** key to change the value and the **A** key to advance the cursor.

11. Once the desired value is selected, press the **On/Off Line** key twice.

12. The display shall read **VALIDATION? NO.** Press the **Blank Strip** key to save this change.

NOTE

If the values were not modified the printer will exit out of the configuration mode and display **IER 512 OFF-LINE.**

13. If parameters were changed the display will read **VALIDATION PERMANENT.** Press the **On/Off Line** key to exit.

6.4 CLEANING/PAINT TOUCH-UP PROCEDURES

6.4.1 CCU, PCU, and RCU Cabinets Cleaning Procedures

The cabinet cleaning procedures for the CCU, PCU, and RCU are as follows:

a. Wipe cabinet exterior with a damp, lint free cloth. Do not use harsh cleaning solvents.

b. Open front door. Clean front panel display and keypad with a damp, lint free cloth.

c. Open rear door. Wipe down front of power supply assemblies with a dry, lint free cloth.

d. Brush interior lightly with a soft bristled brush.

CAUTION

Do not use any cleaning agent on the EMI/RFI shield interconnect on cabinet doors. Lightly brush copper fingers and black conductor paint with a soft brush only, to prevent buildup of foreign materials. Use care when performing these maintenance tasks to avoid wiring damage, accidentally repositioning switches, or otherwise damaging the interior or exterior of the cabinet.

6.4.2 Fan Assembly Cleaning Procedure

The cleaning procedures for the fan assembly are as follows:

a. Unplug main power cord from ac distribution panel.

b. Clean surface of fans with a damp, lint free cloth. Gently vacuum cabinet interior using a shop type vacuum cleaner with a plastic wand.

c. Re-insert main power cord plug into ac distribution panel.

6.4.3 Cabinet Conductive Paint Touch-up Procedure

a. For internal application of touch-up paint, the conductive paint is applied to:

1. the EMI/RFI shield interconnect at top of cabinet,

2. the EMI/RFI shield interconnect at bottom of cabinet, and

3. the internal mating surfaces for cabinet front and back door.

b. When applying internal conductive paint on scratches:

1. Brush on epoxy mixture.

CAUTION

Four surfaces on the cabinets (see above) are coated with conductive paint to make electrical connection between various cabinet surfaces. If the conductive paint becomes chipped, it must be repaired as soon as possible to maintain the cabinet EMI/RFI integrity.

2. Conductive paint may be obtained from Graham Magnetics, North Richland Hills, Texas. The paint is a 2-part brush on epoxy mixture with an 8-hour life. Request Standard Metals conductive paint coating kit number HW-271 (Cobaloy P-212) conductive paint.

6.4.4 Cabinet Exterior Paint Touch-up Procedure

6.4.4.1 Deep Scratch Application. For deep scratch application of exterior touch-up paint, follow these steps:

a. Spray paint on a clean throw away surface, allow paint to congeal, then dab into scratch with a cotton swab and smooth out level with painted surface.

b. After paint dries, lightly buff with fine steel wool and wipe clean.

c. Apply finish spray coat to general area of scratch.

6.4.4.2 Light Scratch Application. For light scratch application of exterior touch-up paint, follow these steps:

a. Lightly buff scratched area and wipe surface clean.

b. Apply thin spray coats as required, allowing surface to dry completely between applications.

NOTE

Results are more satisfactory if paint is applied in several thin coats. A single heavy coat has a tendency to run.

c. Cabinet paint may be obtained from Cardinal Industrial Finishes, color Blue, number A-4103-25177 Air Dry (6-month shelf life). Standard Metals number TU-275.

6.4.5 CRT Cleaning Procedures

The cleaning procedures for the CRT are as follows:

a. Wipe the unit exterior with a damp, lint free cloth. Do not use harsh cleaning agents.

b. Dampen lint free cloth with alcohol or other antistatic cleaning agent, and gently wipe face of CRT.

c. Continue wiping face of CRT, changing cloth until no discoloration is seen on cloth.

6.4.6 RANK Cleaning Procedures

The cleaning procedures for the RANK are as follows:

a. Turn unit power OFF.

b. Wipe keyboard with a damp, lint free cloth. Do not use harsh cleaning agents.

c. Wipe keyboard enclosure with a damp, lint free cloth. Do not use harsh cleaning agents.

6.4.7 RFSP Cleaning Procedures

6.4.7.1 RFSP (FA 10095/2 and FA 10095/11) Cleaning Procedures. The cleaning procedures for the RFSP (FA 10095/2 and FA 10095/11) are as follows:

a. Turn unit power OFF.

b. Wipe exterior of printer with a damp, lint free cloth. Do not use harsh cleaning agents.

c. Gently vacuum printer interior, using a shop type vacuum cleaner with a plastic wand.

6.4.7.2 Cleaning Procedures for the RFSP (FA 10095/14)

6.4.7.2.1 RFSP (FA 10095/14) Printhead and Platen Cleaning Procedures. The cleaning procedures for the (FA 10095/14) printhead and platen are as follows:

a. Set the printhead to the maintenance position:

1. Remove power cord from the printer.

2. Lift the printhead lever up and remove paper stock.

3. Open the right hand side door.

4. Unlock the printhead support by moving it sidewise (direction of arrow in figure 6-7).

5. Rotate the assembly (direction of arrow in figure 6-8) to set it to the maintenance position.

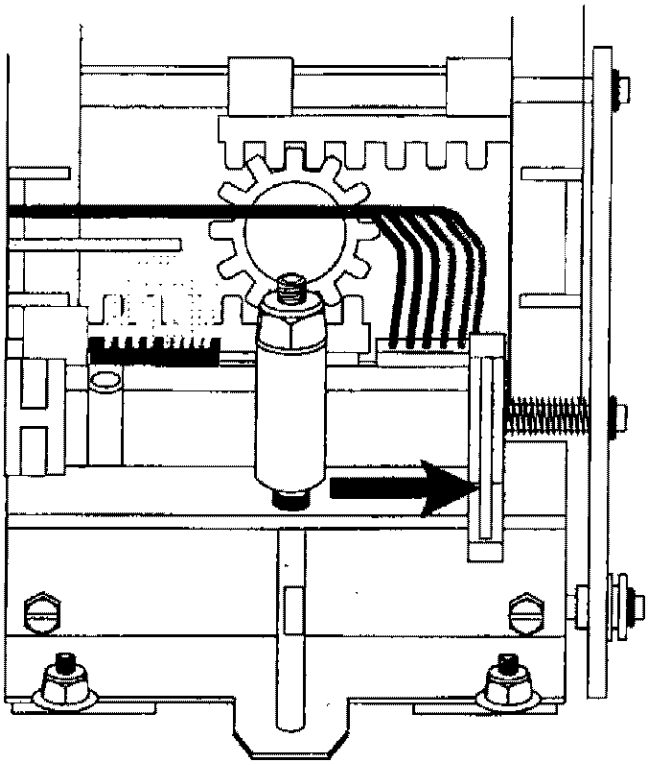


FIGURE 6-7. UNLOCK PRINTHEAD SUPPORT (TOP VIEW)

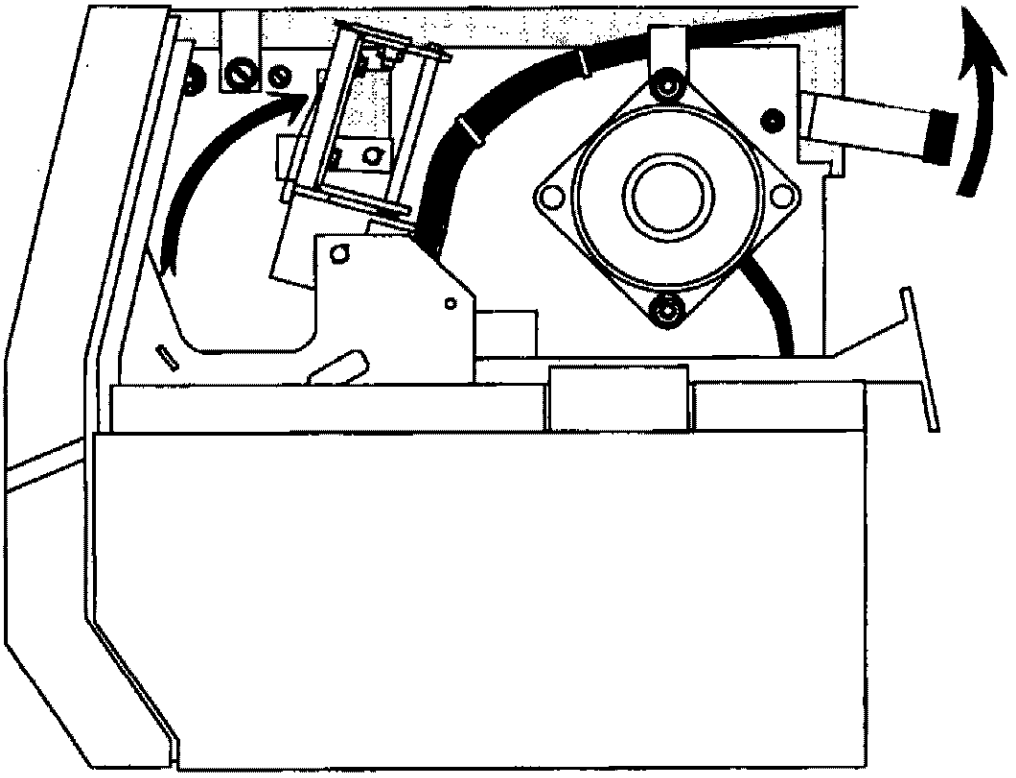


FIGURE 6-8. ROTATE PRINTHEAD ASSEMBLY (SIDE VIEW)

b. Cleaning procedures for the printhead and platen are as follows:

1. Use one of the soft cloths contained in the cleaning kit and moisten it with alcohol from the kit.

2. With the damp cloth clean the line of heating elements (item 2, figure 6-9) of the printhead.

3. Using a different soft cloth, moisten it with water and clean the entire surface of the platen [3]. To rotate the platen, turn knob [1].

NOTE

Do not use alcohol to clean the platen roller. Use of alcohol on the platen roller can cause premature wearing.

4. Inspect the platen roller for any wear. If an excessive amount of wear is noticed, replace the platen as described in paragraph 7.4.26.

c. Clean the paper path as follows:

1. Fold one of the soft cloths lengthwise in six.

2. Moisten the folded cloth with alcohol.

3. Insert the folded cloth into the paper guides to clean them over the entire length. Perform several back and forth movements.

d. Set the printhead back to the operating position:

1. Rotate the printhead back until it locks into the operating position.

2. Close the right-hand side door.

3. Connect the printer to power and power ON.

4. Load the paper stock and print the printhead adjustment test document and check for print degradation. If print is degraded then change printhead. Refer to section 7.4.24 for procedures.

6.4.7.2.2 RFSP (FA 10095/14) Cutter Blade and Blade-Down Sensor Cleaning Procedures. The cleaning procedures for the RFSP (FA 10095/14) cutter blade and blade-down sensor are as follows:

a. Remove power cord from the printer.

b. Lift the printhead lever up and remove paper stock.

c. Open the right hand side door.

d. Loosen the front panel mounting hardware to be able to clear the front panel off the printer front (see figure 6-10). Be careful not to disconnect the control panel flat cable.

e. Remove one of the soft cloths of the cleaning kit and moisten it with alcohol from the cleaning kit.

f. Use the dampened cloth and cautiously clean the cutter blade and the cutter assembly (shaded parts in figure 6-11).

NOTE

The cutter blade edge is sharp.

g. Remove the printer lower cover as shown in figure 6-12.

h. Remove one of the swabs contained in the cleaning kit and moisten it with alcohol from the cleaning kit.

i. Locate the blade down sensor behind the cutter motor. The sensor can be reached through the rear of the printer (see figure 6-13).

j. Rotate the cutter motor hub to gain access to the blade down sensor. Clean the blade down sensor with the moistened swab.

k. Remove dust from the printer interior. Pay special attention to mechanical assemblies.

l. Install the lower cover and the front panel by reversing the removal procedures.

m. Place the printhead back to the operating position.

n. Restore power to the printer and load paper stock. Print out the printer configuration to check for correct printer operation.

6.4.7.2.3 RFSP (FA 10095/14) Platen Roller Brush Cleaning Procedures. The cleaning procedures for the RFSP (FA 10095/14) platen roller brush are as follows:

a. Remove printer lower cover, see figure 6-12.

b. Remove retaining screw (item #2, figure 6-14).

c. Remove platen roller brush (item #1, figure 6-14).

d. Using a vacuum or compressed air, clean all paper dust from the brush.

e. Reassemble printer in reverse order.

6.5 SPECIAL MAINTENANCE PROCEDURES

No special maintenance procedures are required for the CCU, PCU, and RCU configurations. Any special maintenance tasks associated with the CRT, RFSP, and RANK can be found in the FDIO peripheral equipment manuals.

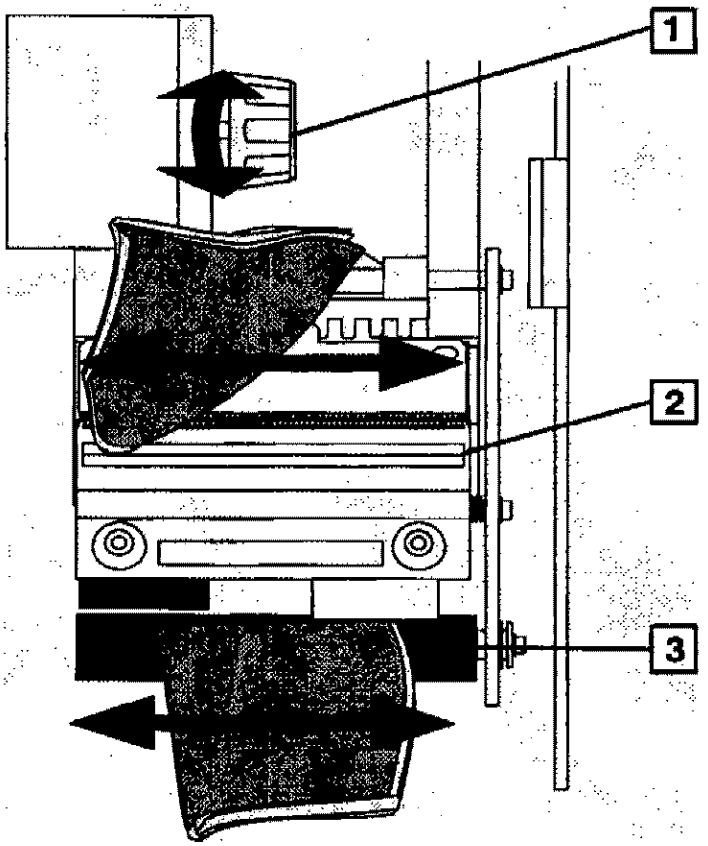


FIGURE 6-9. CLEANING PROCEDURES FOR PRINTHEAD AND PLATEN

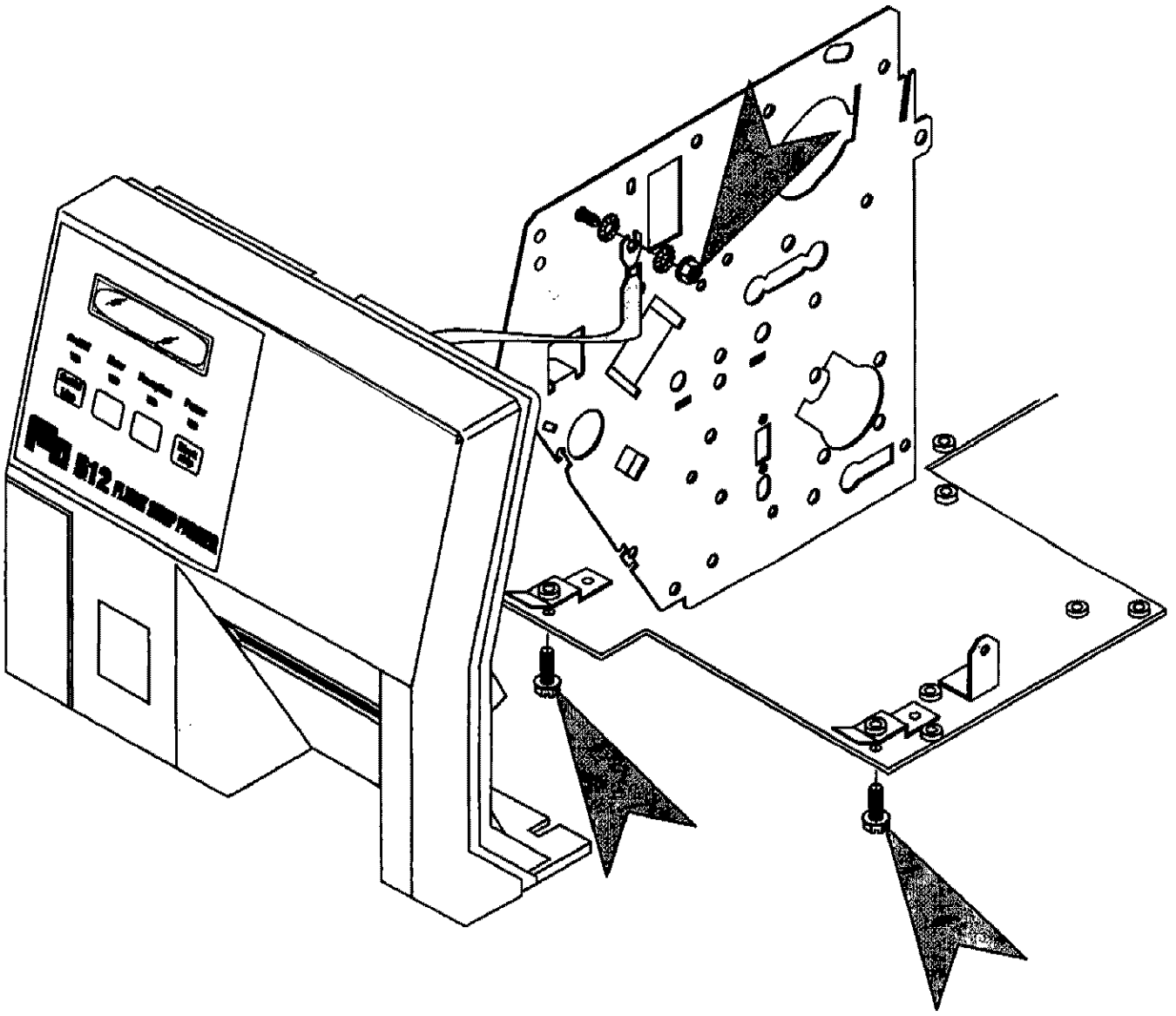


FIGURE 6-10. REMOVAL OF FRONT PANEL

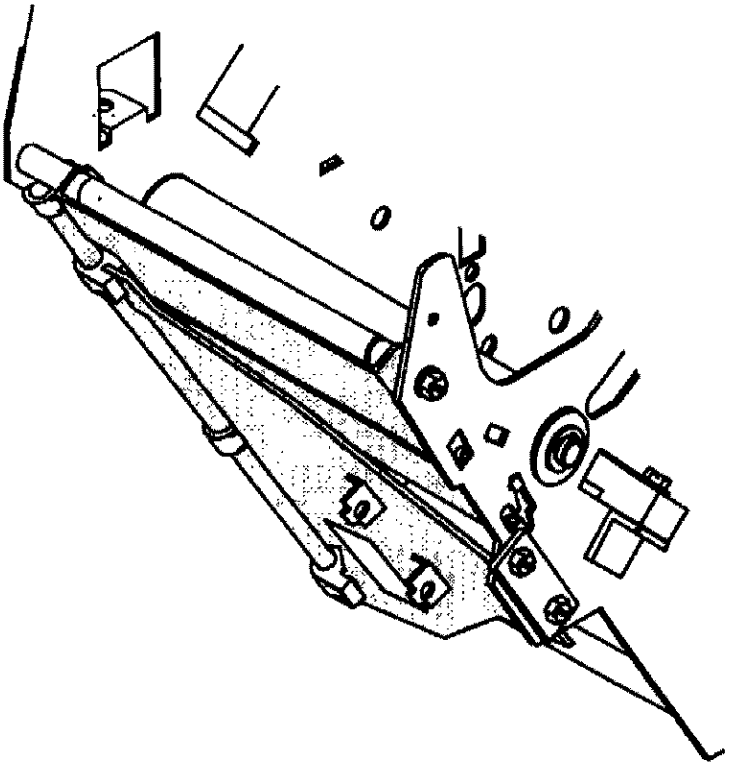


FIGURE 6-11. CLEANING PROCEDURE FOR CUTTER BLADE AND ASSEMBLY

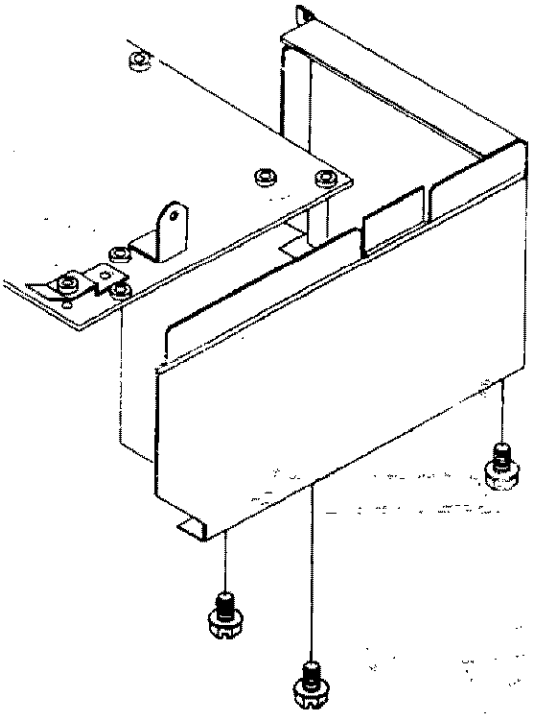


FIGURE 6-12. REMOVAL OF PRINTER LOWER COVER

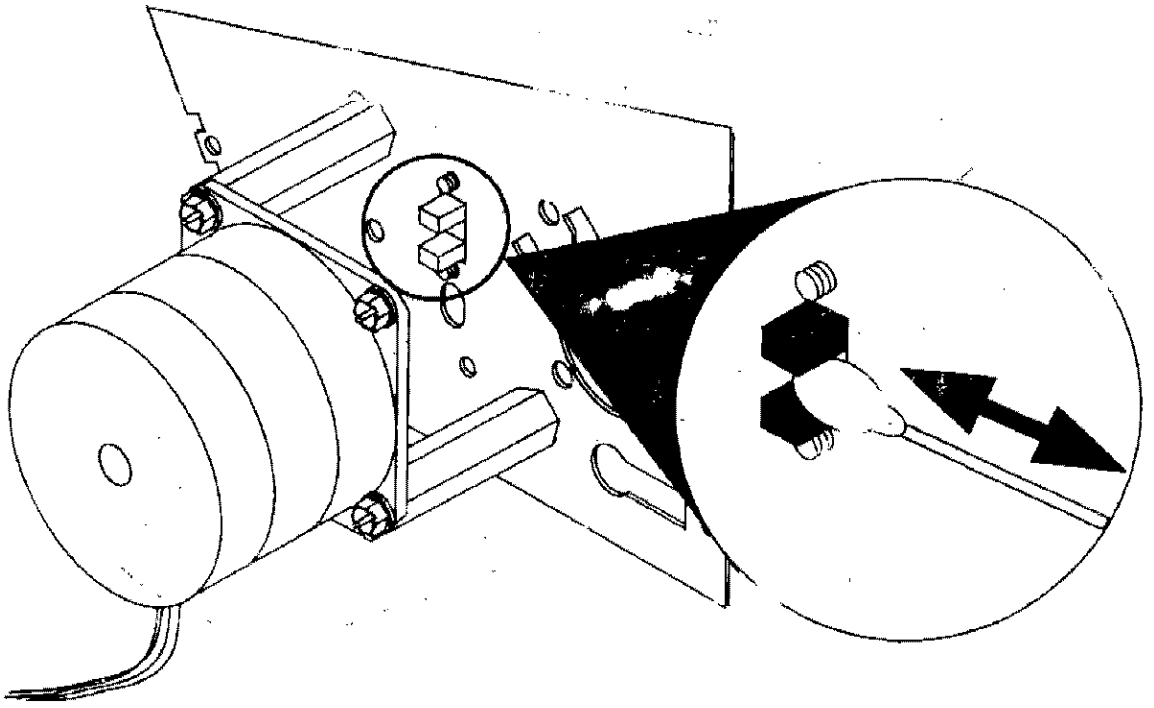


FIGURE 6-13. CLEANING PROCEDURE FOR BLADE DOWN SENSOR

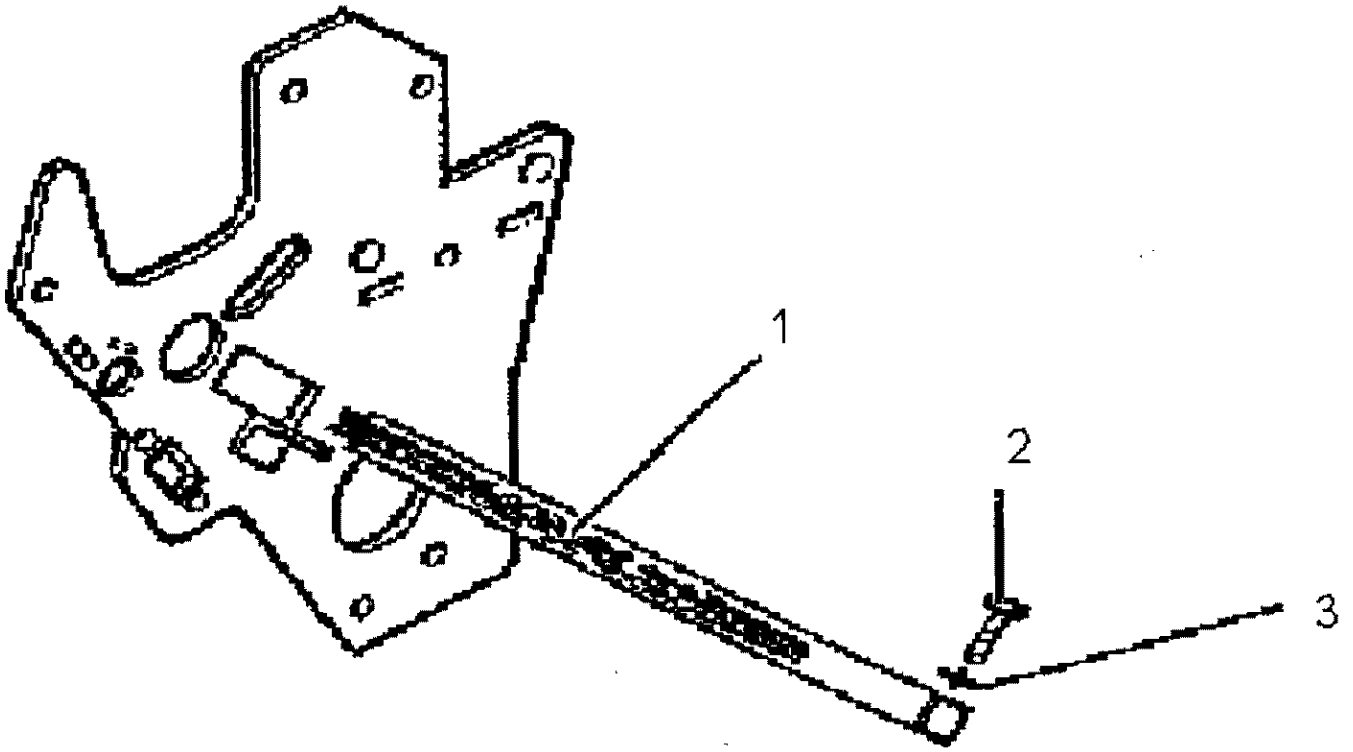


FIGURE 6-14. RFSP (FA 10095/14) PLATEN ROLLER BRUSH REMOVAL

7.0 CORRECTIVE MAINTENANCE

7.1 INTRODUCTION

This section provides step-by-step instructions to diagnose, isolate, and correct faults in the FDIO system. Included are built-in diagnostic program descriptions, troubleshooting procedures, and removal and replacement procedures for defective assemblies, subassemblies, circuit boards, and modules.

Schematic diagrams, circuit board layout pictorials, power distribution diagrams, and wiring diagrams for FDIO system boards, modules, and subassemblies are located in sections 2.0 and 11.0 of this document. Refer to the vendor's service/technical manuals for detailed information on peripherals and modems.

Mandatory maintenance requirements for the FDIO system are located in section 6.0. After replacement of any peripheral, board, module, or sub-assembly, applicable diagnostic programs (see paragraph 7.2.1.2) must be run to verify correct operation of the system.

7.2 ONSITE CORRECTIVE MAINTENANCE

The following paragraphs identify the source of operation problems in the FDIO system. FDIO system problems are classified into the following five categories:

1. Control unit,
2. power,
3. peripheral,
4. telephone line, and
5. NAS computer.

Troubleshooting should initially be isolated to one of these areas. The following paragraphs provide information in identifying the problem source. Control unit status indicators are described in paragraph 3.2.

7.2.1 Isolating Control Unit Problems

The fault isolation tree (see paragraph 7.2.1.1), provides help with isolating a suspected control unit or FDIO system problem using fault isolation built-in diagnostic programs and the SEL.

7.2.1.1 Fault Isolation Tree. If an error code is displayed on the Multibus front panel of the control unit, use table 7-1, table 7-2 and the fault isolation tree, figure 11-30, sheets 1 through 6 to identify the technical problem. The six headings and the error numbers in table 7-1 are defined as follows:

a. Level: non-fatal (0) or fatal (1)

b. Device: indicates whether a peripheral device is involved (yes or no)

c. NAS Category: 1, 2, or 3

d. RCU: indicates whether an RCU is involved (yes or no)

e. Int Req: data prepended to category 1 and 2 messages

f. Error Text Message: shown as it appears in the table

If there is an error that doesn't show up on the front panel, i.e., ac power problems, dc power problems, dual primary, dual secondary, or certain peripheral problems, refer to PCB Fault Isolation Test Procedures FDIO CLIN-54.

7.2.1.2 Diagnostics. Each Multibus card cage assembly contains built-in DIAG programs which automatically test operation in all seven cabinet configurations and associated peripheral devices. Each Multibus assembly contains three types of diagnostic programs to isolate problems. These programs are summarized below:

1. Power-up diagnostics — initiated as power is applied to the CCU, PCU, or RCU control cabinet assembly. Tests the basic operation of the Multibus card cage assembly iSBC 88/45 board.

2. Background diagnostics — initiated when the control unit is operating in normal mode. Continuously tests the basic operation of the iSBC 88/45 and utility boards as a background task of the real-time executive program.

3. Front panel diagnostics — initiated by pressing DIAG key on the front panel keypad. Individual test routines are initiated by pressing the key(s) specified in the display prompt.

The SEL allows maintenance personnel to observe the results of power-up and background DIAG tests (see paragraphs 7.2.1.2.1 and 7.2.1.2.2).

TABLE 7-1. SYSTEM ERROR TABLE

Error#	Level	Device	NAS Category	RCU	Int Req	Error Text Message
01	1	N	1	N	Y	* PRIMARY LAN FAILED
02	0	N	1	Y	Y	RCU LAN FAILURE
03	0	Y	1	N	N	INDETERMINATE ERROR
04	0	Y	1	Y	N	INDETERMINATE ERROR
05	—	—	—	—	—	RESERVED
06	0	Y	1	Y	Y	PRINTER OUT OF PAPER
07	0	Y	1	N	N	ILLEGAL DEVICE ADDRESS
08	0	Y	1	Y	N	ILLEGAL DEVICE ADDRESS
09	0	Y	1	Y	N	MESSAGE TIMED OUT
10	0	Y	1	N	N	MESSAGE TIMED OUT
11	—	—	—	—	—	RESERVED
12	—	—	—	—	—	RESERVED
13	—	—	—	—	—	RESERVED

TABLE 7-1. SYSTEM ERROR TABLE (Continued)

Error#	Level	Device	NAS Category	RCU	Int Req	Error Text Message
14	—	—	—	—	—	RESERVED
15	—	—	—	—	—	RESERVED
16	0	Y	1	N	Y	MODEM LINK FAILING
17	0	Y	1	N	Y	BC FAILURE
18	0	Y	1	Y	Y	BC FAILURE
19	0	N	1	N	Y	ICL CHANNEL FAILURE (PRIMARY)
20	1	N	3	N	Y	ICL CHANNEL FAILURE (SECONDARY)
21	0	N	1	N	Y	PRIMARY FSE TIMED OUT
22	0	N	3	N	Y	SECONDARY FSE TIMED OUT
23	0	N	1	N	N	CONTROL UNIT SWITCH (FORCED)
24	0	N	1	N	N	CONTROL UNIT SWITCH (NORMAL)
25	0	N	2	N	Y	* FSE PRIMARY UNIT FAILURE
26	0	N	2	N	Y	* FSE SECONDARY UNIT FAILURE
27	0	N	1	N	N	CONTROL UNIT SWITCH (F.P.)
28	0	N	2	N	Y	CONTROL UNIT SWITCH (FAILURE)
29	1	N	2	N	Y	* PRIMARY CPU TEST FAILED
30	1	N	2	N	Y	* SECONDARY CPU TEST FAILED
31	—	—	—	—	—	RESERVED
32	1	N	1	N	Y	* PRIMARY ROM FAILURE
33	1	N	3	N	N	SECONDARY ROM FAILURE
34	—	—	—	—	—	RESERVED
35	1	N	1	N	Y	* PRIMARY RAM FAILURE
36	1	N	3	N	N	SECONDARY RAM FAILURE
37	—	—	—	—	—	RESERVED
38	0	N	1	N	Y	* ICL CLEAR TO SEND ERROR
39	1	N	2	N	Y	EEPROM FAILURE

TABLE 7-1. SYSTEM ERROR TABLE (Continued)

Error#	Level	Device	NAS Category	RCU	Int Req	Error Text Message
40	0	N	2	N	N	* CANNOT DOWNLOAD TO SECONDARY
41	—	—	—	—	—	RESERVED
42	0	N	1	N	N	SWITCH NOT ALLOWED
43	0	N	3	N	N	NAS MESSAGE TOO LONG
44	—	—	—	—	—	RESERVED
45	—	—	—	—	—	RESERVED
46	0	N	3	N	N	MODEM TRANSMITTER FAILED
47	0	N	3	N	N	MODEM RECEIVER FAILED
48	0	N	3	N	N	EXCESSIVE ERRORS ON GPI TRANSMITS
49	0	N	3	N	N	RESERVED
50	0	N	3	N	N	UNABLE TO ASSIGN TRANSMITTER (UNIT=2ND)
52	—	—	—	—	—	RESERVED
52	—	—	—	—	—	RESERVED
53	—	—	—	—	—	RESERVED
54	0	N	3	N	N	EXCESSIVE PARITY ERRORS GPO
55	0	N	3	N	N	RCU/CCU CHECKSUM ERROR
56	0	N	3	N	N	PRI/SEC LOOPBACK FAILURE
57	0	N	3	N	N	GPI PARITY ERROR
58	0	N	3	N	N	BAD MESSAGE RECEIVED BY GPO PRIMARY
59	0	N	3	N	N	GPO SECONDARY FAILURE
60	0	N	3	N	N	REJECT MESSAGE RECEIVED FROM PRIMARY
61	0	N	3	Y	N	RCU EEPROM FAILURE
62	—	—	—	—	—	RESERVED
63	0	Y	1	N	N	ILLEGAL PERIPHERAL CONNECTED
64	0	Y	1	N	N	PERIPHERAL IS NOT READY
65	0	Y	1	N	N	PARITY ERROR ENCOUNTERED
66	0	Y	1	N	N	PERIPHERAL IS OFFLINE

TABLE 7-1. SYSTEM ERROR TABLE (Continued)

Error#	Level	Device	NAS Category	RCU	Int Req	Error Text Message
67	0	Y	1	N	N	DEVICE FAULT
68	0	Y	1	N	N	BC IS BUSY TOO LONG
69	0	N	3	N	Y	WARNING: INVALID CONFIGURATION
70	—	—	—	—	—	RESERVED
71	0	N	3	N	N	INTERNAL FAILURE — SECONDARY DEACTIVATED
72	0	N	3	N	N	INTERNAL FAILURE — PRIMARY AND NO BACKUP
73	—	—	—	—	—	RESERVED
74	0	N	3	N	N	WARNING: FP DISABLED VIA NAS
75	0	N	3	N	N	WARNING: FP ENABLED VIA NAS
76	0	N	2	N	N	FSE CABLE INCORRECT OR MISSING
77	0	N	1	N	Y	SPECIAL READ (FORCED SWITCH) FAILURE
78	0	N	1	N	Y	ICL LOOPBACK FAILURE
79	0	Y	1	Y	Y	BC CHECKSUM ERROR

TABLE 7-2. SYSTEM ERRORS DEFINED

01 * Primary LAN Failed — NAS C1/FP — **Int Req**
A LAN loop failure has been detected in the primary control unit of a CCU or PCU.

02 RCU LAN Failure — NAS C1/FP — **Int Req**
A LAN loop failure has been detected in an RCU.

03 Indeterminate Error — NAS C1/FP
The LAN firmware has detected a peripheral error in a PCU or CCU. The peripheral device status table is scanned and a Text Ack with Error (type 11) message was returned but no peripheral error status could be determined.

04 Indeterminate Error — NAS C1/FP
The LAN FW has detected a peripheral error in an RCU. The peripheral device status table is scanned and a Text Ack with Error (type 11) message was returned but no peripheral error status could be determined.

TABLE 7-2. SYSTEM ERRORS DEFINED (Continued)

05	Reserved
06	Printer Out of Paper — NAS C1/FP — **Int Req** The LAN firmware has detected an **out of paper** bit set in the peripheral status word of a PCU or RCU.
07	Illegal Device Address — NAS C1/FP The RCU detects an invalid destination.
08	Illegal Device Address — NAS C1/FP The CCU/PCU detects an invalid destination.
09	Message Timed Out — NAS C1/FP A CCU/PCU associated peripheral fails to acknowledge a message within an allotted time.
10	Message Timed Out — NAS C1/FP An RCU associated peripheral fails to acknowledge a message within an allotted time.
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	Reserved
16	Modem Link Failing — NAS C1/FP — **Int Req** The CCU BC firmware detects a permanent timeout condition due to hardware/Telco problems.
17	BC Failure — NAS C1/FP — **Int Req** The LAN firmware examined the CCU/PCU BC status word and found either: a. BC not ready, or b. BC checksum error
18	BC Failure — NAS C1/FP — **Int Req** The LAN firmware examined the RCU BC status word and found either: a. BC not ready, or b. BC checksum error
19	ICL Channel Failure (Primary) — NAS C1/FP — **INT Req** The ICL firmware has detected a timeout or data mismatch condition on ICL channel A and channel B loopback tests.

TABLE 7-2. SYSTEM ERRORS DEFINED (Continued)

20	ICL Channel Failure (Secondary) — NAS C3/FP — **Int Req** The ICL firmware has detected a timeout or data mismatch condition on ICL channel A and channel B loopback tests.
21	Primary FSE Timed Out — NAS C1/FP — **Int Req** FSE Watchdog timer is not updated in time by the primary unit.
22	Secondary FSE Timed Out — NAS C3/FP — **Int Req** FSE Watchdog timer is not updated in time by the secondary unit.
23	Control Unit Switch (Forced) — NAS C1/FP NAS raised GPI device control line 4 forcing a control unit switch.
24	Control Unit Switch (Normal) — NAS C1/FP NAS initiated a control unit switch via a Type 30 Invoke Backup message.
25	* FSE Primary Unit Failure — NAS C2/FP — **Int Req** The FSE of the secondary control unit detects a failure in the primary. Secondary switches to primary, deactivates the old primary and operates as a single unit.
26	* FSE Secondary Unit Failure — NAS C2/FP — **Int Req** The FSE of the primary control unit detects a failure in the secondary. The primary deactivates the old secondary and operates as a single unit.
27	Control Unit Switch (F.P.) — NAS C3/FP A front panel control unit switch has been processed.
28	Control Unit Switch (FAILURE) — NAS C2/FP — **Int Req** FSE detected the control unit to be unavailable during power up. Control unit operation is deactivated.
29	* Primary CPU Test Failed — NAS C2/FP — **Int Req** Primary unit detected an internal failure and deactivated. If available, the secondary unit is brought online. If the secondary is unavailable, error message 72 (Internal Failure — Primary and No Backup) is displayed on the front panel.
30	* Secondary CPU Test Failed — NAS C2/FP — **Int Req** The secondary control unit detects a failure in the primary, however the primary has not failed which indicates the secondary has failed. The secondary control unit deactivates and error message 71 (Internal Fail — Secondary Deactivated) is posted to the front panel.
31	Reserved
32	* Primary ROM Failure — NAS C1/FP — **Int Req** A calculated checksum failure has been detected in the primary control unit (or RCU) ROM by background DIAGs.

TABLE 7-2. SYSTEM ERRORS DEFINED (Continued)

33 Secondary ROM Failure — NAS C3/FP
A calculated checksum failure has been detected in the secondary control unit ROM by background DIAGs.

34 Reserved

35 * Primary RAM Failure — NAS C1/FP — **Int Req**
A compliment/exclusive OR failure has been detected in the primary control unit (or RCU) RAM by background DIAGs.

36 Secondary RAM Failure — NAS C3/FP
A compliment/exclusive OR failure has been detected in the secondary control unit RAM by background DIAGs.

37 Reserved

38 * ICL-Clear To Send Error — NAS C1/FP — **Int Req**
ICL firmware in the primary control unit detects CTS signal missing. Could be caused by the ICL cable missing or improperly seated.

39 EEPROM Failure — NAS C2/FP — **Int Req**
The site configuration data has been erased from the EEPROM. The EEPROM needs to be reconfigured through the RECN button on the front panel.

40 * Cannot Down Load to Secondary — NAS C2/FP
ICL failed to establish a download mode which negates message synchronization between primary and secondary control units.

41 Reserved

42 Switch Not Allowed — NAS C1/FP

a. A front panel switch request was entered from a secondary control unit.

b. A front panel switch request was entered from a primary control unit and no secondary is online.

c. Primary control unit detects an ICL failure during a requested switch.

43 NAS Message Too Long — NAS C3/FP
Primary control unit detects message overflow and signals the NAS with DSL5. NAS aborts the current message.

44 Reserved

45 Reserved

46 Modem Transmitter Failed — NAS C3/FP
Transmissions to the CCU from the RCU have been attempted five times and failed.

TABLE 7-2. SYSTEM ERRORS DEFINED (Continued)

47 Modem Receiver Failed — NAS C3/FP
The RCU attempted to transmit a message two times and failed. The RCU failed to receive the ADCCP link-level acknowledgement from the CCU.

48 Excessive Errors on GPI Transmits — NAS C3/FP
Excessive errors have occurred on the same GPI input message. Works in conjunction with error message 57. DSL3 (Request Resend) line has been raised on the successive transmissions of the message.

49 Reserved

50 Unable To Assign Transmitter (Unit=2nd) — NAS C3/FP

a. When reported by primary, indicates secondary failed to assume primary status on a control unit switch.

b. When reported by the secondary, indicates the transmitter function was not acquired.

51 Reserved

52 Reserved

53 Reserved

54 Excessive Parity Errors GPO — NAS C3/FP
Two successive parity errors detected on the same message. FDIO GPO interface logic reinitialized.

55 RCU/CCU Checksum Error — NAS C3/FP
CCU computed checksum does not match checksum stored in RANK message.

56 Pri/Sec Loopback Failure — NAS C3/FP
Internal control unit test pattern data mismatch or parity error detected in **primary** control unit.

57 GPI Parity Error — NAS C3/FP
GPI loopback test for parity has failed. This test is run as a result of DSL3 being raised.

58 Bad Message Received By GPO Primary — NAS C3/FP
Primary control unit tests for invalid message format, raises DSL6 (request resend) to NAS when message does not:

a. end with ETX,

b. have minimum message length of 12 bytes,

c. contain STX in header, or

d. contain all legal characters in message.

TABLE 7-2. SYSTEM ERRORS DEFINED (Continued)

59	GPO Secondary Failure — NAS C3/FP Primary/Secondary checksum mismatch. DSL6 raised to NAS which requests NAS to resend the message to the control unit.
60	Reject Message Received from Primary — NAS C3/FP Primary control unit informed secondary to reject the last message. (Used in conjunction with error message 59.)
61	RCU EEPROM Failure — NAS C3/FP The site configuration data has been erased from the EEPROM. The EEPROM needs to be reconfigured through the RECN button on the front panel.
62	Reserved.
63	Illegal Peripheral Connected — NAS C1/FP The BC status indicates an illegal peripheral is connected. i.e., an RFSP connected to a BC with a RANK address.
64	Peripheral Is Not Ready — NAS C1/FP The PCU/RCU BC status word indicates the attached peripheral is not ready during the last attempted access.
65	Parity Error Encountered — NAS C1/FP The BC peripheral status reports a parity error has occurred during the last peripheral data transfer.
66	Peripheral Is Offline — NAS C1/FP The BC peripheral status reports an offline condition existed during the last attempted peripheral access.
67	Device Fault — NAS C1/FP The BC peripheral status reports a device fault, i.e., Headjam, condition existed during the last attempted peripheral access.
68	Bus Connector is Busy Too Long — NAS C1/FP BC Status indicates busy after two retries during a specified time parameter, indicating the busy condition has been in effect too long.
69	Warning: Invalid Configuration — NAS C3/FP — **Int Req** The RCU detected minimum configuration requirements of at least one RANK and one RFSP or CRT not available.
70	Reserved.
71	Internal Failure — Secondary Deactivated — NAS C3/FP An internal failure is detected in the secondary control unit. The unit deactivates itself. (See error message 30.)

TABLE 7-2. SYSTEM ERRORS DEFINED (Continued)

72	Internal Failure — Primary and No Backup — NAS C3/FP Primary unit detects an internal failure with no complimentary control unit to switch to. (See error message 29.)
73	Reserved.
74	Warning: FP Disabled Via NAS — NAS C3/FP A front panel disable command has been received from NAS.
75	Warning: FP Enabled Via NAS — NAS C3/FP A front panel enable command has been received from NAS.
76	FSE Cable Incorrect or Missing — NAS C2/FP
77	Special Read (Forced Switch) Failure — NAS C1/FP — **Int Req** NAS has detected a solid error (undefined) on the FDIO/NAS interface operation and issued a forced switch to the secondary.
78	ICL Loopback Failure — NAS C1/FP — **Int Req** A time-out or data mismatch was detected when ICL channels A and B were operated in loopback mode. (Loopback mode verifies control unit operation without a redundant control unit.)
79	BC Checksum Error — NAS C1/FP — **Int Req** The checksum that was calculated by the BC is different than the checksum stored in the message. If a backup device is specified, the message will be rerouted. If no backup or reroute is unsuccessful, a NAK will be generated.

7.2.1.2.1 Power-up Diagnostics. The power-up Diagnostics are executed in two phases. Phase I Diagnostics are executed immediately when dc power is switched ON to the Multibus card cage assembly of a CCU, PCU, or RCU cabinet assembly. Phase I Diagnostics (boot Diagnostics) consist of the following hardware tests:

ROM Test
RAM Test
8031 Processor Test (CCU and PCU)
SBC 88/45 Board Test
EEPROM Test

NOTE

The EEPROM test takes approximately 30 seconds.

The Multibus front panel LCD will display the name of the test being executed as follows:

ROM TEST (CHECKSUM CODE: XX) PASS

(XX is the hexadecimal total of the FDIO executable code or PROM set)

Followed by:

RAM TEST	PASS

Followed by:

8031 PROCESSOR TEST	PASS

for a CCU or PCU only

Followed by:

88/45 BOARD TEST	PASS

Followed by:

EEPROM (TAKES APROX: 30 SECONDS)

Followed by:

EEPROM (TAKES APROX: 30 SECONDS) PASS

Followed by:

BOOT DIAGNOSTICS	PASS

Followed by:

FDIO INITIALIZATION VER X.X	RCU AN P

(Typical Readout)

X.X = firmware revision level

The control unit becomes inoperative if any of the Phase I hardware tests fail. The display area will indicate the particular test that failed. The control unit will remain inoperative until the defective hardware is repaired.

Phase II Diagnostics include the real-time executive program, Versatile Real-Time Executive (VRTX). These Diagnostics are automatically executed on primary control units if the Phase I Diagnostic tests pass. Secondary control units activate VRTX and enter the normal (run) mode. Secondary control units do not run Phase II Diagnostics.

Phase II Diagnostics consist of the following three hardware tests:

1. GPI and GPO loopback (CCU and PCU only),
2. ICL loopback (CCU and PCU only), and
3. Modem loopback (RCU only).

The Phase II Diagnostics are not displayed. If any of the Phase II hardware tests fail, a corresponding error message will be displayed on the front panel. The error message indicates the nature of the problem detected by the test. Refer to table 7-1 for descriptions of the error messages. The error is also recorded in the SEL and, in some cases, sent to the Host. The error message remains on the Multibus front panel display until the message acknowledge (MSG/ACK) key on the keypad is pressed. The control unit automatically enters the normal mode after the error message(s) are acknowledged.

7.2.1.2.2 Background Diagnostics. Background Diagnostics are continually executed when a control unit is in normal mode. Background Diagnostics consist of the following tests, depending on the control unit status (primary or secondary):

a. Primary control unit
   1. iSBC 88/45 board ROM
   2. iSBC 88/45 board RAM
   3. depending on control unit type as follows:
      (a) CCU/PCU: utility board RAM
      (b) RCU: expanded memory board RAM

b. Secondary control unit
   1. iSBC 88/45 board ROM
   2. iSBC 88/45 board RAM
   3. CCU/PCU utility board RAM

The execution of background Diagnostic tests is controlled by VRTX. Each test is scheduled as a low priority background task and executed while the control unit is idle (not processing messages). If a background Diagnostic test detects a problem, a corresponding error message will be displayed on the Multibus front panel. Certain error conditions will cause a control unit switch to occur automatically. Refer to table 7-1 for the list and descriptions of error messages. The error will also be recorded in the SEL and, in some cases, sent to the Host.

7.2.1.2.3 Multibus Front Panel Diagnostics. The Multibus front panel Diagnostics enable the technician to select and run specific tests (depending upon the control unit status (primary or secondary)). To enter front panel DIAG mode, press the DIAG key on the keypad. This will enable the following five DIAG tests:

1. RAM/ROM (primary or secondary) — iSBC 88/45 and utility board RAM read/write test and iSBC 88/45 board ROM checksum;
2. BC QUERY (primary) — displays BC status and peripheral status of selected device;

3. CANNED MESSAGE (primary) — sends a programmed message to the selected peripheral device which includes the following:

PCU	CCU/RCU
Device #	RCU # Device #
Red and Black Colors	Red and Black Colors
Tab Settings	Tab Settings
Printer Character Set	Printer Character Set
Sample Flight Strip	

4. DISPLAY (secondary) — displays rotating pattern to verify all display dots are functional;

5. KEYPAD (secondary) — displays the particular key pressed.

The following procedures enable front panel Diagnostic tests.

7.2.1.3 ROM/RAM Test Procedure. This test is available on primary and secondary control units. The test performs a checksum on the ROM and verifies each individual memory location in RAM.

1. Press DIAG key. The front panel will display:

ROM/RAM, BC QUERY, CANNED MSG: 1,2,3?

for primary, or

ROM/RAM, DISPLAY, KEYPAD: 1,2,3?

for secondary.

2. Press the 1 key, then the ENTER key. After a short delay, the front panel will display:

TESTING ROM, PLEASE WAIT

Followed by:

ROM PASSED, PRESS ENTER TO CONTINUE

or,

ROM FAILED, XX PRESS ENTER TO CONTINUE

XX = checksum

3. Press the ENTER key. After a short delay the front panel will display:

TESTING RAM, PLEASE WAIT

Followed by:

RAM PASSES, PRESS ENTER TO CONTINUE

or,

RAM FAILED IN: XXXX PRESS ENTER

XXXX = Hexadecimal address of failed memory location.

4. Press ENTER key to acknowledge test results and return to diagnostic menu (as shown in step 1 of this paragraph); or, press EXIT key to exit diagnostic mode and return to normal mode.

7.2.1.4 BC QUERY Test Procedure. This test is available only on primary control units. The test proves communications to BC are possible, the LAN is working properly and allows the status of the peripherals to be determined.

1. Press DIAG key. The front panel will display:

ROM/RAM, BC QUERY, CANNED MSG: 1,2,3?

2. Press the 2 key, then the ENTER key. The front panel will display:

BC QUERY: DEVICE ADDRESS?

3. Enter the device address (decimal) of the BC to be queried, then press the ENTER key. Device addresses are listed in table 2-21. After a brief delay the front panel will display:

DEV#01 (RDY) BC STAT:03 PER STAT:0C	(Typical Readout)

To determine the BC status and peripheral status for the device number displayed, perform the following using tables 7-3, 7-4, and 7-5.

a. Using table 7-3, change the BC STAT:03 and PER STAT:0C hex numbers to 8-bit binary numbers.

b. Place the BC STAT binary number (0000 0011) directly under the [(7654) (3210)] bits on the BC status table 7-4 and follow each line from each bit position to match the ones and zeros with the BC status definitions.

c. Place the PER STAT binary number (0000 1100) directly under the [(7654) (3) (210)] bits on the PER STAT table 7-5 and follow each leg to match the ones and zeros with the peripheral status definitions.

4. Press the ENTER key to acknowledge test results and return to DIAG menu (as shown in step 1 of paragraph 7.2.1.4); or, press the EXIT key to return to normal mode.

TABLE 7-3. BINARY/HEX/DECIMAL CONVERSION TABLE

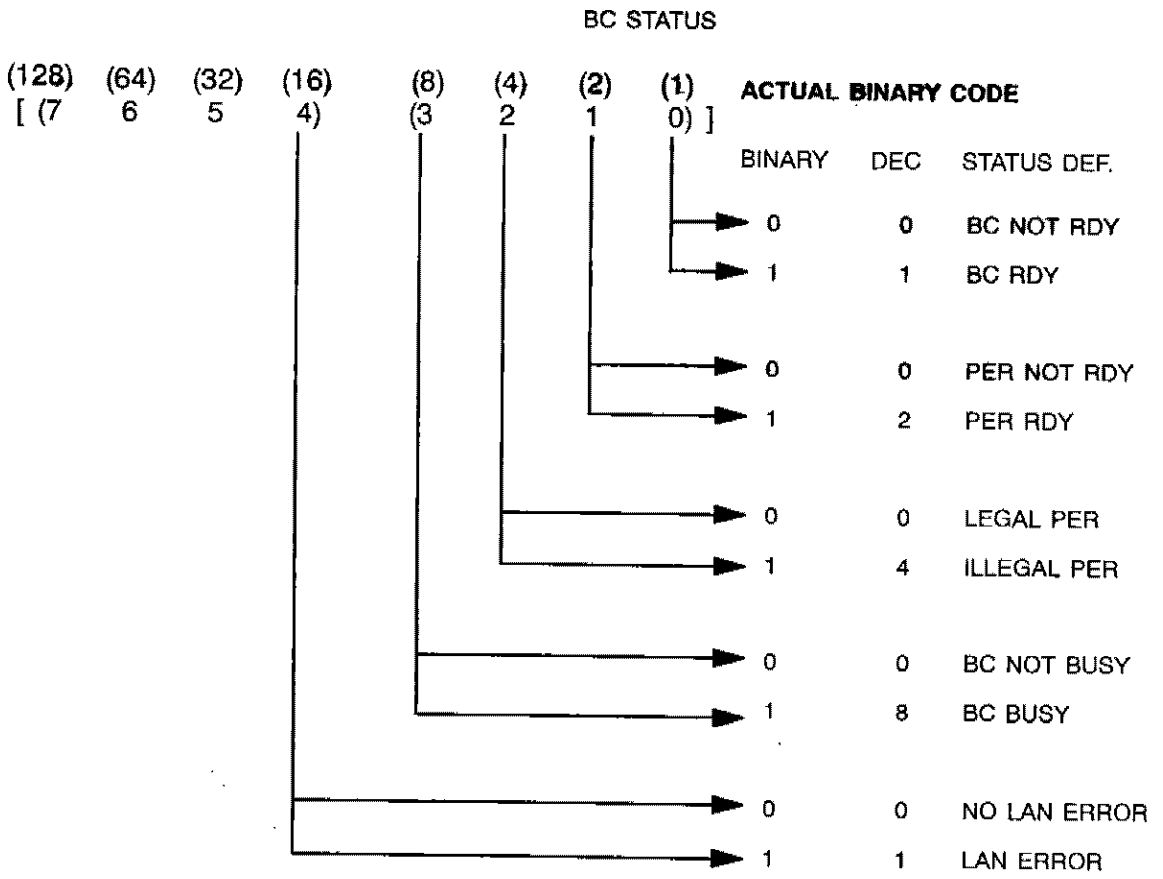
BINARY BITS 76543210	HEX	DECIMAL
00000000	00	0
00000001	01	1
00000010	02	2
00000011	03	3
00000100	04	4
00000101	05	5
00000110	06	6
00000111	07	7
00001000	08	8
00001001	09	9
00001010	0A	10
00001011	0B	11
00001100	0C	12
00001101	0D	13
00001110	0E	14
00001111	0F	15

RESULTS:

BC STAT:03 = 0000 0011

PER STAT:0C = 0000 1100

TABLE 7-4. BC STATUS CODES

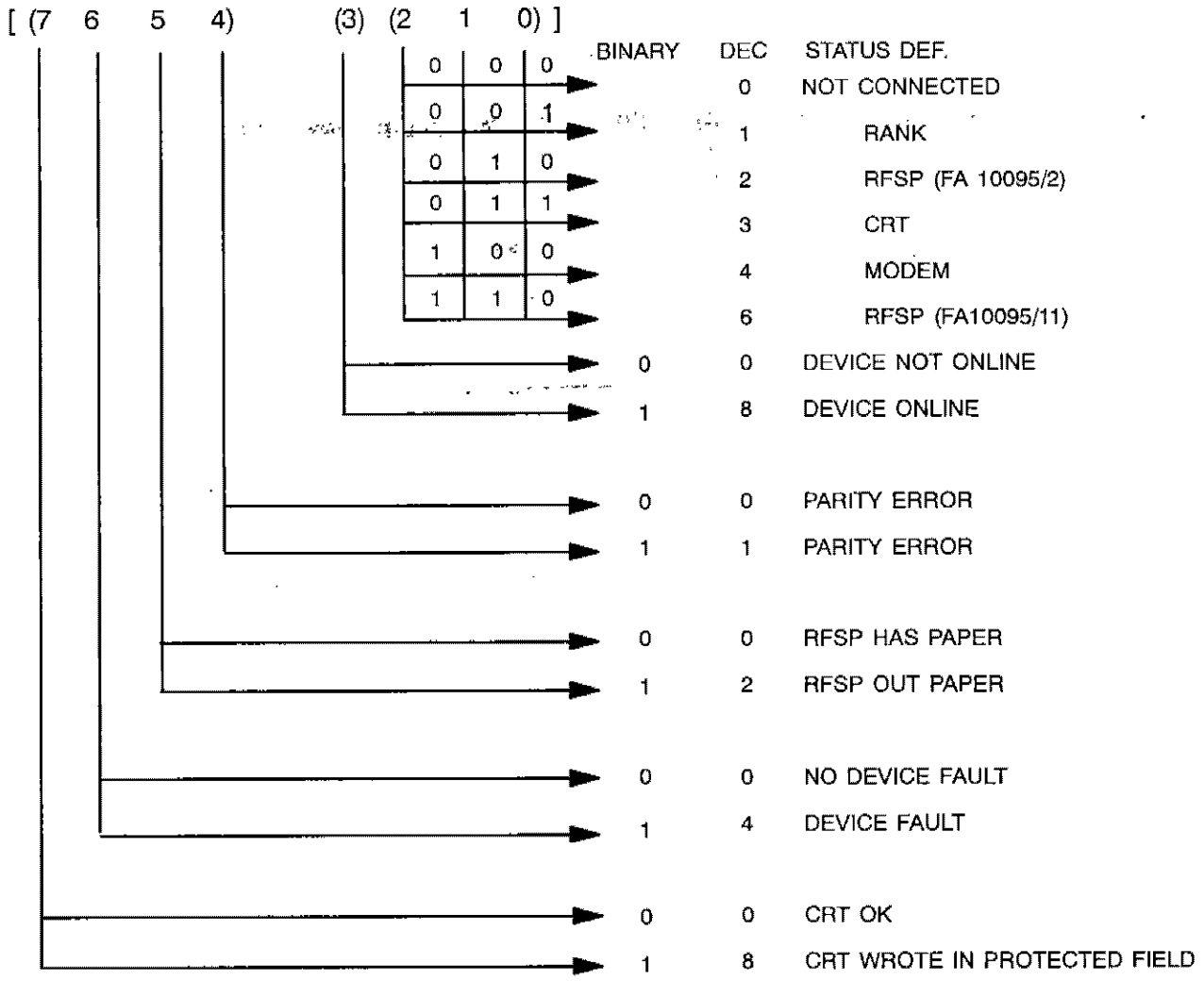


Results for this example are:

BITS	STATUS DEF.
Bit 0 = 1	BC RDY (Bus Connector ready)
Bit 1 = 1	PER RDY (Peripheral ready)
Bit 2 = 0	Legal PER (Legal Peripheral)
Bit 3 = 0	$\overline{\text{BC BUSY}}$ (Bus Connector not busy)
Bit 4 = 0	NO LAN ERROR
Bits 5-7 = 0	NOT USED

TABLE 7-5. PERIPHERAL STATUS CODES

PER STATUS



The results for this example are:

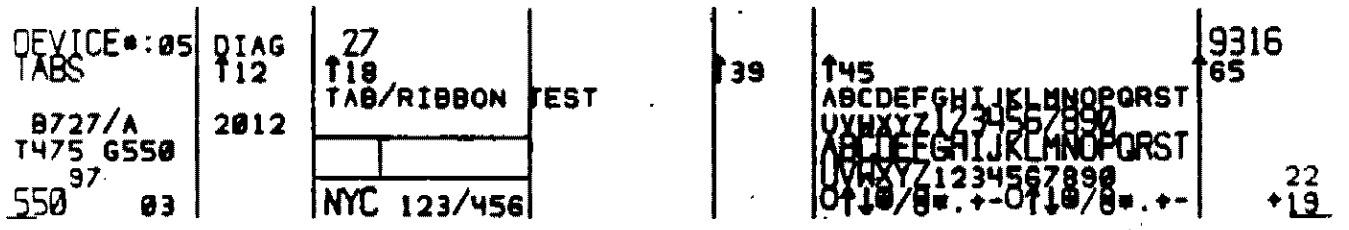
BITS	STATUS DEF.
Bit 0 = 0 Bit 1 = 0 Bit 2 = 1	MODEM (Device is a modem)
Bit 3 = 1	DEVICE ON LINE
Bit 4 = 0	$\overline{\text{PARITY ERROR}}$ (No parity error)
Bit 5 = 0	RFSP HAS PAPER
Bit 6 = 0	NO DEVICE FAULT
Bit 7 = 0	CRT OK

7.2.1.5 CANNED MESSAGE Test Procedure. The canned message test is used to prove the control units are communicating correctly with the peripheral devices and the peripheral devices have received, processed, and acknowledged the communications correctly. The test is performed at the front panel of a control unit.

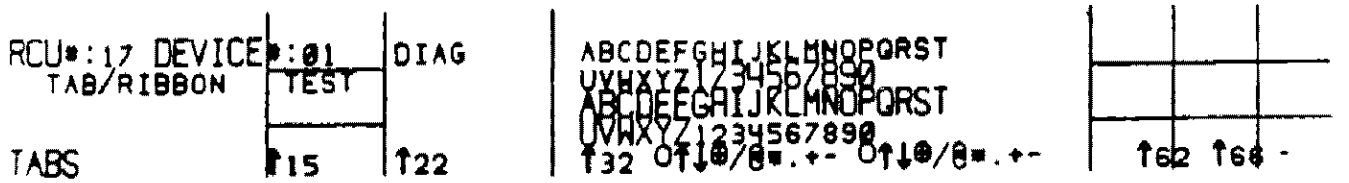
NOTE

In the configurations with redundant control units (CCU, PCU, CCU/CCU, PCU/PCU, and CCU/PCU) the test is available only when the control unit is the primary unit of the redundant pair.

An example of the canned message used for tests from PCU front panels is as follows:



An example of the canned message used for tests from CCU or RCU front panels is as follows:



Procedure Steps

1. Press DIAG key. The front panel will display:

ROM/RAM, BC QUERY, CANNED MSG: 1,2,3?

2. Press the 3 key, then the ENTER key. The front panel will display:

CANNED MSG: WHICH DEVICE #?

3. Enter the device number (1 — 28 decimal) of the peripheral to receive the canned message, then press the ENTER key. Device numbers are listed in Table 2-21, LAN Address Switch Settings.

NOTE

For CCUs, the device number of the RCU must also be specified.

The CCU front panel will display:

CANNED MSG: WHICH RCU #?

4. Enter the device number (decimal) of the RCU associated with the peripheral to receive the canned message, then press the ENTER key. The front panel will display:

NUMBER OF ITERATIONS (1 — 99) :

5. Enter the number of iterations, then press the ENTER key. The front panel will display:

TEST MESSAGE IN PROCESS, PLEASE WAIT

followed by,

MESSAGE ACK OK; PRESS ENTER TO BREAK

for each successful message sent to the selected peripheral device.

6. Once the iterations are complete, press ENTER to acknowledge test results and return to DIAGNOSTIC MENU (as shown in step 1 of paragraph 7.2.1.5); or press EXIT to return to normal mode.

7. The iterations may be stopped at any time by pressing ENTER. When ENTER is pressed the front panel will display:

DIAGNOSTICS ABORTED, PLEASE WAIT

followed by a return to the DIAGNOSTIC MENU display as shown in step 1 of this paragraph.

8. When errors occur during the iterations, the front panel will display:

BAD ACK, ERR:XX PRESS ENTER TO BREAK

for each unsuccessful message sent to the selected peripheral device.

If the bad ACK message shown in step 8 of paragraph 7.2.1.5 is displayed, note the ERROR (ERR) NUMBER (XX) and refer to paragraph 7.2 for determining the type of error and trouble-shooting information to correct the error.

7.2.1.6 Display Test Procedure. This test is available only on the secondary control unit. The test checks that the LCD is functioning properly by visually showing that all the LCD dots used for displayed readouts are available.

1. Press the DIAG key. The front panel will display:

ROM/RAM, DISPLAY, or KEYPAD: 1,2,3?

2. Press the 2 key, then the ENTER key. The front panel displays a special dot pattern which moves across the display. On the first pass the dots fill in the front panel face; on the second pass the dots are removed. Verify that all LCD dots go dark and light to verify display functions properly.

3. The display test is self terminating after about 50 seconds. The display will then return to the DIAGNOSTIC MENU (as shown in step 1 of this paragraph).

7.2.1.7 Keypad Test Procedure. This test is available only on the secondary control unit. The test verifies all front panel keys are operational by causing the key description to be displayed on the LCD when a specific key is pressed.

1. Press the DIAG key. The front panel will display:

ROM/RAM, DISPLAY, or KEYPAD: 1,2,3?

2. Press the 3 key, then the ENTER key. The front panel will display:

KEYPAD TEST: PRESS KEY WITHIN 10 SECONDS

NOTE

To avoid terminating the keypad test prior to verifying each key, press the EXIT key last. Pressing the EXIT key verifies the key operation by displaying EXIT, terminates the keypad test and returns the display to diagnostic menu shown in step 1, of this paragraph.

3. Press each key and verify each key description displayed is as follows:

KEYS	DISPLAYED DESCRIPTION
YES/GO	YES/GO KEY
NO	NO KEY
MSG ACK	ACKNOWLEDGE KEY
CLEAR	CLEAR KEY

KEYS	DISPLAYED DESCRIPTION
1	DIGIT NUMBER : 1
2	DIGIT NUMBER : 2
3	DIGIT NUMBER : 3
4	DIGIT NUMBER : 4
5	DIGIT NUMBER : 5
6	DIGIT NUMBER : 6
7	DIGIT NUMBER : 7
8	DIGIT NUMBER : 8
9	DIGIT NUMBER : 9
0	DIGIT NUMBER : 0
RECN	RECONFIGURATION KEY
DIAG	DIAGNOSTIC KEY
PRI SEC	PRIMARY/SECONDARY KEY
SYS STAT	SYSTEM ERROR LOGGER KEY
EXIT	EXIT KEY

After each key, except for EXIT, is verified, the following display returns:

KEYPAD TEST: PRESS KEY WITHIN 10 SECONDS

4. The keypad test is self-terminating if a key is not pressed within a 10-second time period or is terminated by pressing the EXIT key. The following message is displayed upon termination:

DIAGNOSTICS TERMINATED

7.2.1.8 Modified Keypad Test Procedure for the RCU. Since the control units configured as RCUs do not require a redundant unit and the keypad test is programmed to run on the redundant or secondary unit, the following modified keypad test procedure is used to test the keys on the RCU front panel.

NOTE

Prior to performing this procedure, check to see the system is configured correctly. An RCU needs at least one RANK paired with one CRT or printer to be configured correctly.

1. Press the DIAG key. The front panel will display:

ROM/RAM, BC QUERY, CANNED MSG: 1,2,3?

2. Press each numerical key separately. The key description will be displayed in the second to last space of the display as follows:

ROM/RAM, BC QUERY, CANNED MSG: 1,2,3? 1

(Typical Readout)

After the numerical key is displayed, press the CLEAR key to remove the selection from the display.

3. Press the YES/GO key. Observe that the word, GO, appears in the last three spaces of the display. Press CLEAR to remove the selection from the display.

4. Press the NO key. Observe the word, NO, appears in the last three spaces of the display. Press CLEAR to remove the selection from the display.

5. Press the EXIT key. The front panel will display:

RCU AN P

6. Press the RECN key. The front panel will display:

Standard:

RANK PAIR=1 ERR LOG=2 CRT PAIR=3 TAB=4:

Oceanic:

RANK PAIR=1 ERR LOG=2 FF TIMEOUT=3:

Press the EXIT key and the front panel will return to the display shown in step 5 of paragraph 7.2.1.8.

7. Press the PRI/SEC key. The front panel will display:

42 SWITCH NOT ALLOWED

Press the MSG ACK key. The front panel will return to the display shown in step 5 of paragraph 7.2.1.8.

8. Press the SYS STAT key. The front panel will display:

SYSTEM MENU = 1	DEVICE MENU = 2:

9. Press the **1** key followed by pressing the ENTER key. The front panel will display:

SYS HIST=1 SEC STAT=2 CLR=3 ME=4:

Press the EXIT key. The front panel will return to the display shown in step 5 of this paragraph. This completes the modified keypad test for the RCU.

7.2.2 Isolating Power Problems

Power problems typically cause a control unit or peripheral to become completely inoperative. Figure 7-1 isolates power related faults in the control unit.

Power problems are most often caused by one of the following conditions:

a. Site, ac power distribution, or power supply assembly circuit breakers either defective or set to OFF;

NOTE

The power supply assembly circuit breakers switch 115 V ac to the power supply input(s). Each circuit breaker illuminates an internal lamp when its power supply output is nominal.

b. The ac and dc power cables disconnected or defective;

c. Circuit board not properly seated in backplane connector, or circuit board or backplane is defective.

NOTE

Each BC board contains two on board fuses. Each fuse is in series with a 5 V BC power supply.

d. Power supply output below nominal (out of adjustment, see section 6.3 for power supply adjustment instructions) or defective;

e. The ac power distribution assembly not connected or defective.

Peripheral power problems are discussed in the vendor's service/technical manual.

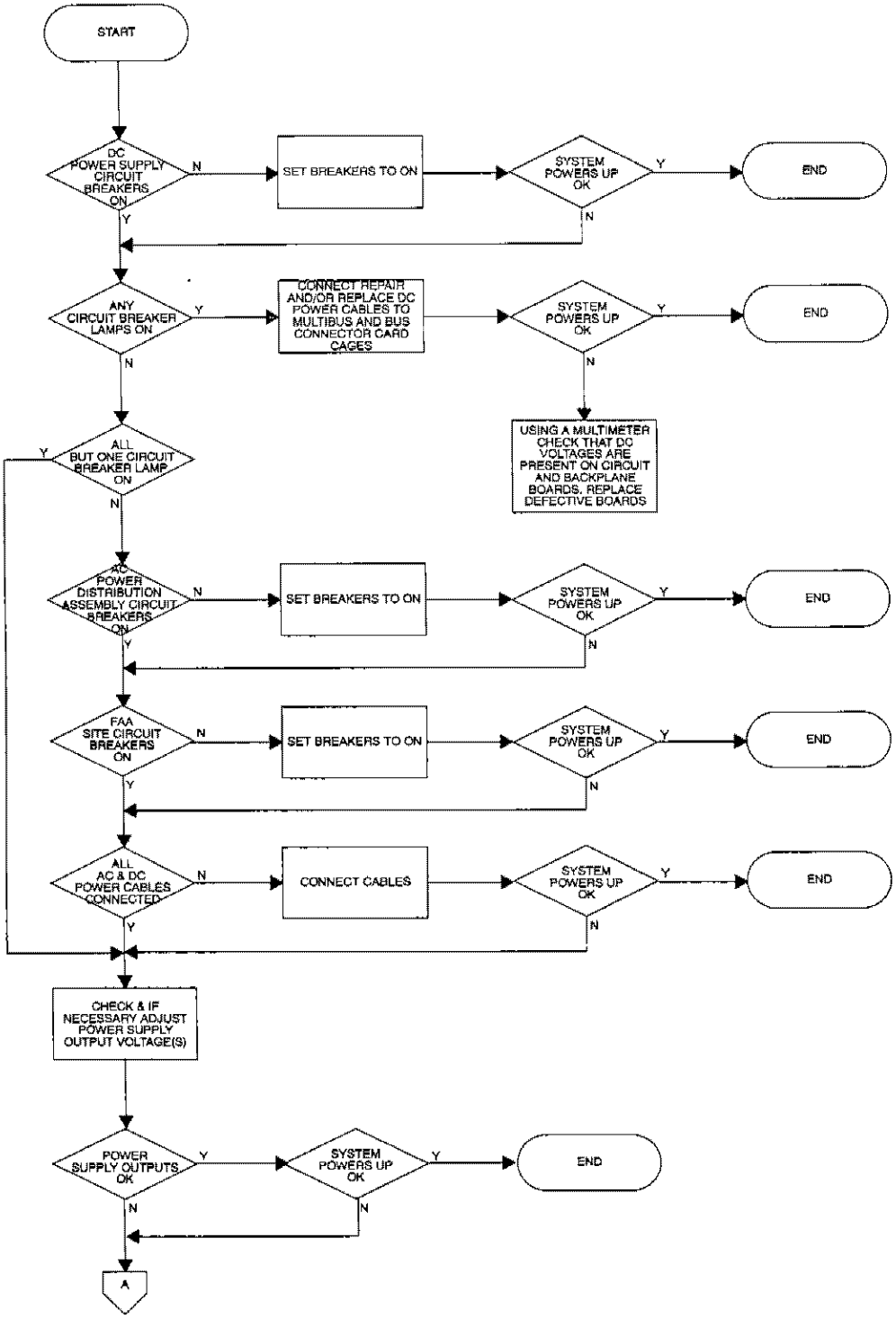


FIGURE 7-1. ISOLATING POWER PROBLEMS (SHEET 1)

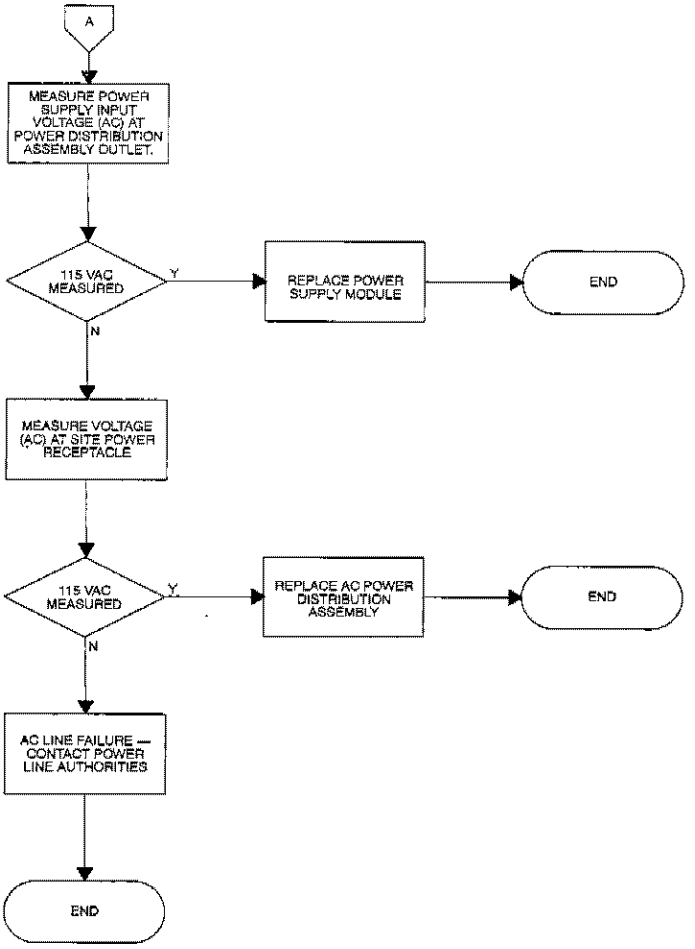


FIGURE 7-1. ISOLATING POWER PROBLEMS (SHEET 2 — END)

7.2.3 Isolating Peripheral Problems

The front panel Diagnostics (BC Query and Canned Message; see paragraph 7.2.1.2.3) and the applicable flowchart shown in figures 7-2 through 7-5 are used in identifying a RFSP, CRT, or RANK failure or verifying correct operation. In addition, the RFSP features built-in self test and Diagnostics.

NOTE

A defective BC board can cause abnormal peripheral operation.

7.2.4 Isolating TELCO Problems

The front panel diagnostics (see paragraph 7.2.1.2.3) are used to perform BC Query Test from the CCU to one of the RCUs peripherals that has a suspected bad modem. The results BC STAT 01,PER STAT 04 indicate a problem existing in the TELCO or modem link. Contact the local FAA representative for repair.

7.2.5 Isolating Host Problems

The front panel diagnostics (see paragraph 7.2.1.2.3) are used to perform canned message procedures from the CCU and PCU to any respective peripherals. This verifies correct operation from the control unit to the peripheral. Verify the Host GPI/GPO cable to the PAMRI adapters using a Multimeter. If these tests have no failures, contact the local FAA representative for repair.

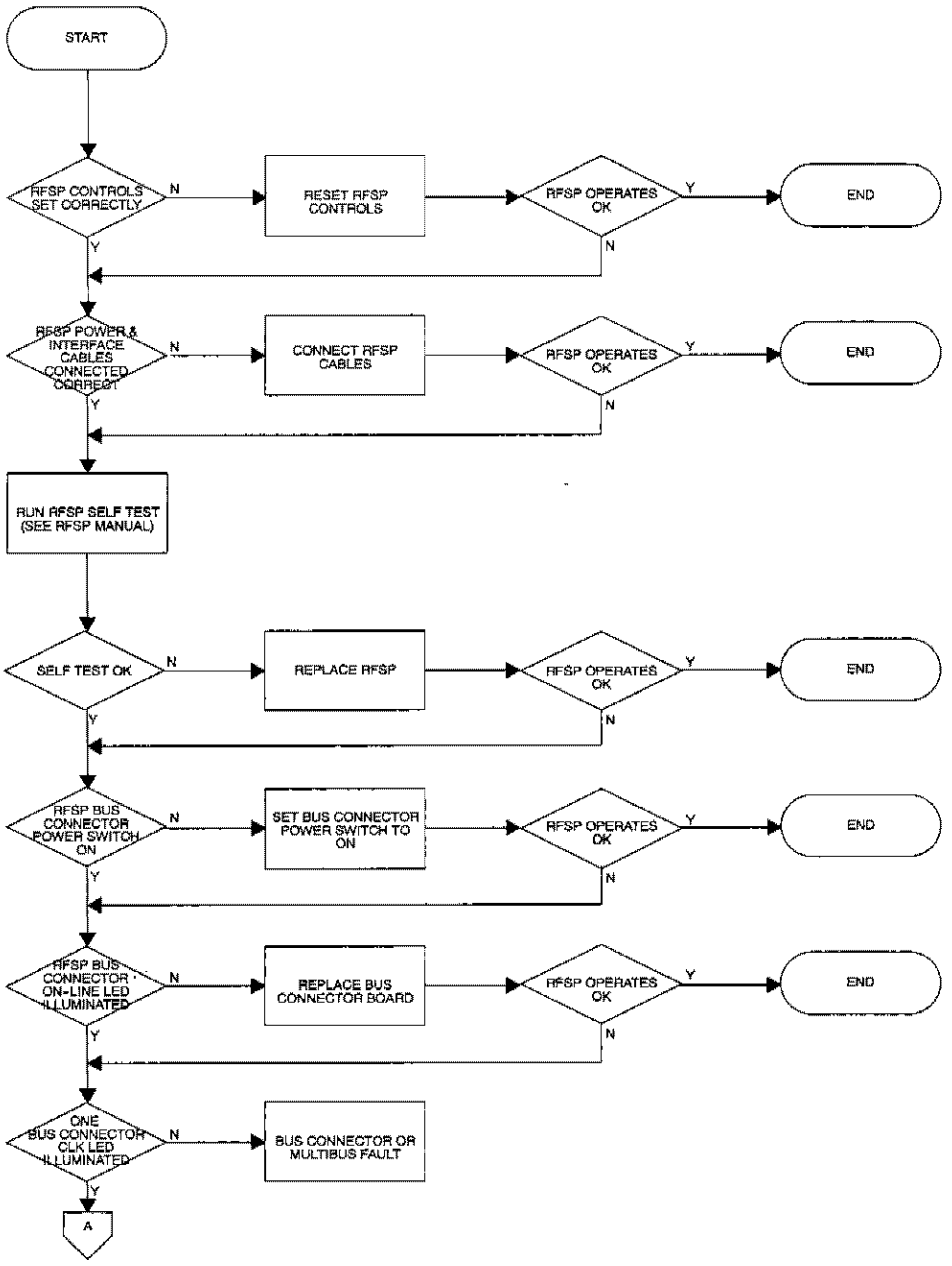


FIGURE 7-2. RFSP FAULT ISOLATION (SHEET 1)

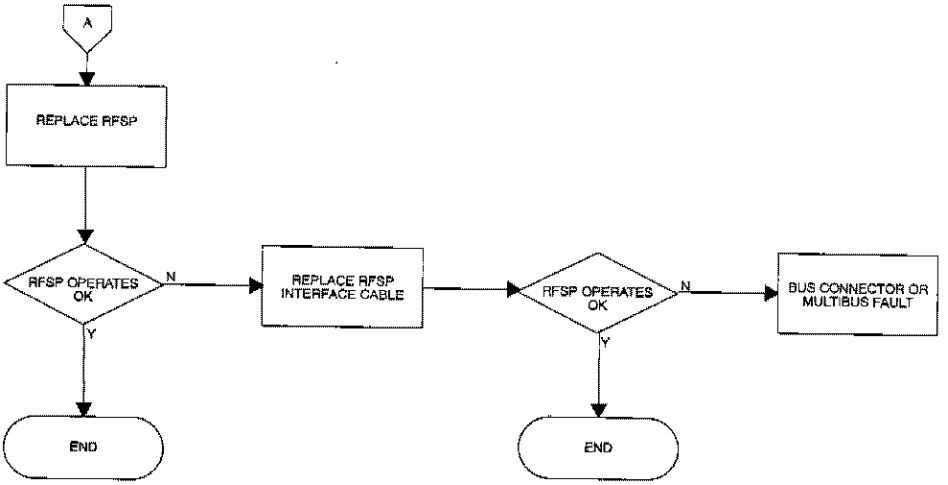


FIGURE 7-2. RFSP FAULT ISOLATION (SHEET 2 —END)

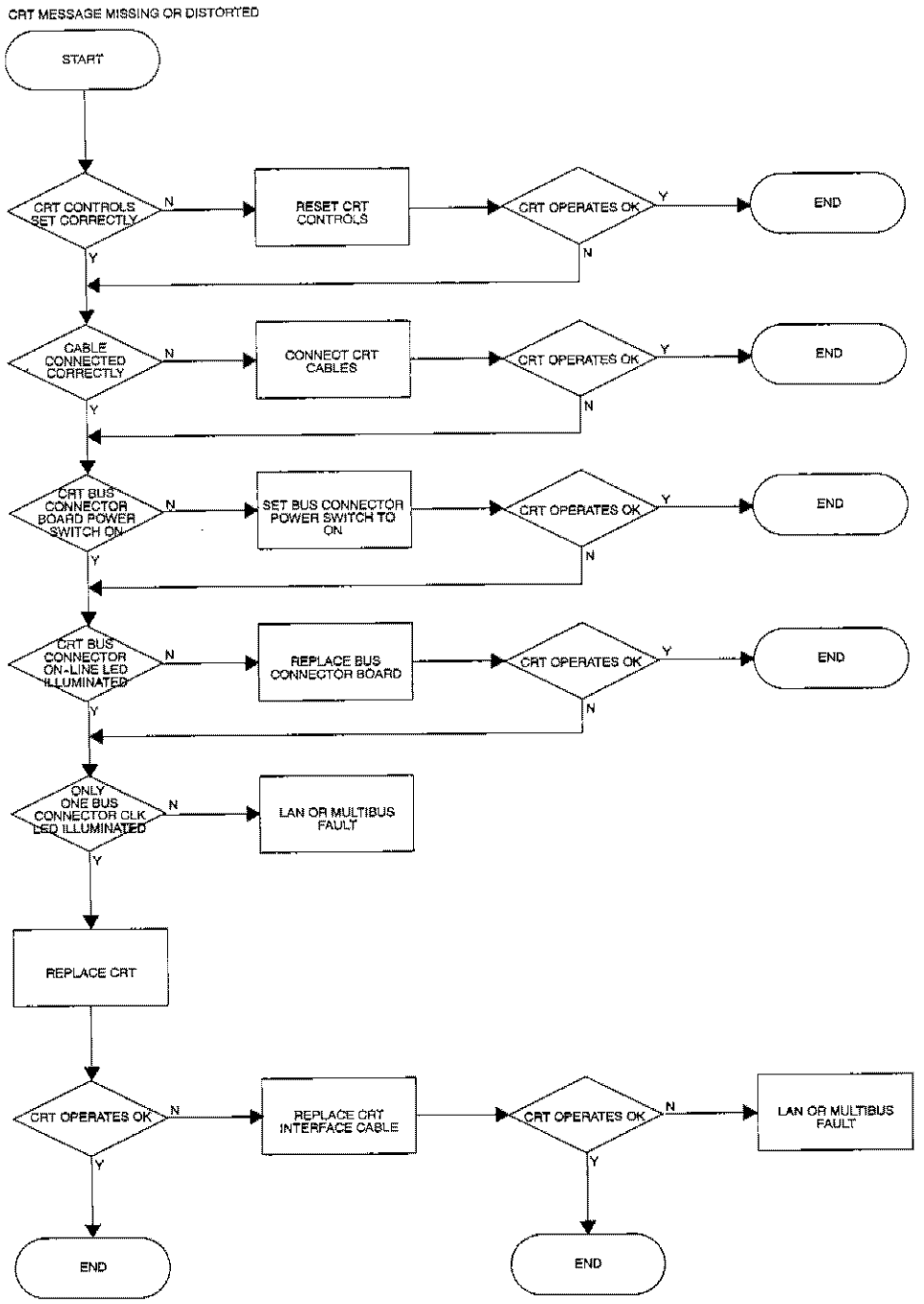


FIGURE 7-3. CRT FAULT ISOLATION

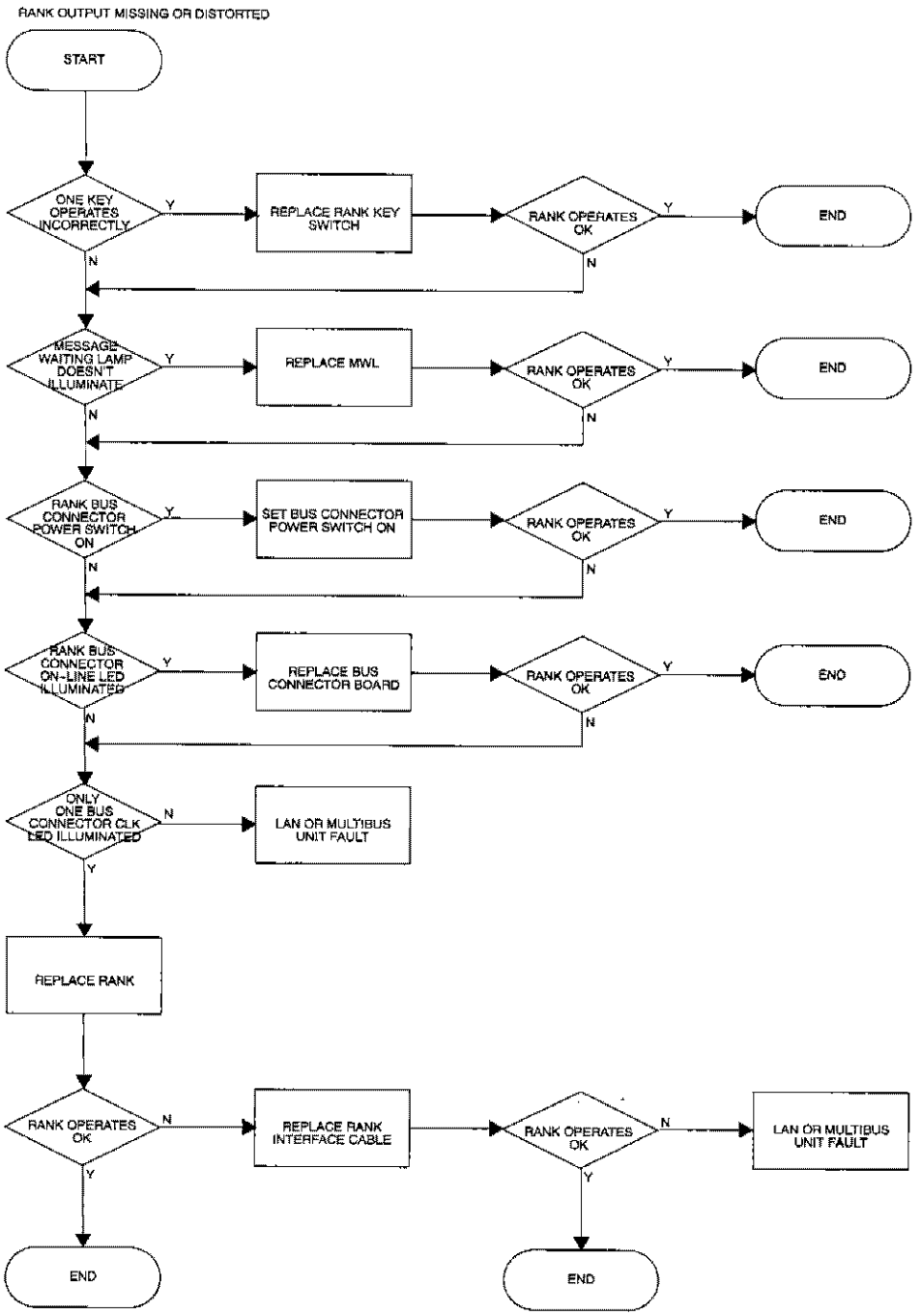


FIGURE 7-4. RANK FAULT ISOLATION

7.2.6 Status Indicators

As shown in figures 7-5 and 7-6, both the BC board and BC backplane contain LED status indicators which show BC power supply status and clock activity.

7.2.7 System Error Logger (SEL) Operational Procedure

The SEL was designed to assist the technician in the Diagnostics and repair of a control unit. The following data is assumed understood before the SEL is used:

a. Any menu will allow the EXIT button to force the front panel to leave SEL and return to main mode (the display will either be clear or displaying a warning message.)

b. With the exception of the EXIT button, all entries must be followed by ENTER to be processed. This will give the technician a chance to recover and clear the entry before processing.

c. In all submenus, the menu option will cause the front panel to return to the previous menu.

d. The maximum number of errors stored for any device is 64. New errors will begin to overwrite the oldest.

e. There are separate error storage areas. Device 0 will be designated for system errors. The remainder of the storage areas will be device errors, relative to the control unit in which the error is stored. As an example, PCU device 5 will be a printer, while that same device in a CCU will be an RCU control unit. The CCU treats an RCU as a peripheral device, without regard to the RCU having its own peripheral devices.

The following procedures describe how to assign and use the SEL option (Sys Stat Key on the front panel display). See figure 7-7 for SEL overview.

7.2.7.1 SEL Procedure to Assign Error Logger. The error logger assignment is made from the PCU and RCU Multibus front panel assemblies. The front panel must be in main mode to make the assignment. The procedure to assign the error logger device from either a PCU or an RCU is as follows (changes in procedure from one device to another are noted):

1. Press RECN at the front panel (secondary at the PCU may be used). The PCU display will read:

CNTRL ID=1 ERR LOG=2 PRIM/SEC=3:

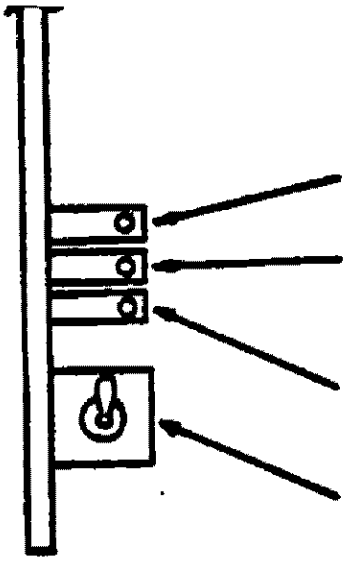
The RCU display will read:

RANK PAIR=1 ERR LOG=2 CRT PAIR=3 TAB=4:

NOTE

The RANK pairing procedure is explained in section 3.0.

BUS CONNECTOR BOARD (VIEW FROM FRONT OF CARD CAGE)



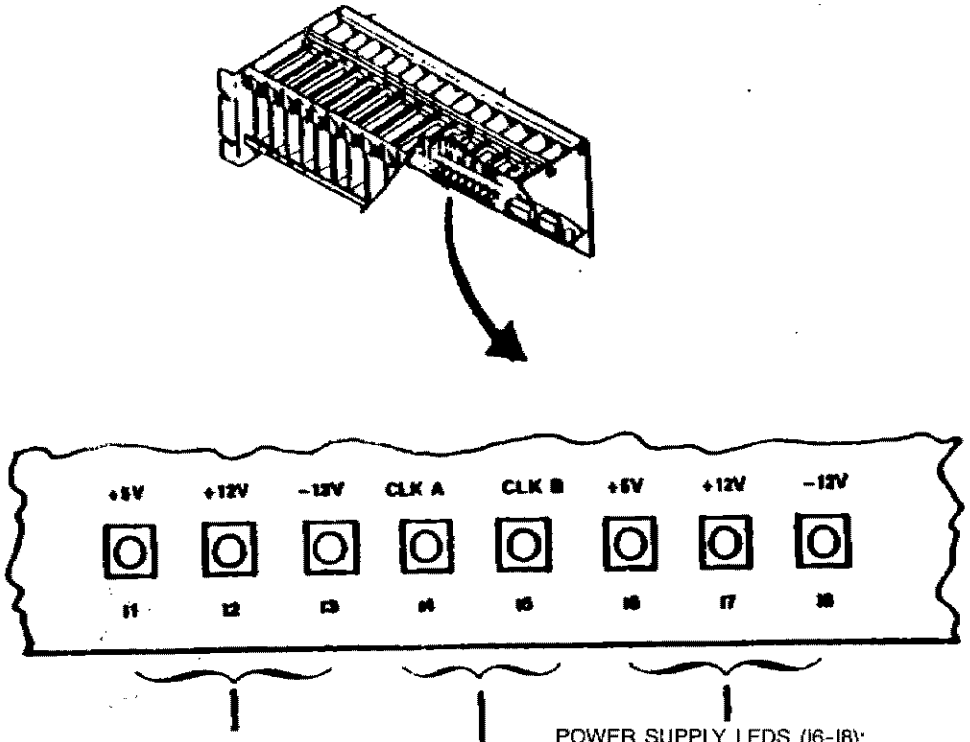
LAN A (I8): ILLUMINATES TO INDICATE THE BUS CONNECTOR BOARD IS COMMUNICATING ON LAN A.

LAN B (I2): ILLUMINATES TO INDICATE THE BUS CONNECTOR BOARD IS COMMUNICATING ON LAN B. (I2 IS NOT FUNCTIONAL ON RCU CABINETS) NOTE: IF I2 & I3 ARE BOTH ILLUMINATED, A FAULT IS INDICATED.

ON-LINE (I1): ILLUMINATES TO INDICATE THE BUS CONNECTOR BOARD IS ON-LINE. I1 EXTINGUISHES TO INDICATE THE BUS CONNECTOR BOARD IS BYPASSED.

POWER SWITCH: WHEN TOGGLE IS UP (ON), +5 V IS CONNECTED. WHEN TOGGLE SWITCH IS DOWN (OFF), +5 V IS DISCONNECTED.

FIGURE 7-5. BC BOARD STATUS INDICATORS



POWER SUPPLY LEDS (I1-I3):
EACH LED ILLUMINATES TO INDICATE THE RESPECTIVE POWER SUPPLY MODULE OUTPUT VOLTAGE IS NOMINAL. THESE THREE LEDS ARE ASSOCIATED WITH THE POWER SUPPLY MODULE(S) CONNECTED TO BACKPLANE CONNECTOR P22.
NOTE: +12 V & -12 V LEDS ARE NOT FUNCTIONAL ON PCU CABINETS.

POWER SUPPLY LEDS (I6-I8):
EACH LED ILLUMINATES TO INDICATE THE RESPECTIVE POWER SUPPLY MODULE OUTPUT VOLTAGE IS NOMINAL. THESE THREE LEDS ARE ASSOCIATED WITH THE POWER SUPPLY MODULE(S) CONNECTED TO BACKPLANE CONNECTOR P22. NOTE: I6-I8 ARE NOT FUNCTIONAL ON RCU CABINETS.

LAN CLOCK LEDS I4 & I5:
I4 ILLUMINATES TO INDICATE LAN CLOCK A IS ACTIVE.
I5 ILLUMINATES TO INDICATE LAN CLOCK A IS ACTIVE.
DURING NORMAL OPERATION, ONLY ONE LED ILLUMINATES (E.G., IF XCU A IS PRIMARY, CLK A INDICATOR ILLUMINATES).
NOTE: IF BOTH CLK A AND CLK B ARE ILLUMINATED, A FAULT IS INDICATED.
NOTE: CLK B LED IS NOT FUNCTIONAL ON RCU CABINETS.

FIGURE 7-6. BC BACKPLANE STATUS INDICATORS

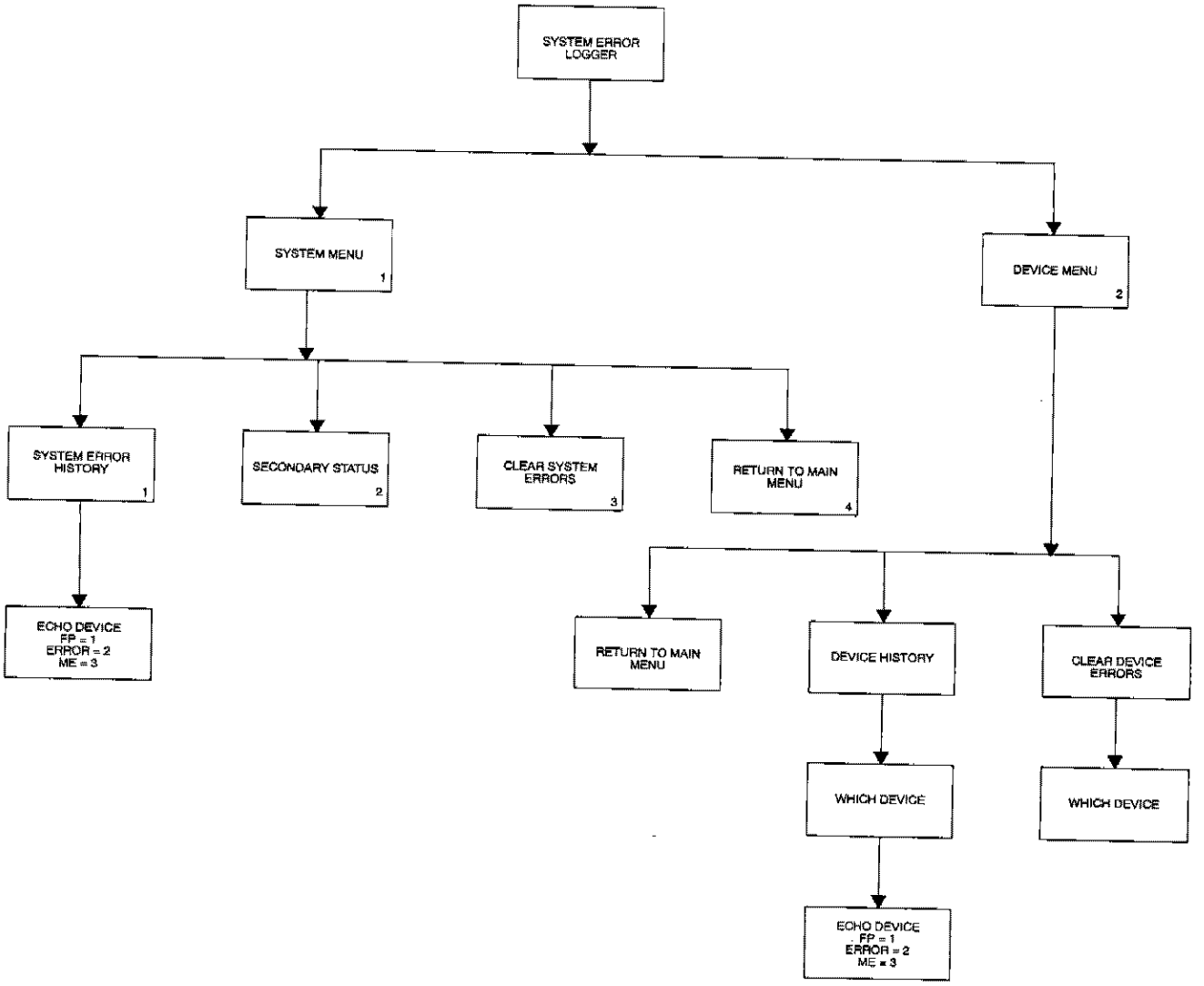


FIGURE 7-7. SEL OVERVIEW

2. Press **2** and ENTER.

   The display at a PCU will read:

ERR DEV1: 00	NEW? 30=MENU:

   The display at an RCU will read:

ERR DEV1: 00	NEW? 16=MENU:

3. The assigned error logger value is displayed. If a new value is to be assigned, enter the peripheral number and press ENTER. If, for example, the new device number entered was a **3** from the front panel, it will appear as shown:

   The display at an RCU will read:

ERR DEV1: 03	NEW? 16=MENU:

   The display at a PCU will read:

ERR DEV1: 03	NEW? 30=MENU:

4. To exit back to the main menu, press EXIT on the keypad.

NOTE

Error logger assignments must correspond to the BC assignments. Valid assignments for the PCU are 1 through 28 and the maintenance channel (29). Valid assignments for the RCU are 1 through 10.

7.2.7.2 SEL Procedure for Accessing System Status. To enter SEL press the SYS STAT key on the front panel keypad. The following menu will appear:

SYSTEM MENU = 1	DEVICE MENU = 2:

At this point the technician has the option of exploring system type (paragraph 7.2.7.2.1) or device (paragraph 7.2.7.2.2) oriented errors. Enter the appropriate option number.

7.2.7.2.1 System Menu. When the system option is chosen, the following menu will appear:

SYS HIST=1	SEC STAT=2	CLR=3	ME=4:

If **2** is pressed at the RCU, the following menu will appear:

NO SECONDARY IN RCU,	PRESS ENTER

Press ENTER to get back to the system menu. Descriptions of each option on the system menu are as follows:

OPTION	PROCEDURE	DESCRIPTION
SYS HIST	7.2.7.2.1.1	Used to display system related errors on the front panel or error logger.
SEC STAT	7.2.7.2.1.2	Used to find out the present state of a secondary in a PCU or CCU.
CLR	7.2.7.2.1.3	Used to erase all system errors presently stored.
ME	—	Used to return SEL to the previous menu.

Enter the appropriate menu option and refer to the appropriate paragraphs.

7.2.7.2.1.1 System History. The system history option is used to display online system related errors (table 7-1) on the front panel display or error logger.

NOTE

The errors encountered during front panel diagnostics are not entered into the error logger. Those errors are normally encountered during a troubleshooting mode and not considered online system related errors.

When this option is chosen, the following menu will be displayed:

```
ECHO DEVICE:    FP=1    ERR LOG=2    3=ME:
```

This menu gives the technician the option of displaying the online system errors on the front panel or having them printed on the error logger or returning to the system menu.

7.2.7.2.1.1.1 Front Panel as Error Echo Device. To display the system errors on the front panel, enter option number 1. The front panel will either display the most recent system error, or the following message:

```
NO ERR(S) LOGGED,          PRESS ENTER
```

No errors have been logged at this time. Press ENTER to return to the system menu.

If system error messages are logged, press ENTER until all logged error messages have been displayed.

NOTE

The system error log can be interrupted at any time by pressing the NO key.

The front panel display will return to the system menu.

After cycling through the errors in the error logger, the last message before the system menu is displayed will read:

END OF ERROR LOG, PRESS ENTER

To return to the system menu, press ENTER.

If a problem exists with the error logger, the following message will be displayed:

ERR LOG NOT RESPONDING CONT? (Y/N):

Enter YES/GO to try and continue to print the error log. Enter NO to return to the system menu.

7.2.7.2.1.1.2 Error Logger as an Echo Device. To print the system errors enter option number 2. One of the following messages will appear:

PRINTING LOG, PLEASE WAIT...:

This message will appear when the system errors are being printed. This is the normal response.

END OF ERROR LOG, PRESS ENTER

This message will appear when system errors have all been correctly printed. Pressing ENTER returns the display to the system menu.

NO ERROR LOGGER, PRESS ENTER

This message will appear if the error logger is not defined or cannot be accessed. Pressing ENTER returns the display to the system menu.

ERR LOG NOT RESPONDING CONT? (Y/N):

This message will appear if something has gone wrong with the printing of the error log. Pressing YES/GO allows the logger to try and continue printing the error log. Pressing NO returns the display to the system menu.

NO ERRORS LOGGED

This message will appear when no errors have been logged since the errors have last been cleared. Pressing ENTER returns the display to the system menu.

7.2.7.2.1.2 Secondary Status. The secondary status option (number 2 on the system menu) is used to display the present state of a secondary unit in a PCU or CCU. When this option is chosen on a primary control unit, the displayed state of operation is of the secondary unit paired with the primary unit.

When this option is chosen at a secondary control unit, the unit is displaying the state of operation of itself. If the secondary state option is chosen, one of the following three messages will appear on the front panel display:

```
SECONDARY IS OK,          PRESS ENTER
```

This message will appear when the secondary has no errors. Press ENTER to return to the system menu.

```
FSE FAILURE               code: XX
```

This message will appear when FSE has failed.

The fault codes (code: XX) associated with this fault display are:

CODE	DESCRIPTION
11	Internal FSE failure (FSE firmware has failed)
13	Primary and secondary control units not in sync and internal FSE failure
FF	ICL Failure

Press ENTER to return to the system menu.

```
CONTROL UNIT FAILURE      code: XX
```

This message will appear when a control unit has failed.

The fault codes (code: XX) associated with this fault display are:

CODE	DESCRIPTION
00	All circuits of control unit are inoperative
10	8031 Processor failure
12	Primary and secondary control units not in sync (primary and secondary not talking to each other)

Press ENTER to return to the system menu.

7.2.7.2.1.3 Clearing the System History. Option number 3 of the system menu will clear all stored system errors. With this option, the following message will appear on the front panel display:

```
CLEARING SYSTEM ERROR HISTORY
```

When the process is completed, the system menu will be displayed.

7.2.7.2.2 Device Menu. When the device option is chosen, the following menu will be displayed:

```
DEV HIST=1        CLR HIST=2        MENU=3 :
```

Descriptions of each option on the device menu are as follows:

OPTION	PROCEDURE	DESCRIPTION
DEV HISTORY	7.2.7.2.2.1	Used to display device related errors on the front panel or error logger.
CLR HISTORY	7.2.7.2.2.2	Used to erase device errors presently stored.
MENU	—	Used to return SEL to the previous menu.

Enter the desired menu option and refer to the proper paragraph for the procedure.

7.2.7.2.2.1 Device History. The device history option is used to display device related errors on the front panel display or error logger. When this option is chosen the following message will be displayed:

```
WHICH DEVICE ?                    :
```

Enter the device number. Note that the RCU has 21 devices, the CCU has 28 RCU devices, and the PCU has 29 devices. The next menu in sequence will request the output device. The display will read:

```
ECHO DEVICE: FP=1 ERR LOG=2 3=ME:
```

This menu provides the option of displaying the device errors on the front panel or having them printed on the error logger.

7.2.7.2.2.1.1 Front Panel as Error Echo Device. Option number 1 will display the device errors on the front panel. At this time the front panel will display either the most recent device error on the front panel or the following message:

```
NO ERR(S) LOGGED,          PRESS ENTER
```

Press ENTER to return to the device menu. No errors have been logged at this time.

When error messages exist, press ENTER until all logged error messages have been displayed.

NOTE

The device error log can be interrupted at any time by pressing the NO key.

After cycling through the errors in the error logger, the last message before the device menu is displayed will read:

```
END OF ERROR LOG,        PRESS ENTER
```

Press ENTER and the device menu will be displayed.

If the displaying of the error log has a problem, the following message will appear:

```
ERR LOG NOT RESPONDING   CONT? (Y/N):
```

This message will appear if something has gone wrong with the printing of the error log. Enter YES/GO to continue trying to print the error log. Enter NO to return to the device menu.

7.2.7.2.2.1.2 Error Logger as an Echo Device. To print the device errors on the error logger enter option number 2. One of the following messages will appear:

```
PRINTING LOG,            PLEASE WAIT...:
```

This message will appear when the device errors are being printed. This is the normal response.

```
END OF ERROR LOG,        PRESS ENTER
```

This message will appear when the device errors have all been printed correctly. Pressing ENTER returns the display to the device menu.

```
NO ERROR LOGGER,         PRESS ENTER
```

This message will appear if the error logger is not defined or cannot be accessed.

```
ERR LOG NOT RESPONDING   CONT? (Y/N):
```

Pressing YES/GO allows the logger to try printing the error log. Pressing NO returns the display to the device menu.

7.2.7.2.2.2 Clearing the Device History. Option number 2 of the device menu will clear all errors associated with a particular device. When this option is chosen, the following message will appear on the front panel display:

```
WHICH DEVICE ?                    :
```

Enter the device number.

The next message to be displayed will request the output device:

CLEARING DEVICE ERROR HISTORY

When the process is completed, the device menu will be displayed.

7.3 TOOLS AND TEST EQUIPMENT

The following five tools are required to perform corrective maintenance described in this section:

1. Screwdriver, slotted 1/4-inch;
2. Screwdriver, Phillips-head number 6;
3. Nut drivers, 3/8-inch, 7/16-inch, 1/2-inch;
4. End wrenches (box or open-ended), 3/8, 7/16, 1/2-inch;
5. Digital multimeter, 1 percent accurate.

No special tools or test equipment are required for field maintenance procedures.

7.4 REMOVAL AND REPLACEMENT PROCEDURES

Paragraphs 7.4.1 and 7.4.26.1 provide instructions to remove and replace FDIO system assemblies, subassemblies, circuit boards, modules, and peripherals.

7.4.1 AC Power Distribution Assembly

Use paragraphs 7.4.1.1 and 7.4.1.2 and figure 7-8 to remove and replace the ac power distribution assembly.

7.4.1.1 Removal

1. Open rear door of CCU or PCU cabinet (front door of RCU cabinet).
2. Set both circuit breakers (1) and (2) on the ac power distribution assembly to OFF.
3. Remove the ac line cord (7) from main power receptacle (5). (Push in, rotate left, and remove power cord plug.)

CAUTION

To maintain separate system and redundant system integrity the technician must keep ac power plugs attached to the same ac power distribution assembly location on all cabinets with two ac power distribution assemblies (all CCU and PCU configured cabinets).

4. Remove all power plugs from the ac power distribution assembly outlets, (3) and (4).
5. Remove the four Phillips-head screws (6) which secure the ac power distribution assembly to the cabinet mounting rails.
6. Carefully remove the ac power distribution assembly from the cabinet.

7.4.1.2 Replacement. Replacement is the reverse of the removal procedures.

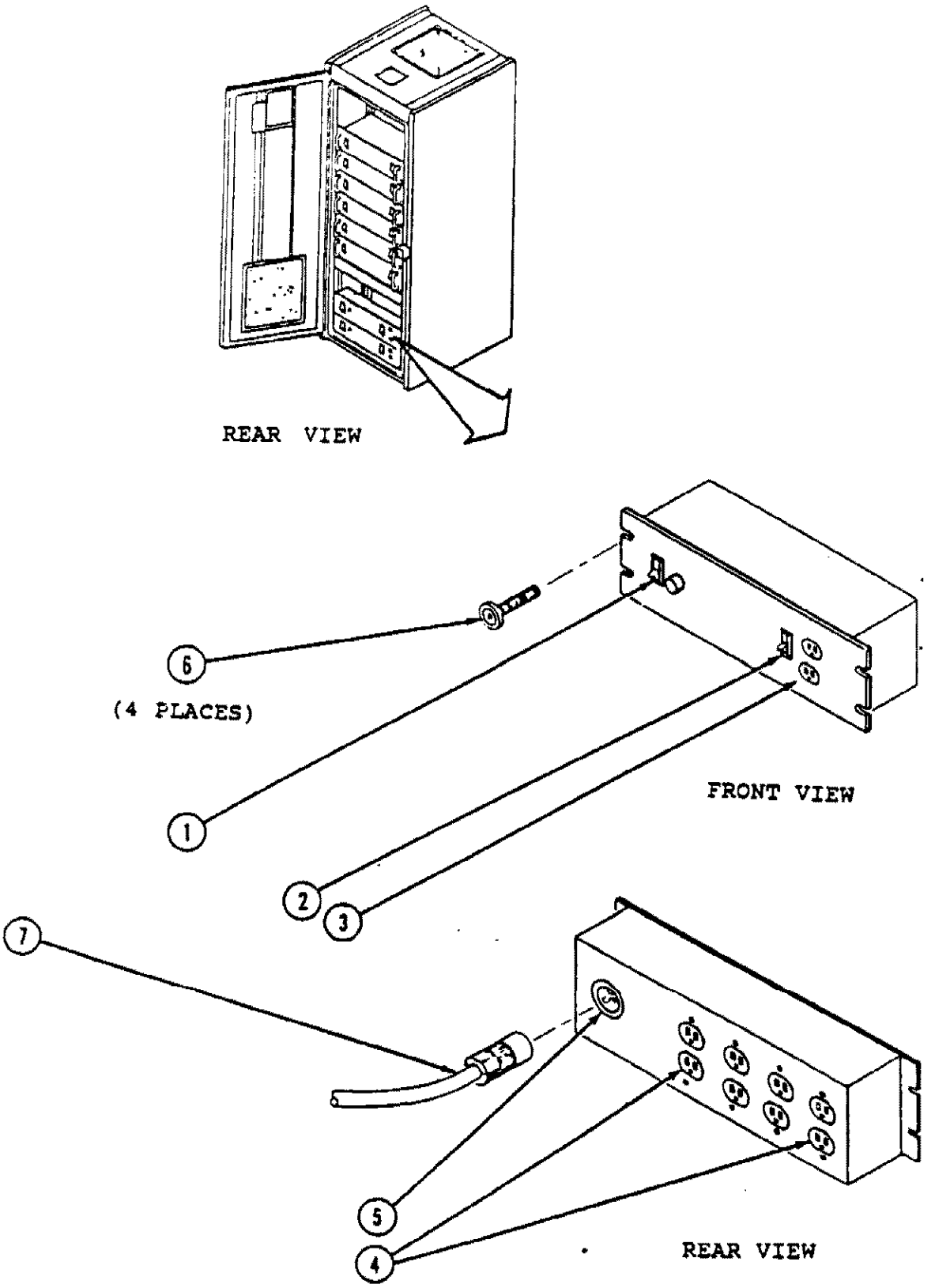


FIGURE 7-8. AC POWER DISTRIBUTION ASSEMBLY REMOVAL AND REPLACEMENT

7.4.2 Power Supply Assembly

Use paragraphs 7.4.2.1 and 7.4.2.2 along with figure 7-9 to remove and replace a power supply assembly.

7.4.2.1 Removal

1. Open rear door of CCU or PCU cabinet (front door of RCU cabinet).
2. Set power supply circuit breaker(s) (1) and (2) to OFF.

CAUTION

To maintain separate system and redundant system integrity the technician must keep ac power plugs attached to the same ac power plugs attached to the same ac power distribution assembly location on all cabinets with two ac power distribution assemblies.

3. Disconnect the power supply assembly ac power cable(s) (3) from the ac power distribution assembly outlet(s) (figure 7-8 (4)).
4. Remove the four Phillips-head screws (4) which secure the power supply assembly to the cabinet mounting rails.
5. Carefully slide the power supply assembly out of the cabinet to the full extent of the mounting rails (5).
6. Support the power supply assembly and remove the six-slotted hex-head screws (6) (three on each side of assembly).
7. Carefully lift the power supply assembly clear of the mounting rails and place on a properly supported work surface.

7.4.2.2 Replacement. Replacement is the reverse of the removal procedures.

CAUTION

Reconnect ac power cable(s) to same ac power distribution assembly the cables were disconnected from.

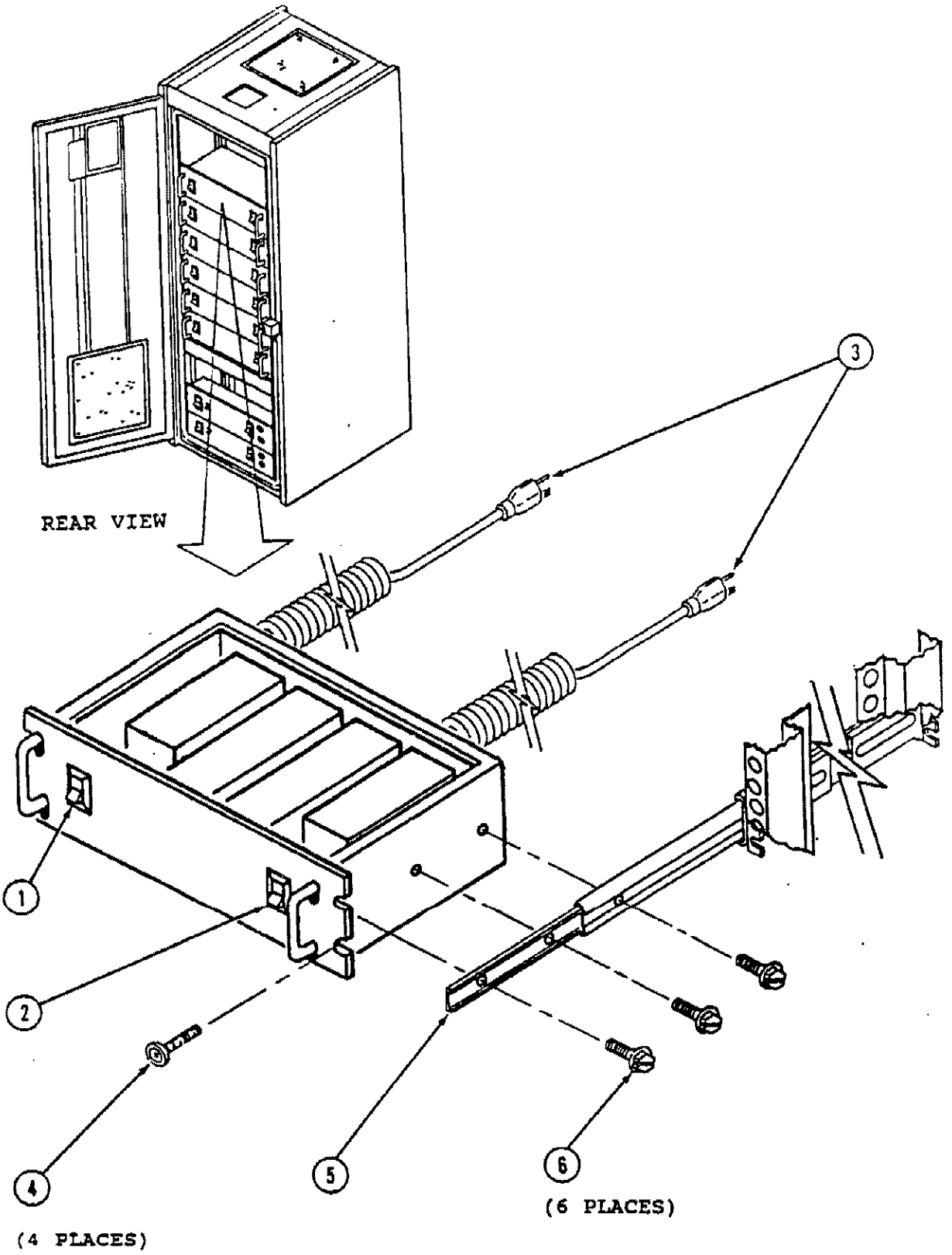


FIGURE 7-9. POWER SUPPLY ASSEMBLY REMOVAL AND REPLACEMENT

7.4.3 Power Supply Module

Use paragraphs 7.4.3.1 and 7.4.3.2 along with figure 7-10 to remove and replace a power supply module.

7.4.3.1 Removal

1. Open rear door of CCU or PCU cabinet (front door of RCU cabinet).
2. Set control unit ac power distribution assembly(s) circuit breaker(s) to OFF (see figure 7-8 (1) and (2)).
3. Set power supply assembly circuit breaker(s) (1) to OFF.
4. Remove the four Phillips-head screws (2) which secure the power supply assembly to the cabinet mounting rails.
5. Carefully slide the power supply assembly (3) out of the cabinet to the full extent of the mounting rails.
6. Loosen the four Phillips-head screws (4) used to secure the power supply module (5) or (6) to the power supply assembly mounting bars.
7. Disconnect the wired plugs connected to J4, J5, J6, and P7 (7) (5 V power supply module) or to J7 and J8 8 (±12 V power supply module).
8. Slide the power supply module slightly to the right, and lift the module off the four mounting bar securing screws (4).
9. Remove the four screws which secure the screen to the power supply.
10. Remove the wiring harnesses that are attached to the power supply. Retain these harnesses so that they can be attached to the new power supply. Reference figure 11-18 for schematic drawings of the power supplies.

7.4.3.2 Replacement. Replacement is the reverse of the removal procedures.

NOTE

Before connecting the wiring harnesses of the HD5-12 power supply, verify that the jumper between the power supply terminals and the sense terminals has been removed. If it is still there, remove the jumper.

7.4.4 Multibus Cardcage Assembly

Use paragraphs 7.4.4.1 and 7.4.4.2 along with figure 7-11 to remove and replace a Multibus cardcage assembly.

7.4.4.1 Removal

1. Open the front and back doors to the control cabinet.
2. Turn circuit breakers OFF on the power supply assembly providing power to the Multibus being removed. See the dc power supply diagram (figure 11-18, sheets 1 through 4) to determine which power supply assembly to turn OFF.
3. Turn knurled knobs (1) on front panel (2) 1/2-turn counterclockwise, and lower panel to horizontal position.

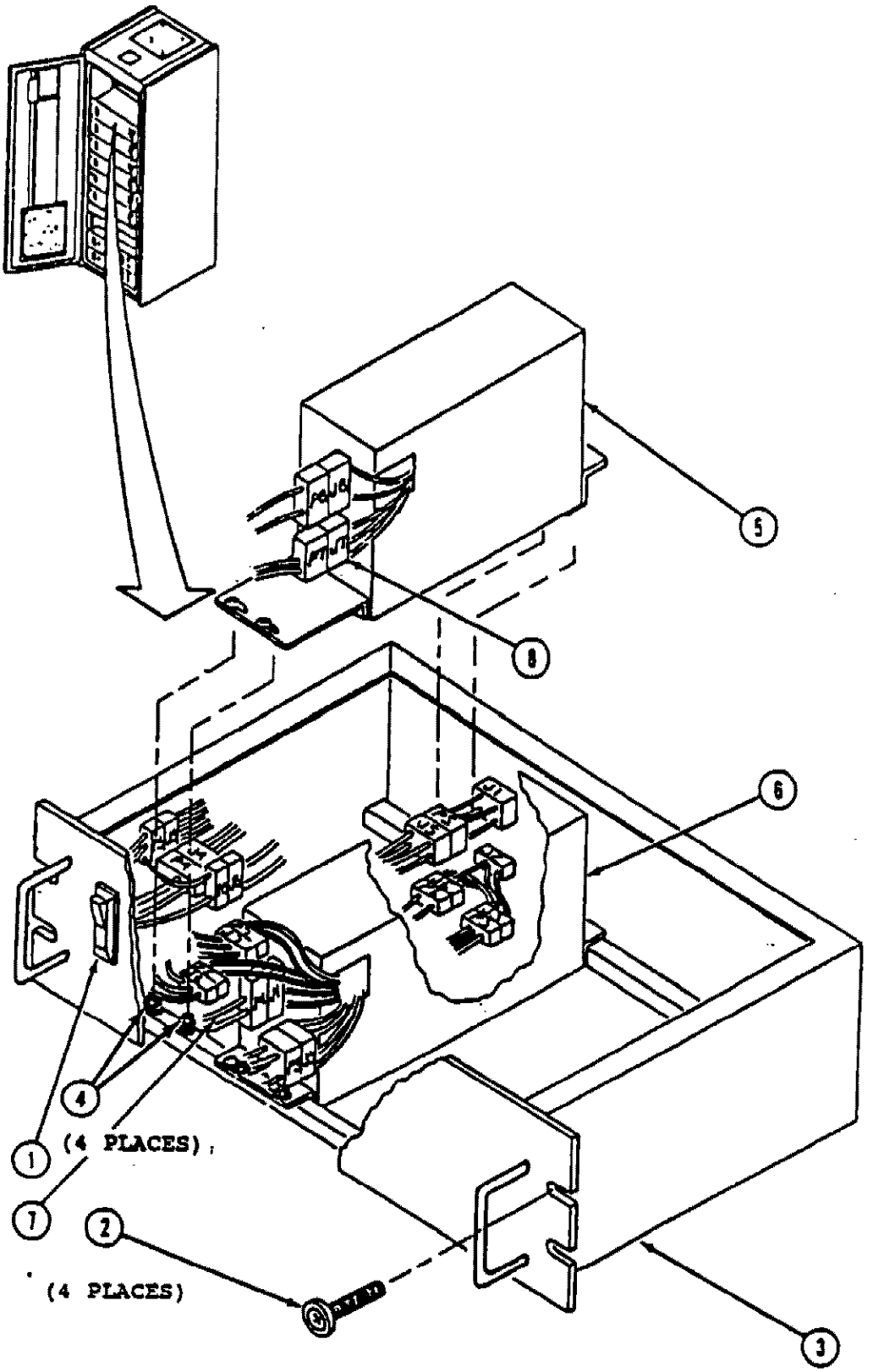


FIGURE 7-10. POWER SUPPLY MODULE REMOVAL AND REPLACEMENT

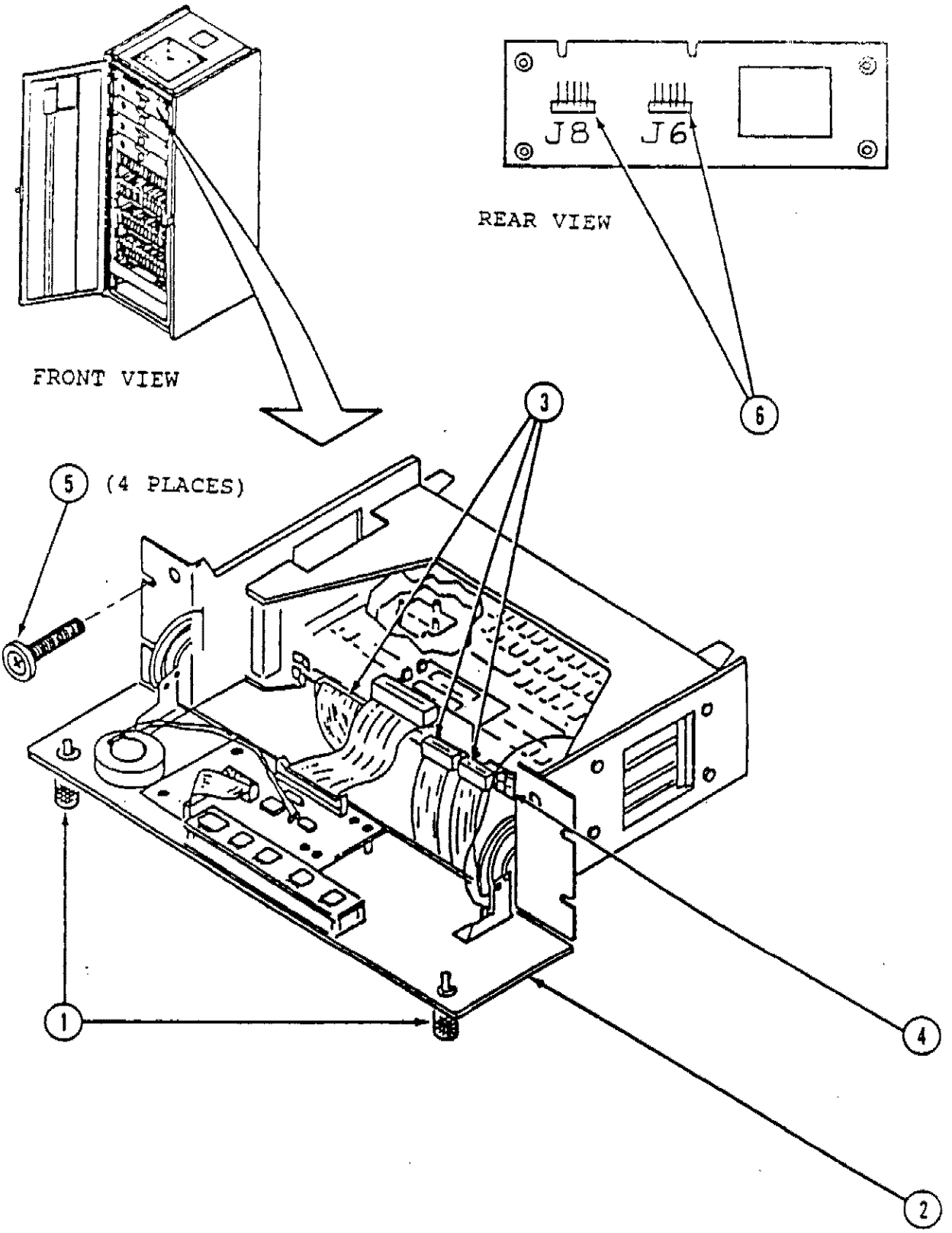


FIGURE 7-11. MULTIBUS CARDCAGE ASSEMBLY REMOVAL AND REPLACEMENT

4. Disconnect all data cables (3) from PCBs in Multibus assembly (CPU, utility, front panel interface, and terminator boards in the CCU or PCU cabinets; CPU, 16 K RCU memory expansion, and front panel interface boards in the RCU cabinet).
5. Disconnect utility board ground wire (4) from utility board connector.
6. Support the Multibus cardcage assembly, and remove the four Phillips-head screws (5) (two to a side) that hold the cardcage assembly to the cabinet vertical mounting rails.
7. While supporting, pull assembly about halfway out of cabinet until dc power cables attached to J6 and J8 (6) on Multibus backplane board (rear side) can be reached and disconnected.
8. Remove Multibus cardcage assembly from cabinet, and place on properly supported work surface.

7.4.4.2 Replacement. Replacement is the reverse of the removal procedure.

7.4.5 iSBC 88/45 Board

Use paragraphs 7.4.5.1 and 7.4.5.2 along with figure 7-12 to remove and replace a CPU board.

7.4.5.1 Removal

1. Open the front and back doors to the control cabinet.
2. Turn circuit breakers OFF on the power supply assembly providing power to the Multibus cardcage assembly housing the board being removed. See the dc power diagram (figure 11-18, sheets 1 through 4) to determine which power supply assembly to turn OFF.
3. Turn knurled knobs (1) on front panel (2) 1/2-turn counterclockwise, and lower panel to horizontal position.
4. Disconnect all data cables (3) from CPU board (4) and front panel interface board (6).

NOTE

The CPU board in the RCU also has a cable connected to J2 that must be disconnected.

5. Remove CPU board by applying pressure to the two ejectors (5) on front edge of board and sliding board out of Multibus slot.
6. Once CPU board is removed, remove the front panel interface board (6) from the CPU board in the following manner:
   a. Squeeze the spacer lock on the standoff spacer that supports the front panel interface board above the CPU board with a pair of needle nose pliers.
   b. Lift the front panel interface board off the standoff and away from the CPU board J5 connector.

7.4.5.2 Replacement. Replacement is the reverse of the removal procedure.

CAUTION

Make sure that P1 of the front panel interface board is properly aligned with J5 of the CPU board before applying pressure to the interface board to reconnect the two boards. If not properly aligned, both P1 and J5 can be damaged.

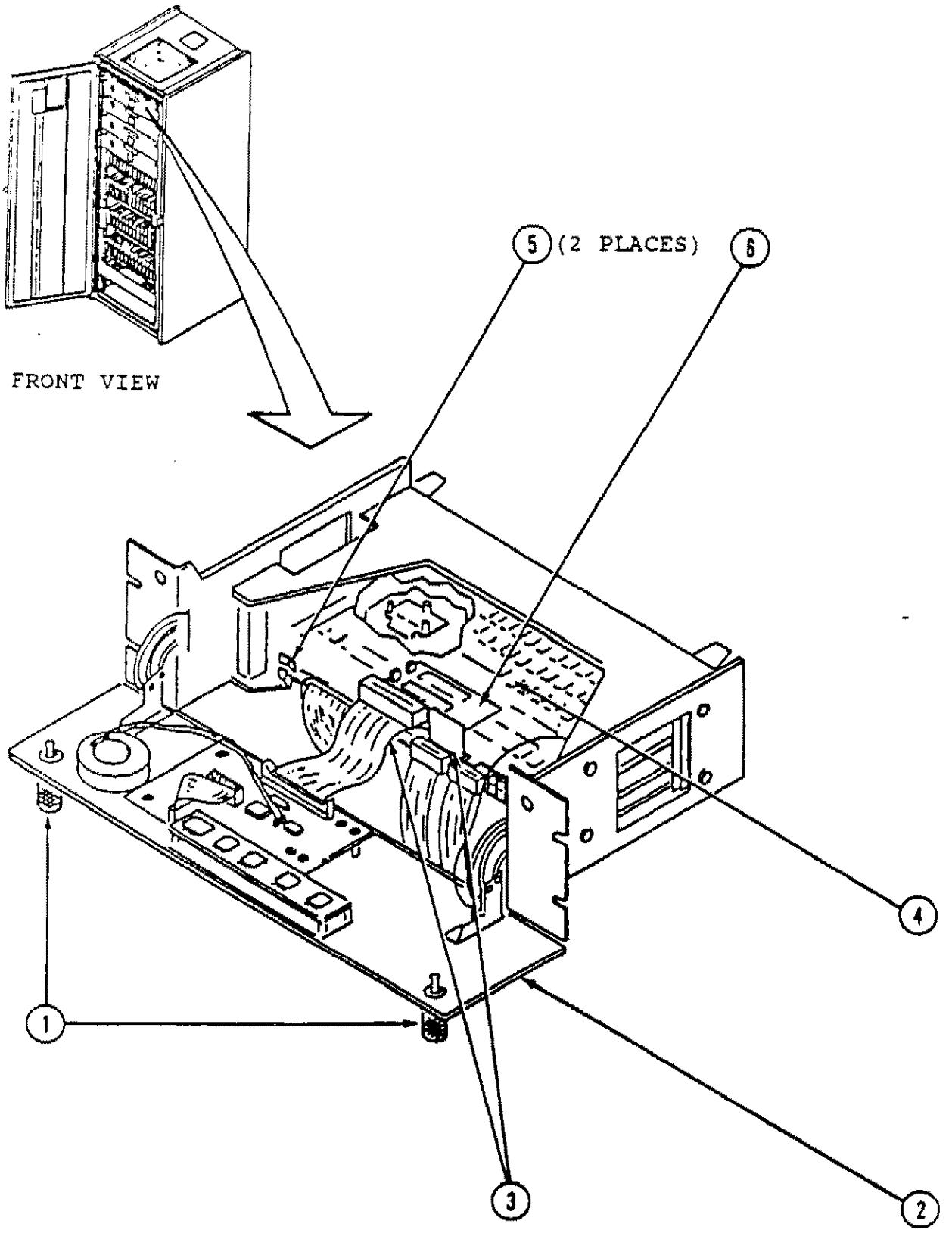


FIGURE 7-12. iSBC 88/45 BOARD REMOVAL AND REPLACEMENT

7.4.6 Utility Board

Use paragraphs 7.4.6.1 and 7.4.6.2 along with figure 7-13 to remove and replace a utility board.

7.4.6.1 Removal

1. Open the front and back doors to the control cabinet.

2. Turn circuit breakers OFF on the power supply assembly providing power to Multibus cardcage housing the board being removed. See the dc power diagram (figure 11-18, sheets 1 through 4) to determine which power supply assembly to turn OFF.

3. Turn knurled knobs (1) on front panel (2) 1/2-turn counterclockwise, and lower panel to horizontal position.

4. Disconnect all data cables (3) from utility board (4) in the Multibus cardcage assembly.

5. Disconnect utility board ground wire (5) from board connector.

6. Disconnect data cable (6) connected to J1 of the front panel interface board (7).

7. Remove utility board by applying pressure to the two ejectors (8) on the front edge of board and sliding board out of Multibus slot.

7.4.6.2 Replacement. Replacement is the reverse of the removal procedure.

7.4.7 16 K RCU Memory Expansion Board

Use paragraphs 7.4.21 and 7.4.7.2 along with figure 7-14 to remove and replace a 16 K RCU memory expansion board from the RCU.

7.4.7.1 Removal

1. Open the front door to the control unit.

2. Turn circuit breakers OFF on the power supply assembly providing power to the Multibus cardcage assembly housing the board being removed. See dc power diagram (figure 11-18, sheets 1 through 4) to determine which power supply assembly to turn OFF.

3. Turn knurled knobs (1) on front panel (2) 1/2-turns counterclockwise, and lower panel to horizontal position.

4. Disconnect data cable (3) connected to J1 of the front panel interface board (4).

5. Remove 16 K RCU memory board (5) by applying pressure to the two ejectors (6) on the front edge of board and sliding board out of Multibus slot.

7.4.7.2 Replacement. Replacement is the reverse of the removal procedure.

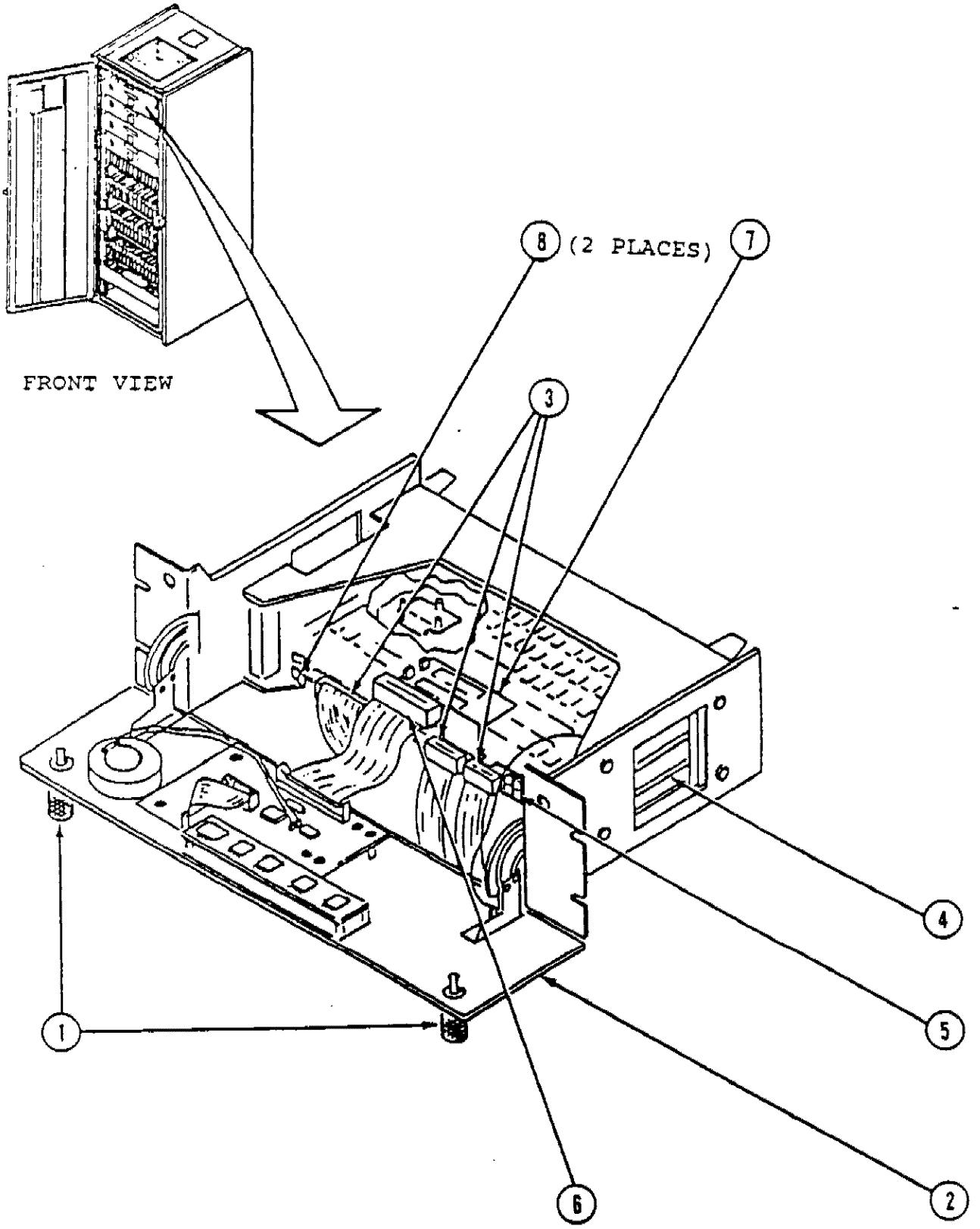


FIGURE 7-13. UTILITY BOARD REMOVAL AND REPLACEMENT

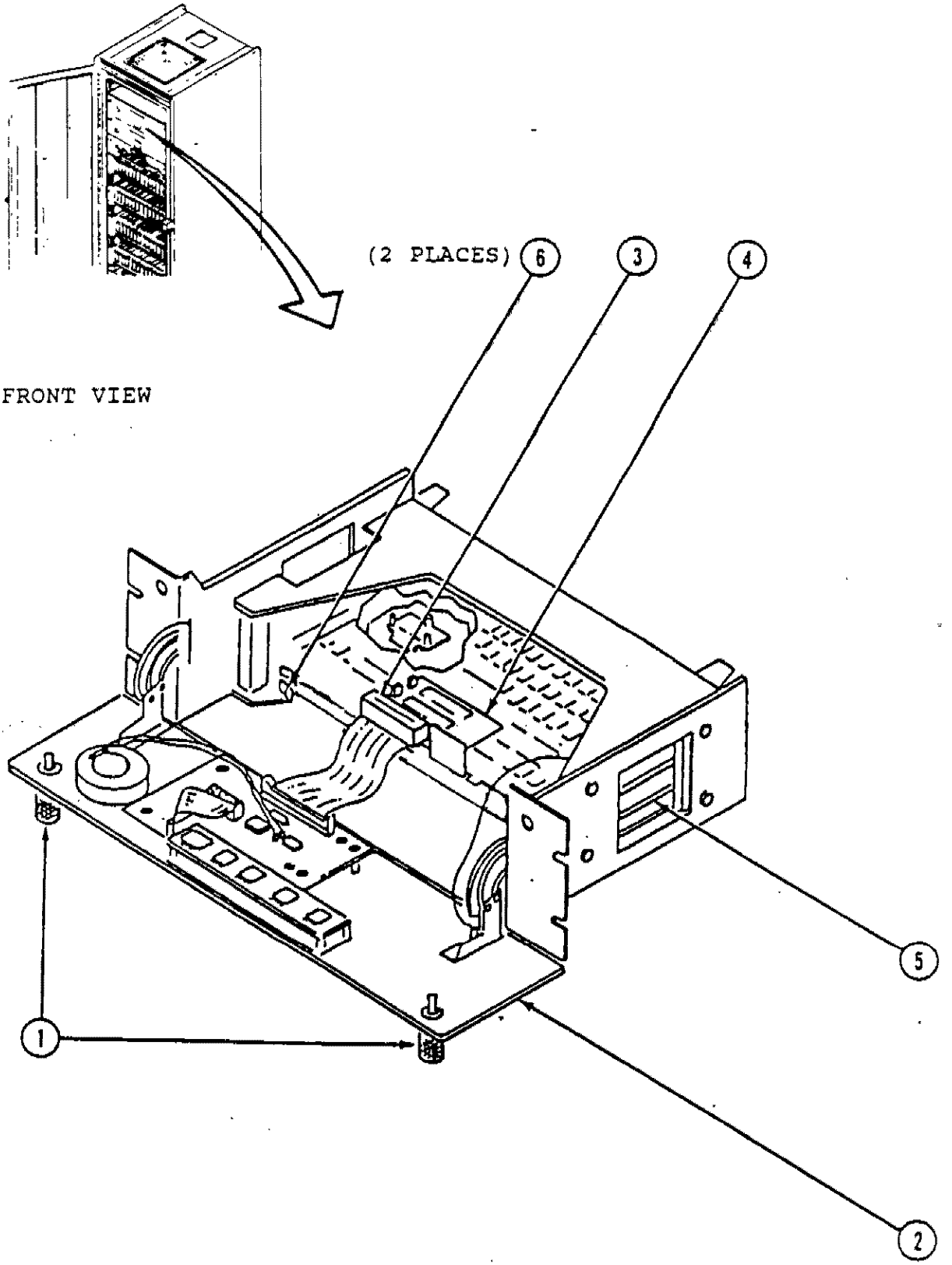


FIGURE 7-14. 16 K RCU MEMORY EXPANSION BOARD

7.4.8 Front Panel Interface

Use paragraphs 7.4.8.1 and 7.4..8.2 along with figure 7-15 to remove and replace a front panel interface board.

7.4.8.1 Removal

1. Open the front and back doors to the control cabinet.

2. Turn circuit breakers OFF on the power supply assembly providing power to the Multibus cardcage assembly housing the board being removed. See dc power diagram (11-18, sheets 1 through 4) to determine which power supply assembly to turn OFF.

3. Turn knurled knobs (1) of front panel (2) 1/2-turns counterclockwise and lower panel to horizontal position.

4. Disconnect all data cables (3) from CPU board (4) and front panel interface board (6).

NOTE

The CPU board in the RCU also has a cable connected to J2 that must be disconnected.

5. Remove CPU board by applying pressure to the two ejectors (5) on front edge of board and sliding board out of Multibus slot.

6. Once CPU board is removed, remove the front panel interface board (6) from the CPU board as follows:

   a. Squeeze the spacer lock on the standoff spacer that supports the front panel interface board above the CPU board with a pair of needle nose pliers.

   b. Lift the front panel interface board off the standoff and away from CPU board J5 connector.

7.4.8.2 Replacement. Replacement is the reverse of the removal procedure.

CAUTION

Make sure that P1 of the front panel interface board is properly aligned with J5 of the CPU board before applying pressure to the interface board to reconnect the two boards. If not properly aligned, both P1 and J5 can be damaged.

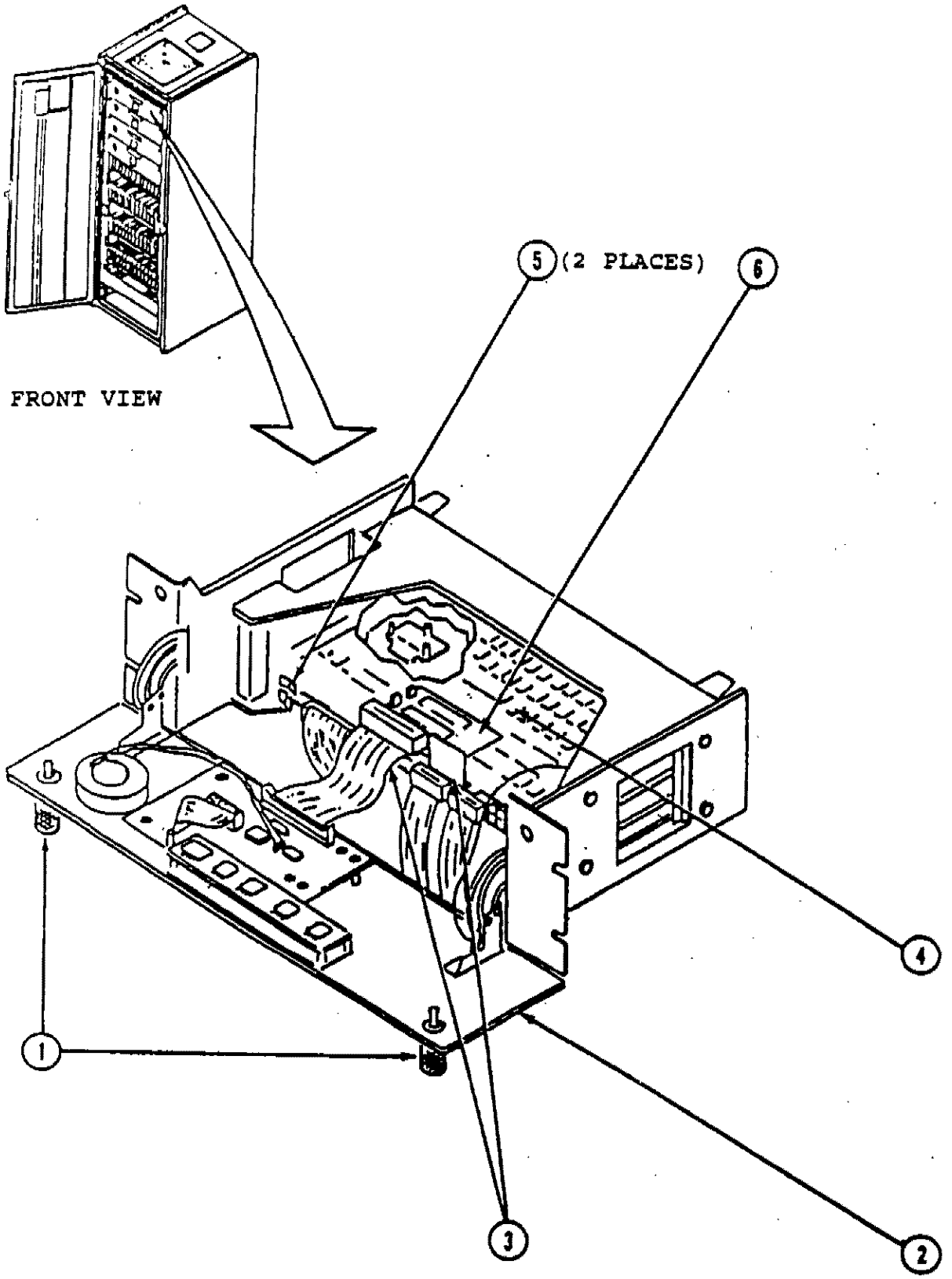


FIGURE 7-15. FRONT PANEL INTERFACE BOARD REMOVAL AND REPLACEMENT

7.4.9 Front Panel Control Board

Use paragraphs 7.4.9.1 and 7.4.9.2 along with figure 7-16 to remove and replace the front panel control board.

7.4.9.1 Removal

1. Open the front and back doors to the control cabinet.
2. Turn circuit breakers OFF on the power supply assembly providing power to the Multibus cardcage assembly housing the board being removed. See dc power diagram (figure 11-18, sheets 1 through 4) to determine which power supply assembly to turn OFF.
3. Turn knurled knobs (1) on front panel (2) 1/2-turn counterclockwise, and lower panel to horizontal position.
4. Disconnect ribbon cables from J101 (3) and J102 (4) on control board.
5. Disconnect wires from W3 (red+) and W4 (black-) (5) on the control board.
6. Remove four nuts (6) at corners of the control board.
7. Remove front panel control board (7) from front panel (2).

7.4.9.2 Replacement. Replacement is the reverse of the removal procedures.

7.4.10 LCD Module

Use paragraphs 7.4.10.1 and 7.4.10.2 along with figure 7-17 to remove and replace the LCD module.

7.4.10.1 Removal

1. Open the front and back doors to the control cabinet.
2. Turn circuit breakers OFF on the power supply assembly providing power to the Multibus cardcage assembly housing the board being removed. See dc power diagram (figure 11-18, sheets 1 through 4) to determine which power assembly to turn OFF.
3. Turn knurled knobs (1) on front panel (2) 1/2-turn counterclockwise, and lower panel to horizontal position.
4. Disconnect LCD module ribbon cable (3).
5. Remove four nuts (4) at corners of LCD module.
6. Remove LCD module (5) from front panel (2).

7.4.10.2 Replacement. Replacement is the reverse of the removal procedures.

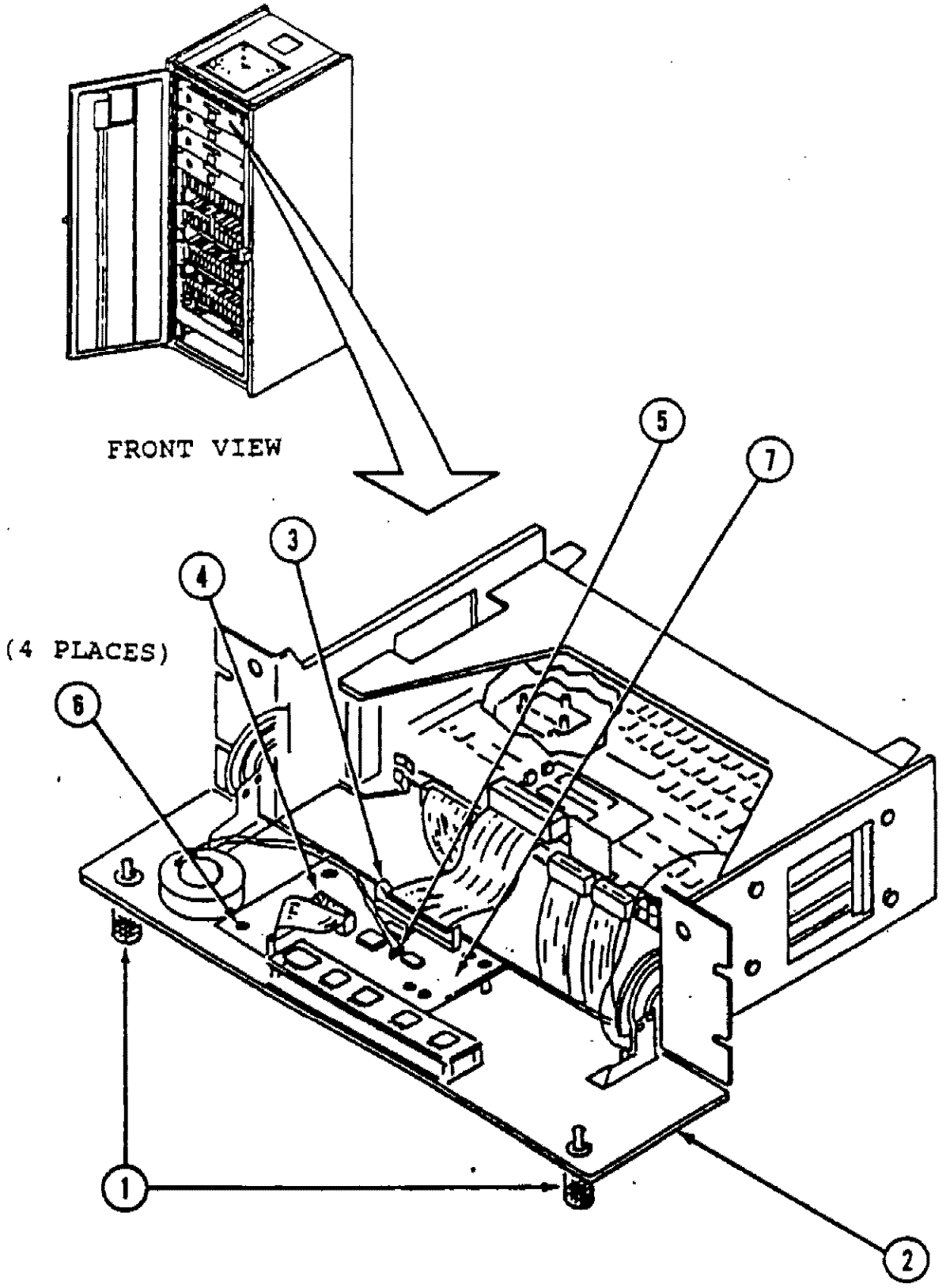


FIGURE 7-16. FRONT PANEL CONTROL BOARD REMOVAL AND REPLACEMENT

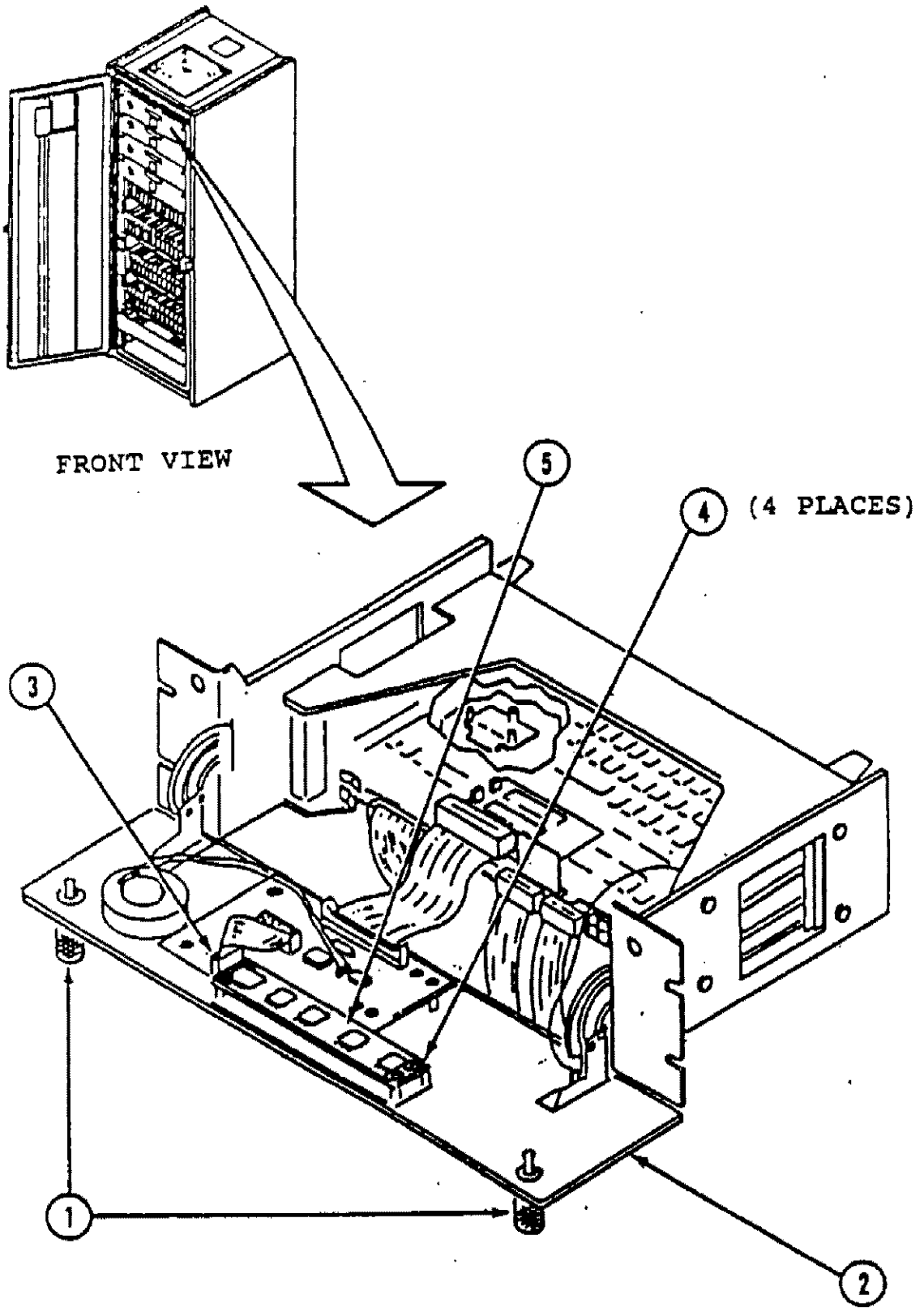


FIGURE 7-17. LCD MODULE REMOVAL AND REPLACEMENT

7.4.11 Audible Alarm

Use paragraphs 7.4.11.1 and 7.4.11.2 along with figure 7-18 to remove and replace the audible alarm.

7.4.11.1 Removal

1. Open the front and back doors to the control cabinet.
2. Turn circuit breakers OFF on the power supply assembly providing power to the Multibus cardcage assembly housing the board being removed. See dc power diagrams (figure 11-18, sheets 1 through 4) to determine which power assembly to turn OFF.
3. Turn knurled knobs (1) on front panel (2) 1/2-turn counterclockwise, and lower panel to horizontal position.
4. Disconnect wires W3 and W4 (3) from the front panel control board. (W3 and W4 are Burg Post type connectors.)
5. Press the audible alarm (4) from the front side of the Multibus front panel until it pops out the rear of the panel. (Alarm is a press in type device.)

7.4.11.2 Replacement. Replacement is the reverse of the removal procedures.

7.4.12 GPI/GPO Interface Board

Use paragraphs 7.4.12.1 and 7.4.12.2 along with figure 7-19 to remove and replace a GPI/GPO interface board.

7.4.12.1 Removal

1. Open the front and back doors to the control cabinet.
2. Disconnect the Host GPI and GPO cables from the interface board (1).
3. Remove the four Phillips-head screws (2) which secure the GPI/GPO interface board to the GPI/GPO panel assembly (3).
4. Remove the eight Phillips-head screws (4) which secure the connectors (5) to the GPI/GPO panel assembly. (Connectors and interface board are soldered together.)
5. Remove the GPI/GPO interface board.

7.4.12.2 Replacement. Replacement is the reverse of the removal procedures.

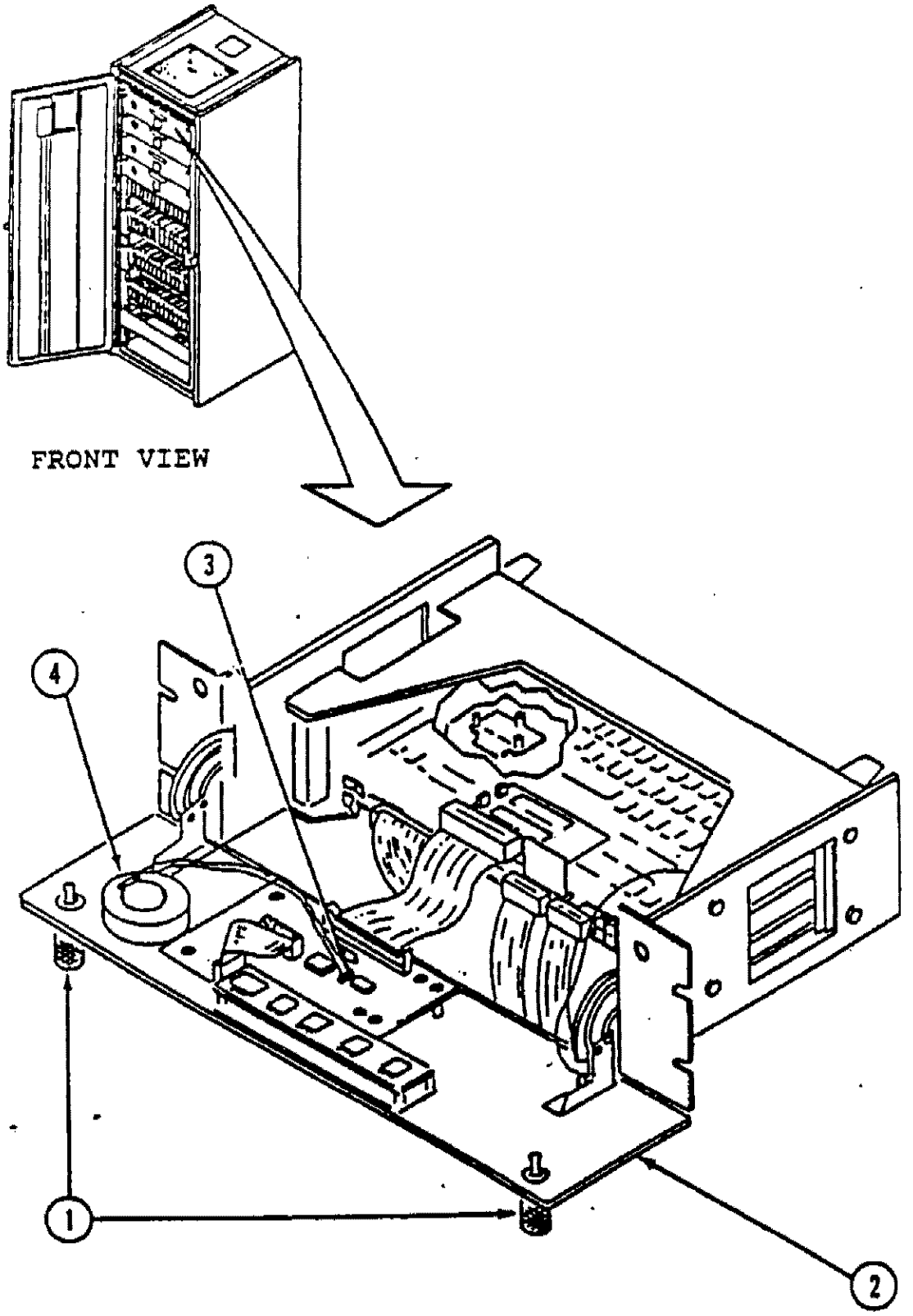


FIGURE 7-18. AUDIBLE ALARM REMOVAL AND REPLACEMENT

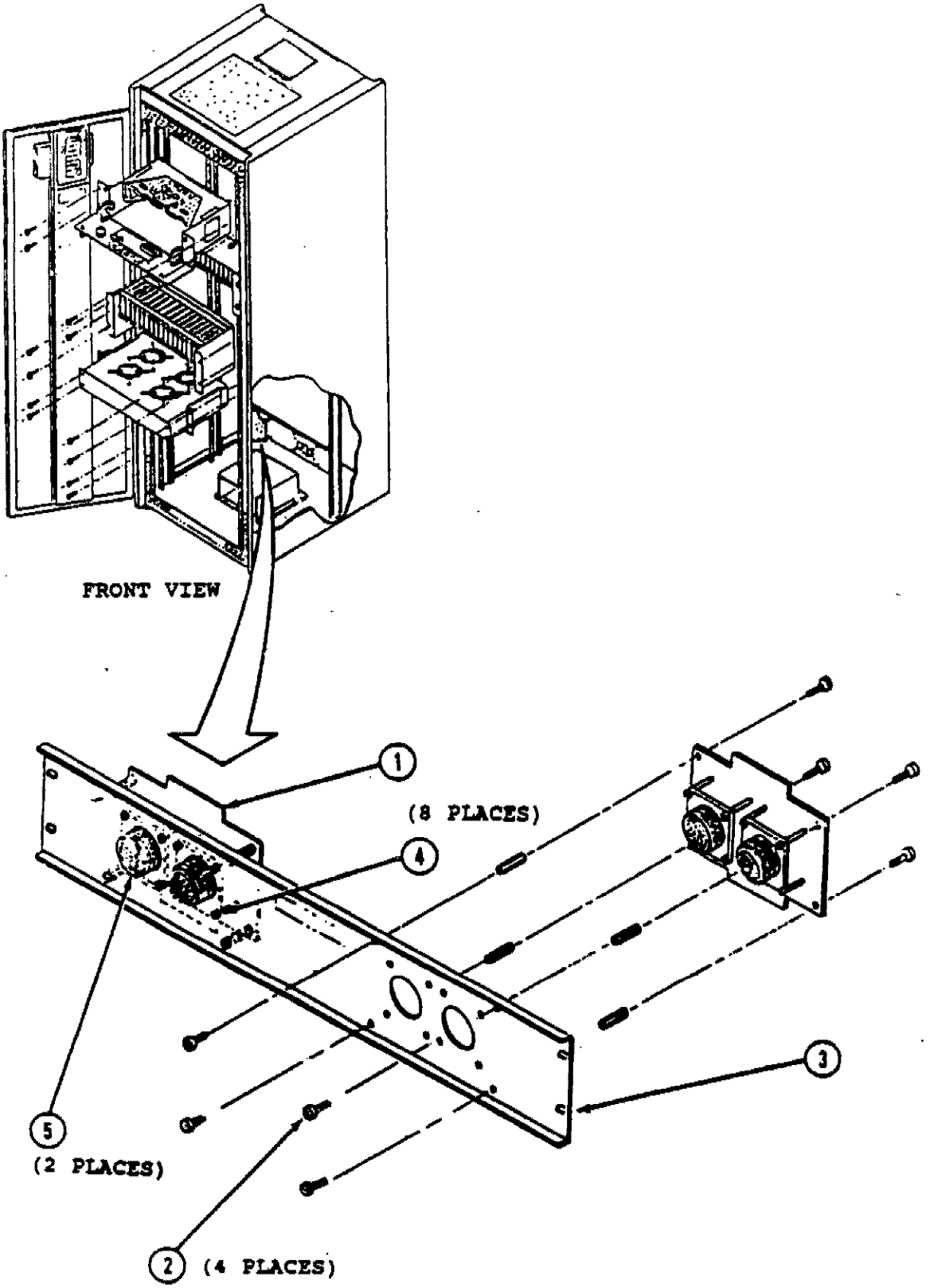


FIGURE 7-19. GPI/GPO INTERFACE BOARD REMOVAL AND REPLACEMENT

7.4.13 Terminator Board

Use paragraphs 7.4.13.1 and 7.4.13.2 along with figure 7-20 to remove and replace the terminator board in CCU or PCU cabinets (RCU cabinets do not have terminator boards).

7.4.13.1 Removal

1. Open the front and back doors to the control cabinet.
2. Turn circuit breakers OFF on the power supply assembly providing power to the Multibus cardcage housing the board being removed. See dc power diagram (figure 11-18, sheets 1 through 4) to determine which power supply assembly to turn OFF.
3. Turn knurled knobs (1) on front panel (2) 1/2-turn counterclockwise, and lower panel to horizontal position.
4. Disconnect all data cables (3) from CPU board (4), front panel interface board (5), and utility board (6).
5. Disconnect utility board ground wire (7) from the board connector.
6. Remove CPU board (4) and utility board (6) by applying pressure to ejectors (8) on front edge of boards and sliding boards out of Multibus slots.

NOTE

Front panel interface board is mounted on CPU board and will be removed along with CPU board.

7. Remove the ribbon cable (9) from the terminator board (10).
8. Squeeze the spacer lock on the three standoff spacers 11 that attach the terminator board to the lower left corner of the Multibus assembly with a pair needle nose pliers, and remove the terminator board from the assembly.

7.4.13.2 Replacement

1. Align three terminator board standoffs 11 with holes in bottom of Multibus assembly, and push up on board until standoffs are locked in place on the assembly.
2. Perform removal procedure using steps 7 through 1 in paragraph 7.4.13.1.

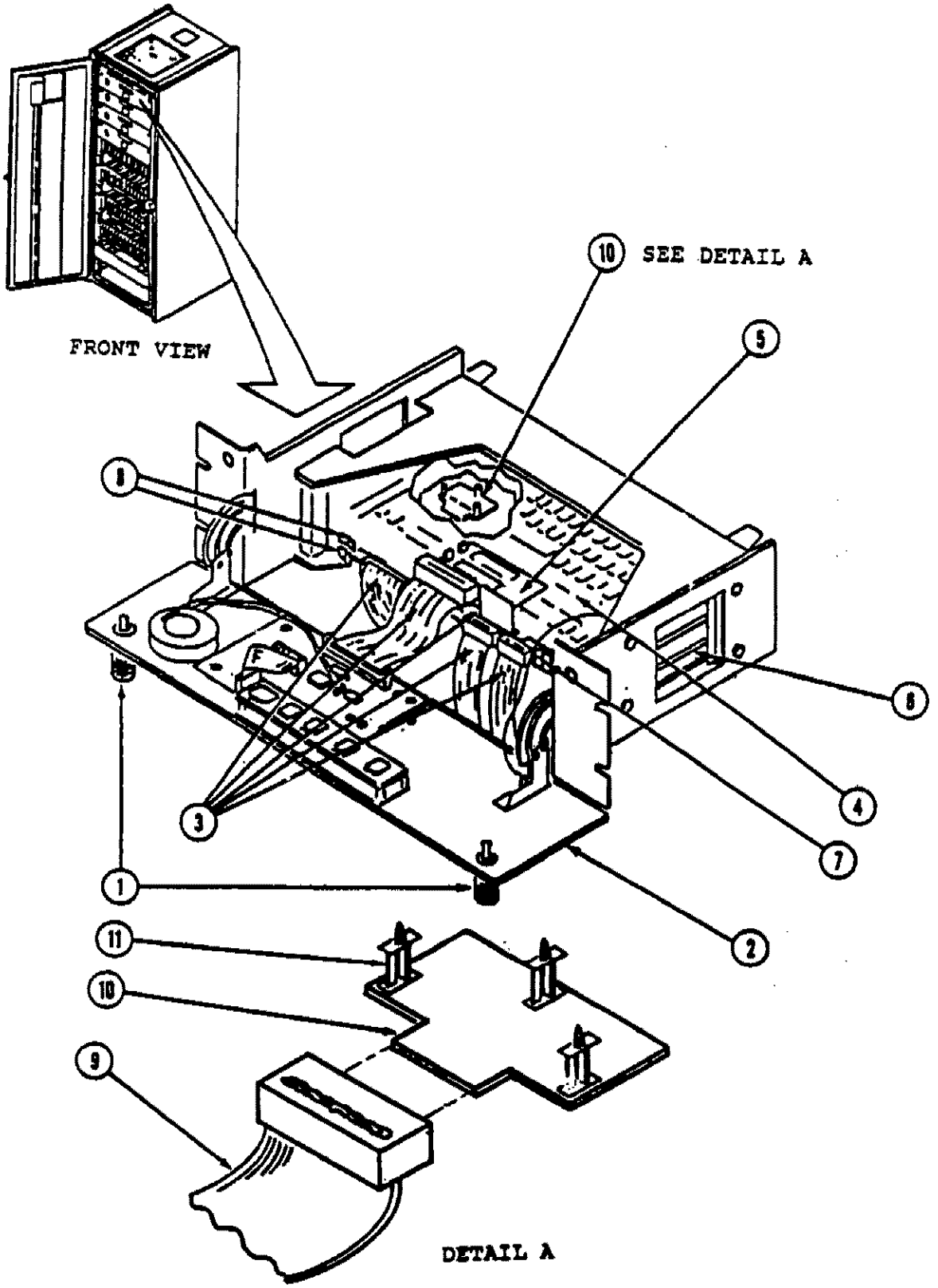


FIGURE 7-20. TERMINATOR BOARD REMOVAL AND REPLACEMENT

7.4.14 BC Board

Use paragraphs 7.4.14.1 and 7.4.14.2 along with figure 7-21 to remove and replace a bus connect board.

7.4.14.1 Removal

1. Open the front door to the control cabinet.
2. Set BC board power switch (1) (located on the front edge of the board) to OFF (down position).
3. Lift up on BC board ejector lever (2).

NOTE

If more than one BC board is being removed, mark the location of each board so it can be returned to same cardcage slot. Each card is addressed for a particular peripheral attached to the cardcage slot. Failure to replace the BC(s) in the original slot(s) can interrupt communications to the peripherals.

4. Slide BC board (3) out of BC card cage.

7.4.14.2 Replacement. Replacement is the reverse of the removal procedure.

7.4.15 BC Cardcage and Backplane Board

Use paragraphs 7.4.15.1 and 7.4.15.2 along with figure 7-22 to remove and replace a BC cardcage and backplane board.

7.4.15.1 Removal

1. Open the front and back doors to the control cabinets.
2. Turn circuit breakers OFF on the power supply assembly providing power to the BC cardcage assembly housing the board being removed.

NOTE

When more than one BC is being removed, mark each board with the original location so the boards can be returned to the same card cage slot. Each card is addressed for a particular peripheral attached to the cardcage slot. Failure to replace the BCs in the original slots can interrupt communications to the peripherals.

3. Remove all BC boards from BC cardcage assembly (refer to paragraph 7.4.14.1, steps 2, 3, and 4).

NOTE

When more than one peripheral cable is being removed, mark each cable with the original BC backplane peripheral connectors (P1 — P16) so the cables can be returned to the original connector location. Each BC is addressed for a peripheral attached to a particular connector. Failure to connect the peripheral cables to the original connectors can interrupt communications to the peripherals.

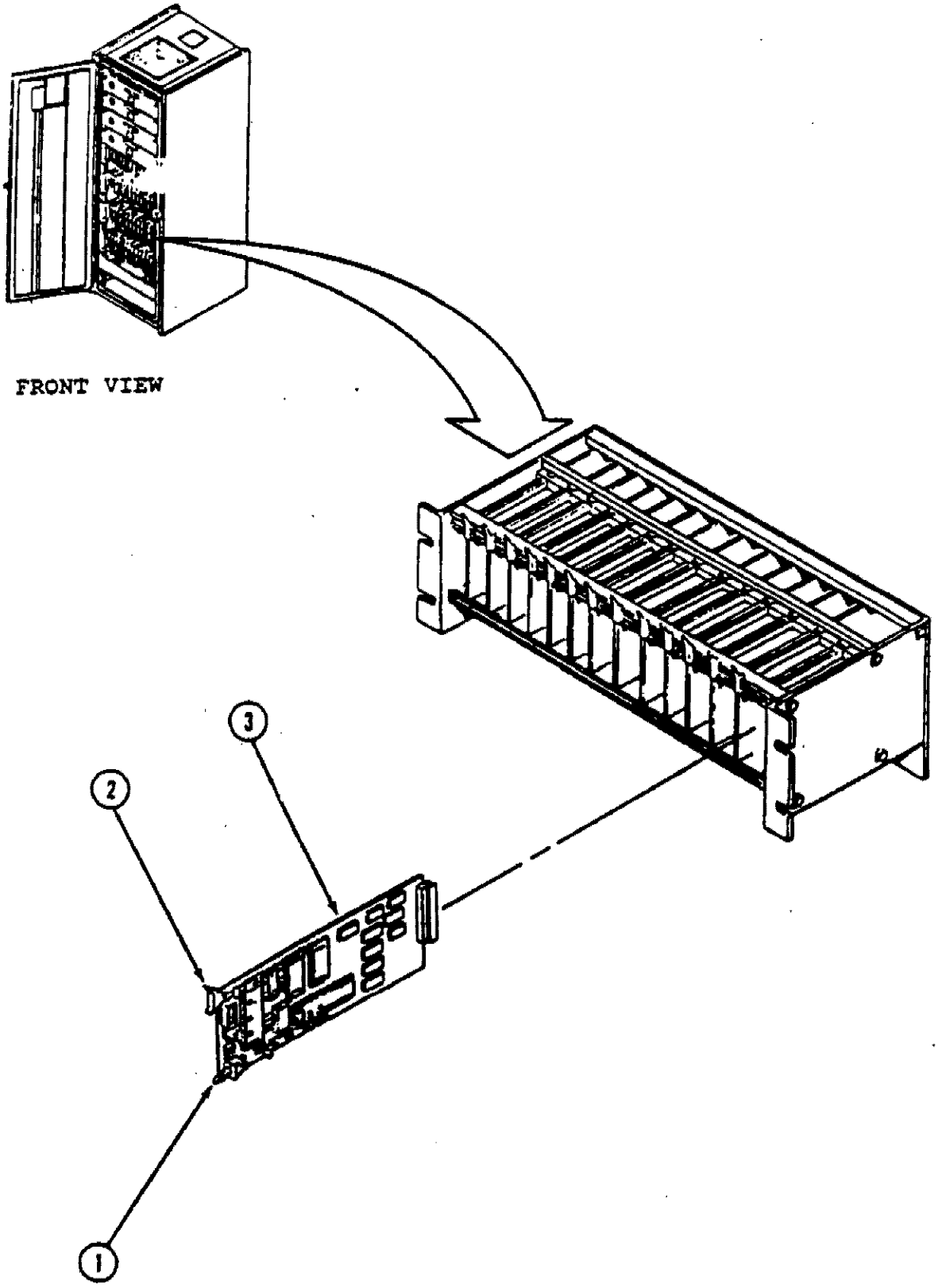


FIGURE 7-21. BC BOARD REMOVAL AND REPLACEMENT

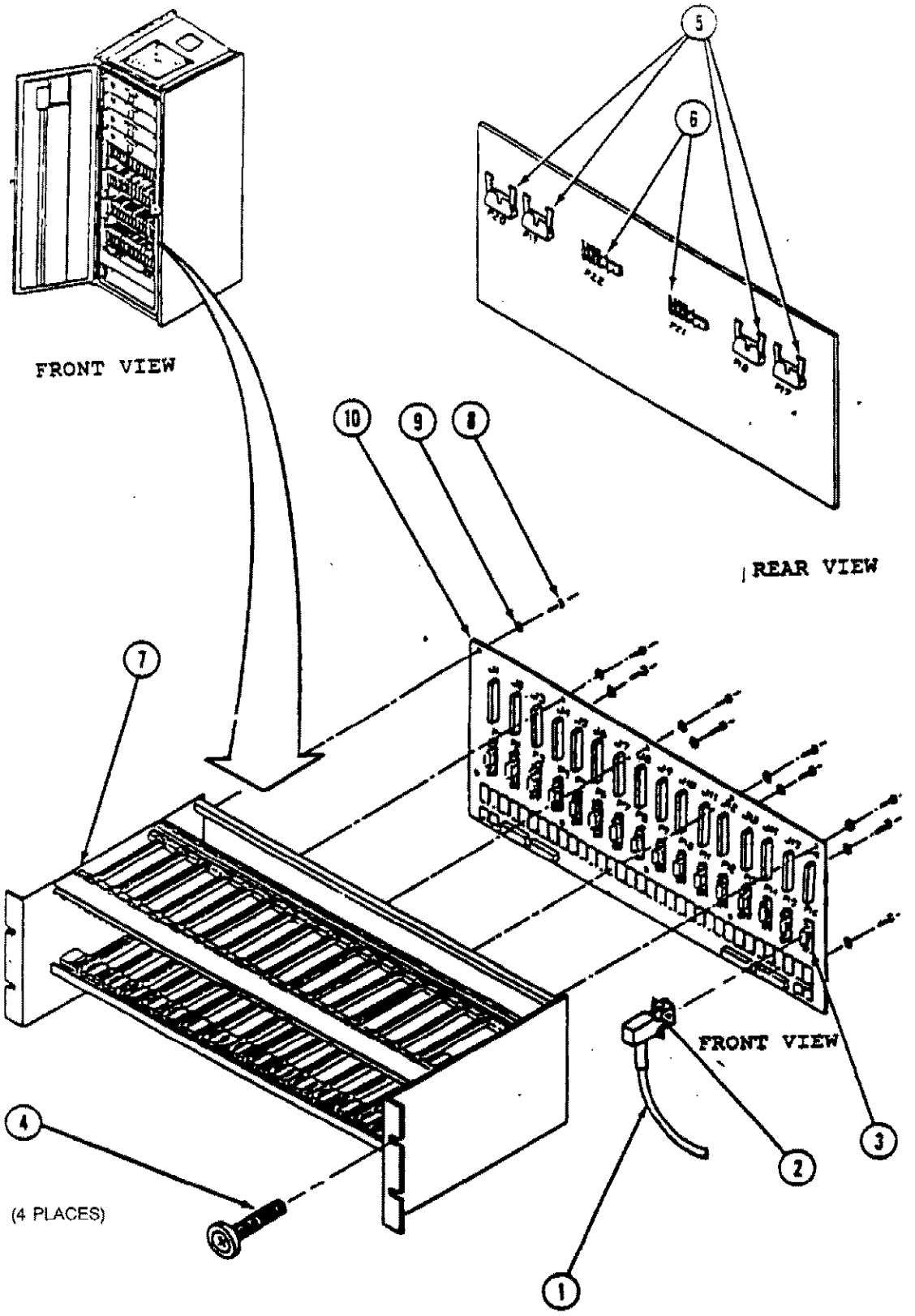


FIGURE 7-22. BC CARDCAGE AND BACKPLANE BOARD REMOVAL AND REPLACEMENT

4. Disconnect all peripheral cables (1) attached to P1 through P16 on the BC backplane. The cables are removed by loosening the two screws (2) (one on each side of the cable plugs) and then disconnecting the cables from the board connectors (3).

5. Support the BC cardcage, and remove the four Phillips-head screws (4) (two to a side) that hold the cardcage assembly to the cabinet vertical mounting rails.

NOTE

The following cables (data and power) are attached to connectors mounted on the rear side of the BC backplane board.

6. While supporting, pull assembly out of cabinet until data cables and dc power cables can be reached and disconnected. The data cables are connected to P17 through P20 (5). The release buttons on each side of the board cable connectors must be pushed in to release the data cables. The dc power cables are connected to P21 and P22 (6). (The power cable connectors are slide on connectors.)

7. Remove BC cardcage assembly (7) from cabinet, and place on properly supported work surface.

8. Remove the 10-slotted HEX HD screws (8) and washers (9) that hold the backplane board to the cardcage assembly, and remove the backplane board (10).

7.4.15.2 Replacement. Replacement is the reverse of the removal procedure.

7.4.16 Fan Assembly

Use paragraphs 7.4.16.1 and 7.4.16.2 along with figure 7-23 to remove and replace the fan assembly.

7.4.16.1 Removal

1. Open the rear and front doors of the cabinet.

2. Unplug the fan assembly power cord from the ac power distribution assembly outlet.

WARNING

It is recommended that another person support the fan assembly while the four mounting screws are being removed to avoid personal injury and/or equipment damage.

3. Remove the four Phillips-head screws (1) which secure the fan assembly (2) and the fan support brackets (3) to the cabinet mounting rails.

4. Remove fan assembly from cabinet, and place on properly supported work surface.

7.4.16.2 Replacement. Replacement is the reverse of the removal procedures.

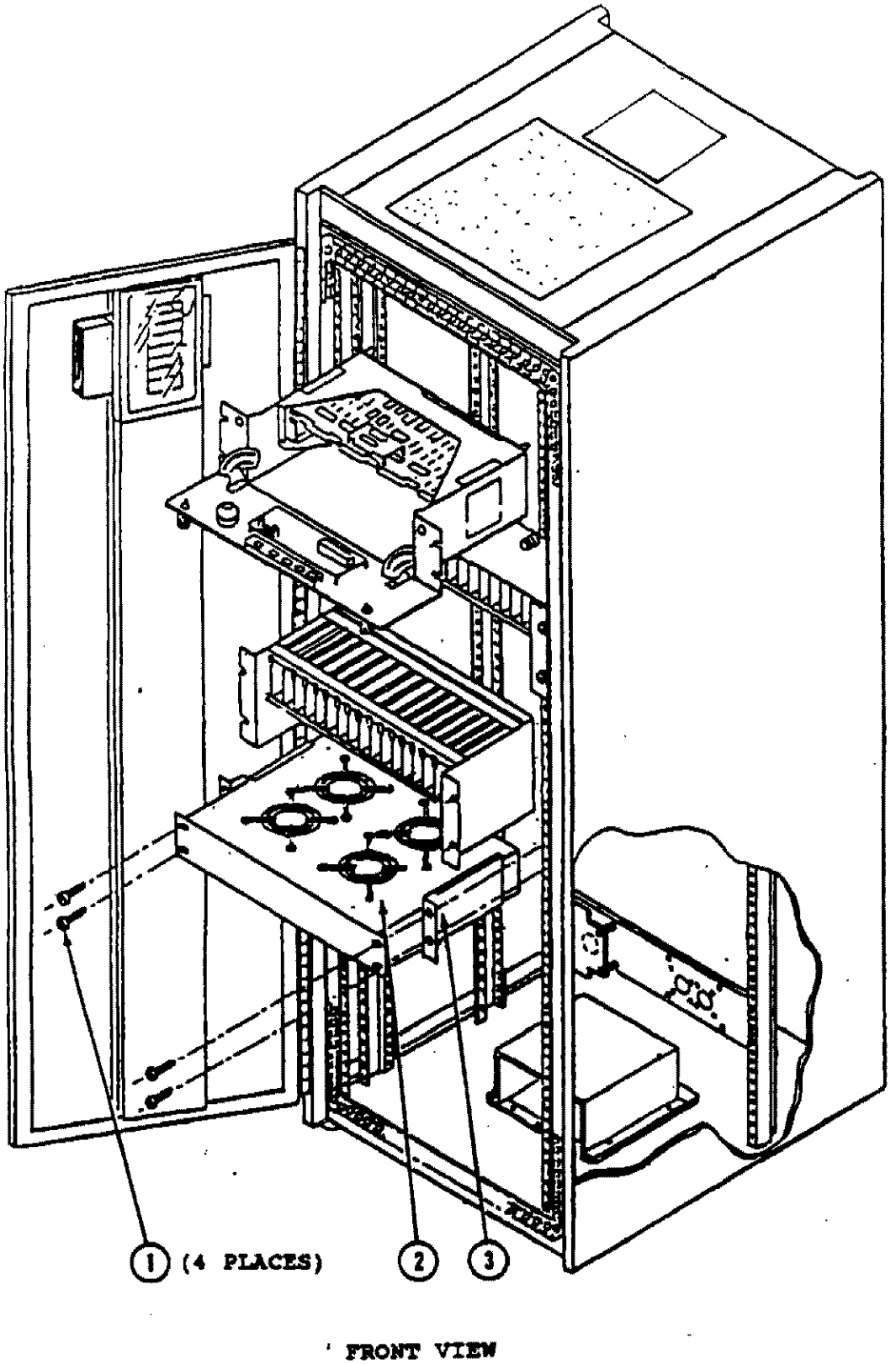


FIGURE 7-23. FAN ASSEMBLY REMOVAL AND REPLACEMENT

7.4.17 RANK

Use paragraphs 7.4.17.1 and 7.4.17.2 along with figure 7-24 (FA 10095/3) and figure 7-25 (FA 10095/17) to remove and replace a RANK peripheral element.

7.4.17.1 Removal

1. Open the front door to the control unit, and turn OFF the associated BC card in the control unit.
2. Turn the RANK power switch (1) to the OFF position.
3. Disconnect the RANK ac power cord (2) from the ac power receptacle.
4. Disconnect data cable (3) from the DB25 connector.

7.4.17.2 Replacement. Replacement is the reverse of the removal procedure.

7.4.18 RANK (FA 10095/3 Only) Keyboard

Use paragraphs 7.4.18.1 through 7.4.18.3 along with figure 7-26 to remove and replace the RANK keyboard from its housing.

7.4.18.1 Removal

1. Remove the RANK from its station. Refer to paragraph 7.4.17.1 for procedures.
2. Remove five Phillips-head screws (1) that secure the RANK cover (2) to the base (3) (three on bottom front and two at top rear corners), and remove top cover.
3. Disconnect P1 (power) and P2 (data) connectors (4) attached to keyboard.
4. Remove the four Phillips-head screws (5) that hold the keyboard (6) to the keyboard support bracket (7) (two at each end of the keyboard), and lift the keyboard out of the base. (Make sure to retain the nylon washers (8).)

7.4.18.2 Replacement. Replacement is the reverse of the removal procedures.

CAUTION

Make sure keyboard is isolated from brackets with the nylon washer.

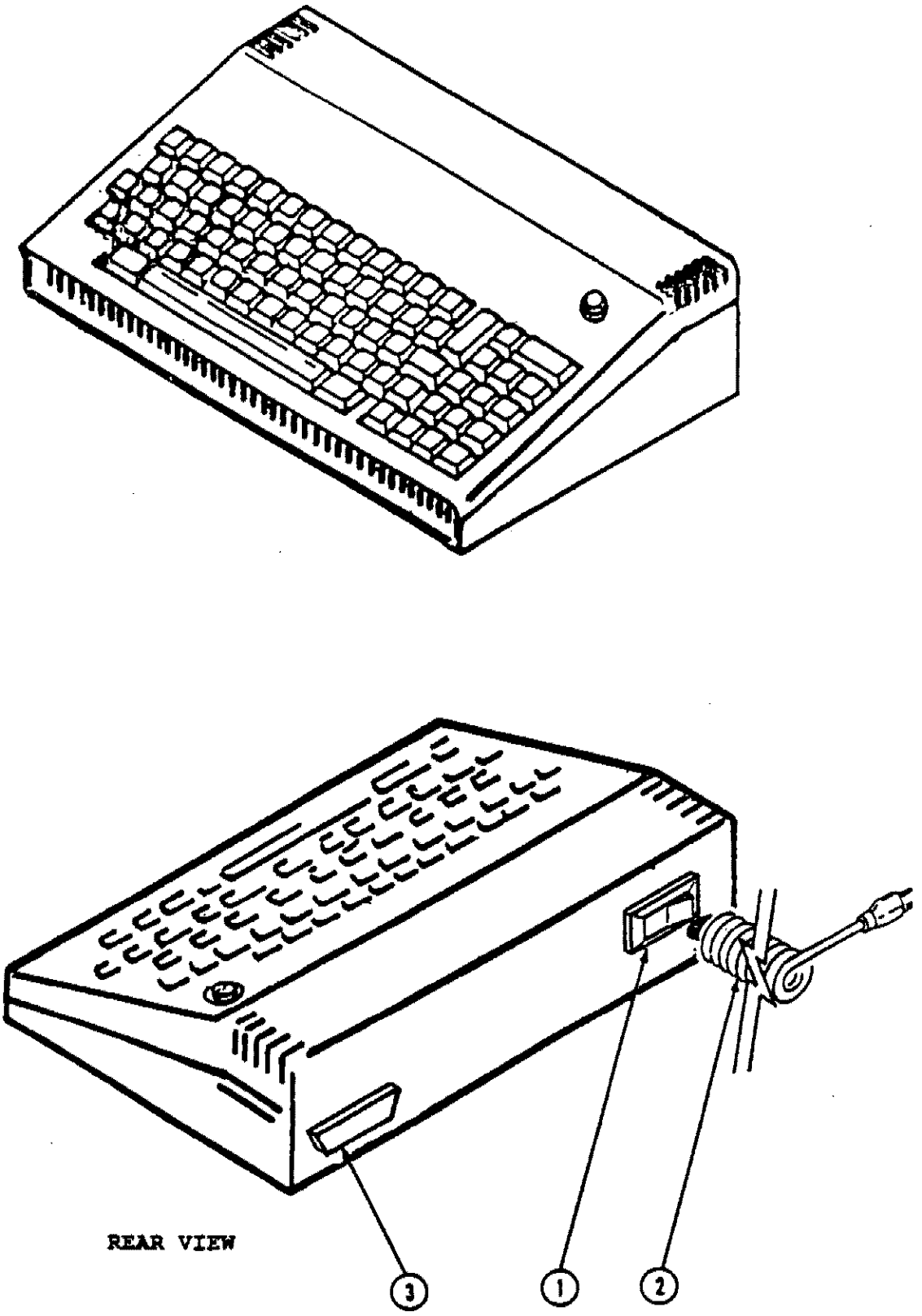
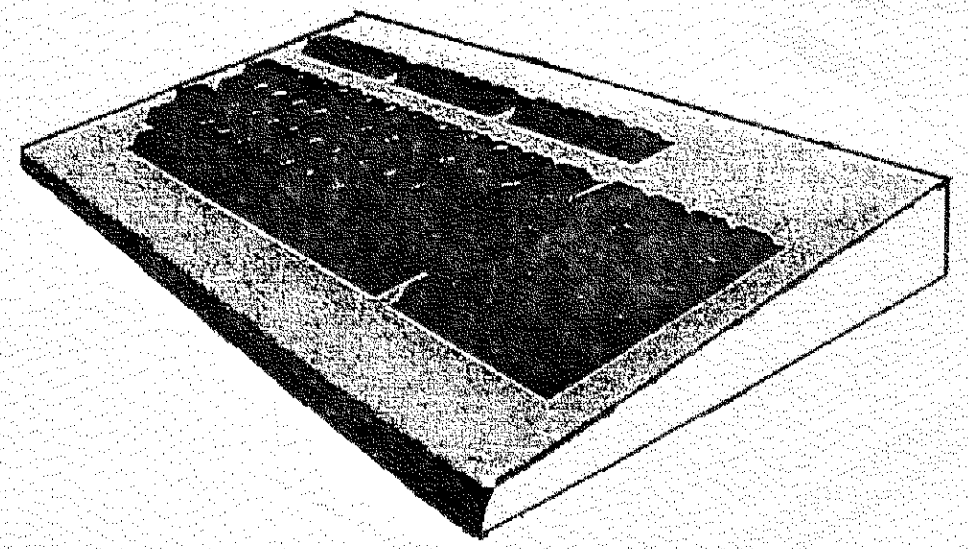


FIGURE 7-24. RANK (FA 10095/3) REMOVAL AND REPLACEMENT



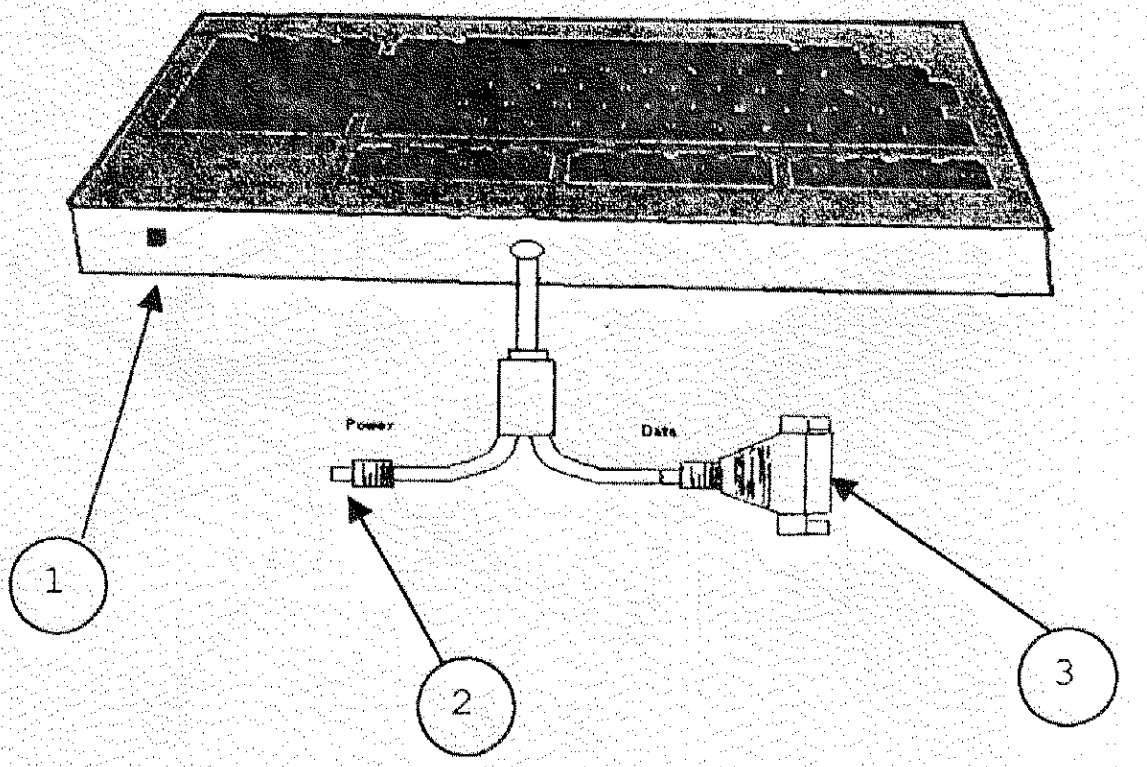


FIGURE 7-25. RANK (FA 10095/17) REMOVAL AND REPLACEMENT

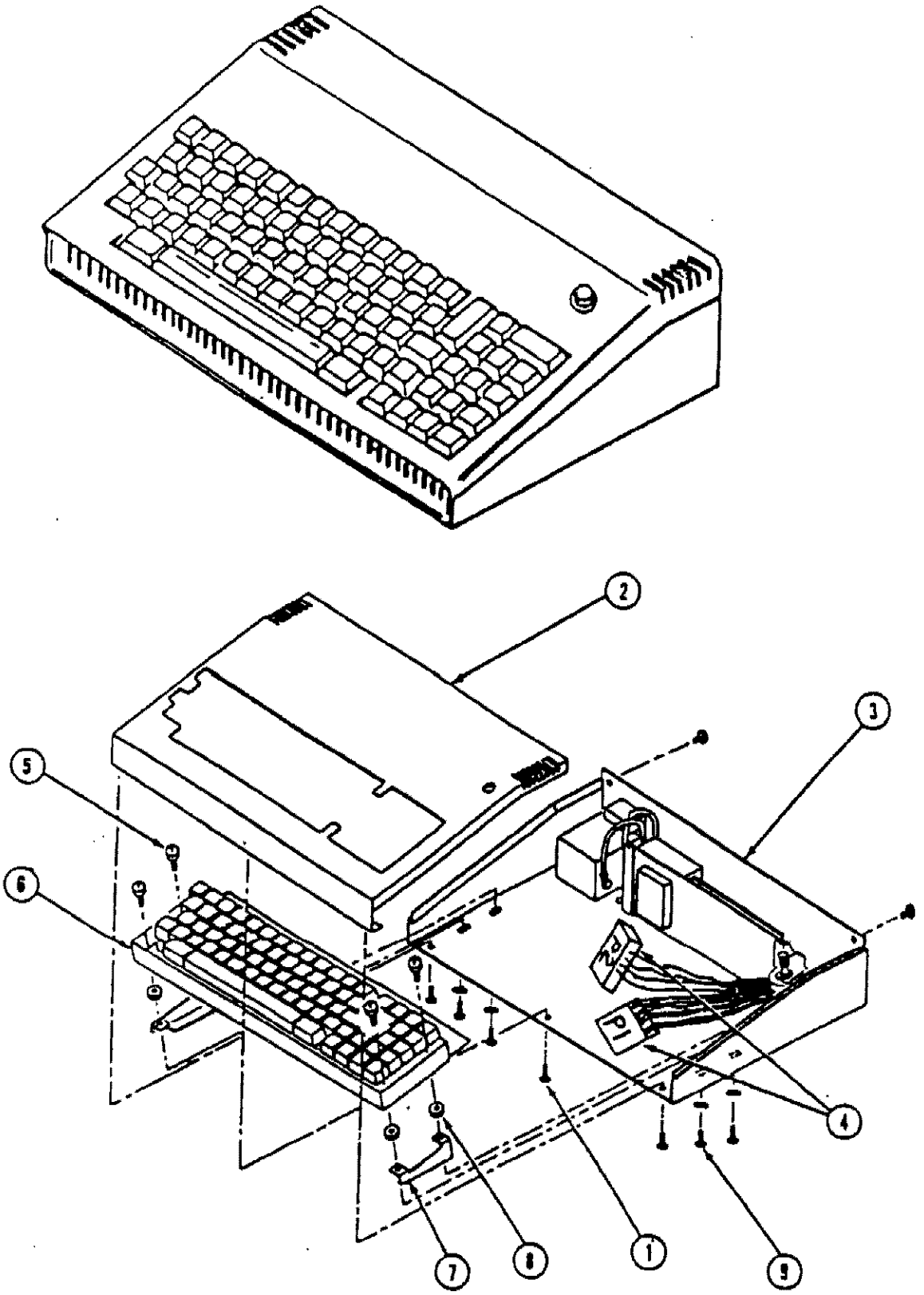


FIGURE 7-26. RANK (FA 10095/3) KEYBOARD REMOVAL AND REPLACEMENT

7.4.18.3 Alignment

1. After installing the cover, check that the keyboard is aligned and all the keys spring up after depressing.

2. If misaligned, loosen the four Phillips-head screws (9) on the bottom of the base that hold the keyboard brackets (two on each side).

3. Reposition the keyboard, tighten the four screws, and recheck the alignment. Repeat if necessary.

7.4.19 RANK (FA 10095/3) Keycap and LAMP and (FA 10095/17) Keycap

Use paragraphs 7.4.19.1 and 7.4.19.2 along with figure 7-27 to remove and replace the (FA 10095/3) RANK keycaps and lamps. Use paragraphs 7.4.19.3 and 7.4.19.4 along with figure 7-27A to remove and replace the (FA 10095/17) RANK keycaps.

NOTE

The paragraphs 7.4.19.1 and 7.4.19.2 procedures are for all RANK (FA10095/3) keycaps except the spacebar. Removal of the spacebar keycap and lamp is in paragraph 7.4.21.1.

7.4.19.1 Removal

1. Turn the RANK power switch (1) OFF.

2. Using keycap extraction tool (2), pull keycap (3) straight up from the keyboard (4) to expose lamp.

3. Press the white plastic key shaft down to expose the lamp, and pull lamp straight up to remove.

7.4.19.2 Replacement. Replacement is the reverse of the removal procedures.

NOTE

Make sure pins on lamp are aligned with the socket when inserting lamp.

7.4.19.3 FA 10095/17 Removal.

1. Turn the RANK power switch (1) OFF.

2. Using keycap extraction tool (2), pull keycap (3) straight up from the keyboard.

7.4.19.4 FA 10095/17 Replacement. Replacement is the reverse of the removal procedures.

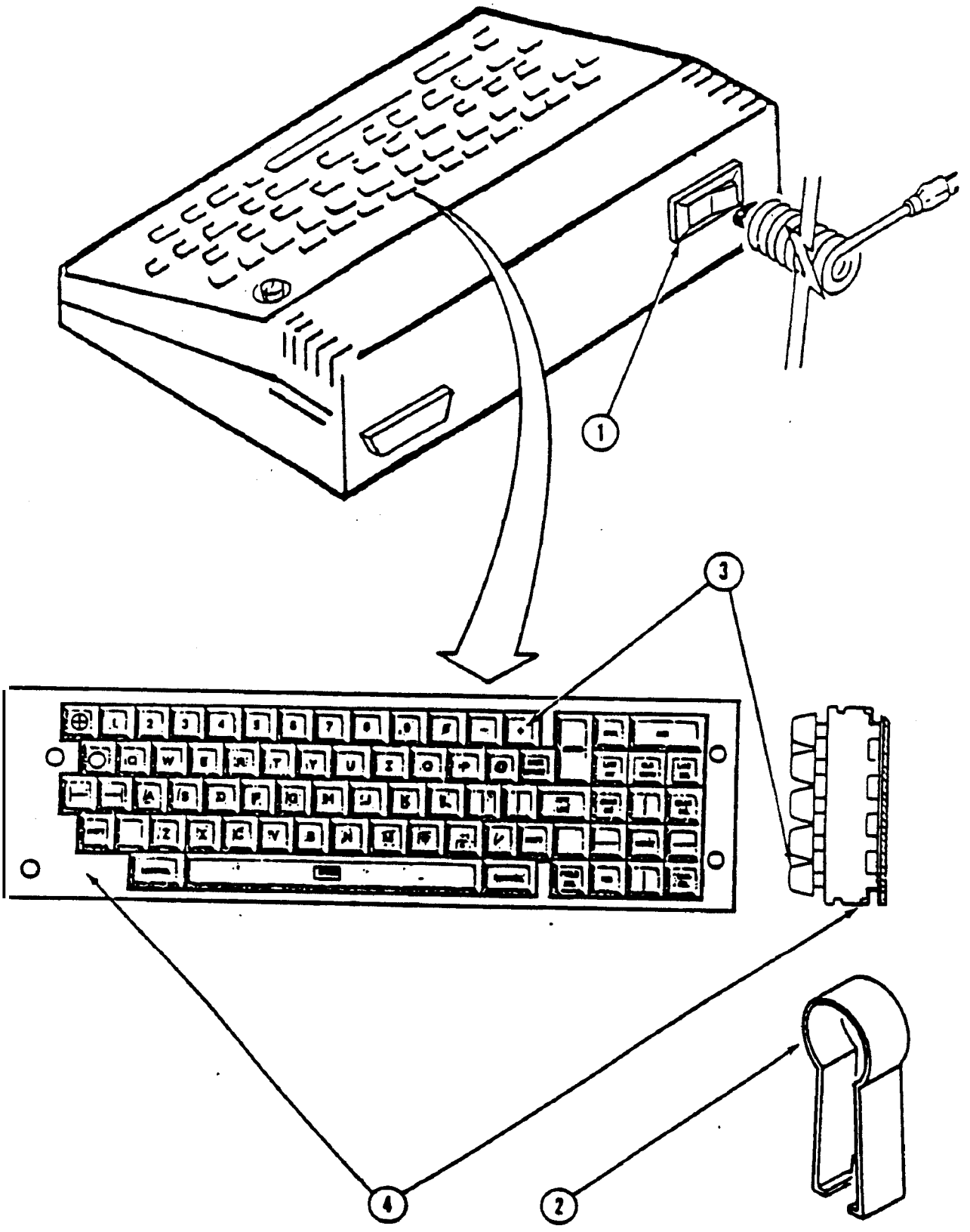


FIGURE 7-27. RANK (FA 10095/3) KEYCAP AND LAMP REMOVAL AND REPLACEMENT

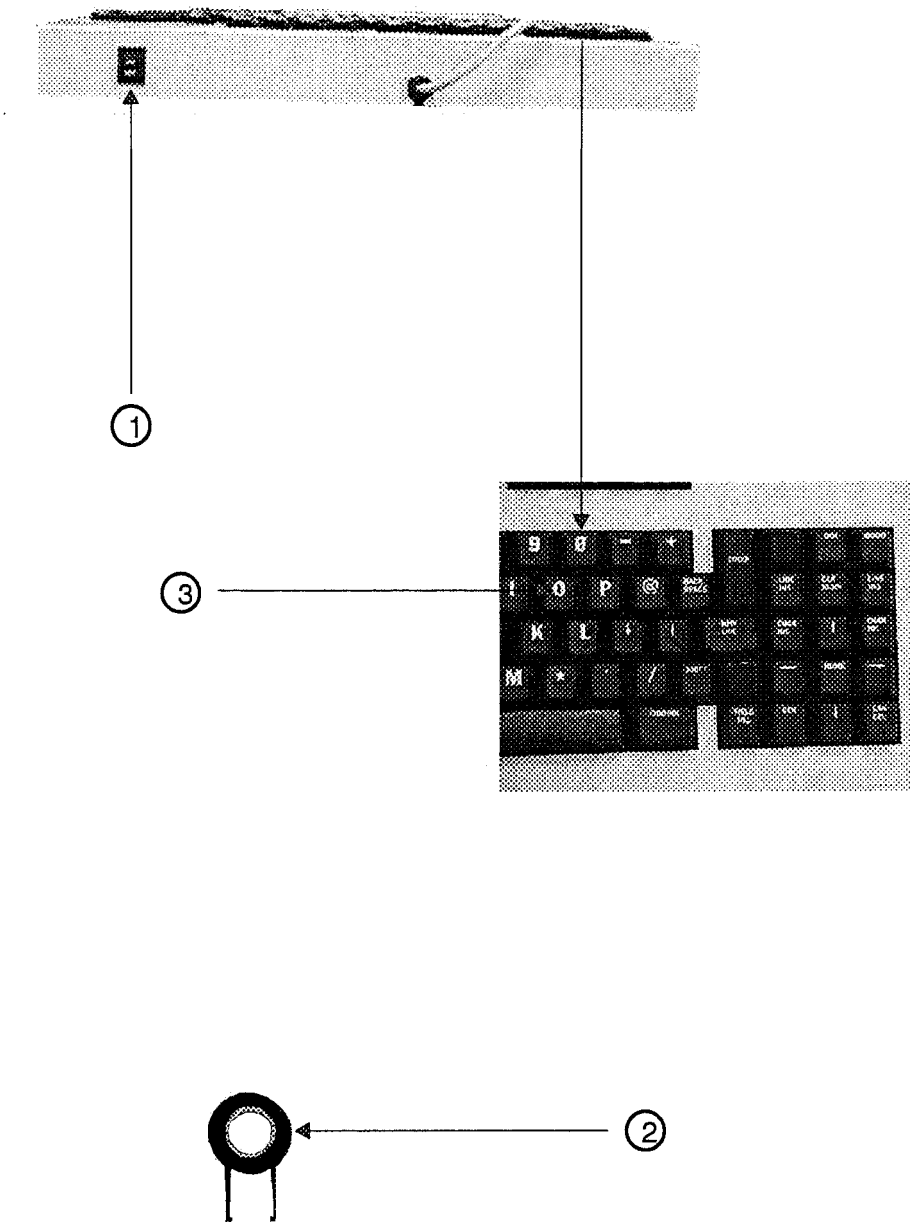


FIGURE 7-27A. RANK (FA 10095/17) KEYCAP REMOVAL AND REPLACEMENT

7.4.20 RANK (FA 10095/3) Power Supply

Use paragaphs 7.4.20.1 and 7.4.20.2 along with figure 7-28 to remove and replace the RANK power supply.

7.4.20.1 Removal

1. Remove the RANK from its station. Reference paragraph 7.4.17.1.
2. Remove the five Phillips-head screws (1) that secure the RANK top cover (2) to the base (3) and remove top cover.
3. Loosen two Phillips-head screws (4) holding power supply brackets (5) to keyboard housing, slide power supply (6) toward front and lift.
4. Detach keyboard dc cable (7) from power supply J1 (8).
5. Detach ac power lines (9) from load side of filter.
6. Remove power supply from housing.

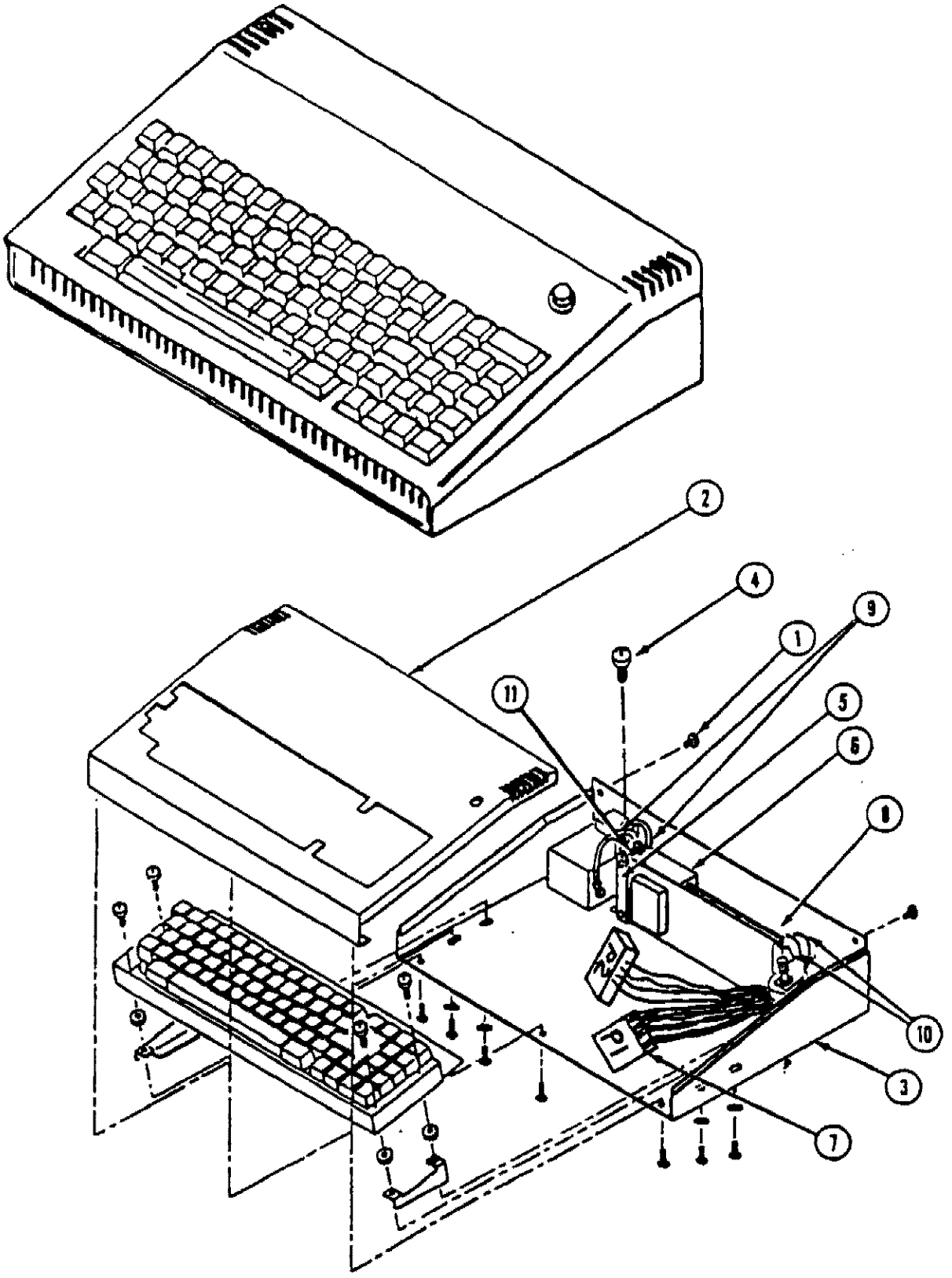


FIGURE 7-28. RANK (FA 10095/3) POWER SUPPLY REMOVAL AND REPLACEMENT

7. Detach black and red wires from E1 and E2 (10) (lamp intensity).

8. Remove the four (two each side) Phillips-head screws (11) that secure the mounting brackets (5) to the power supply, and remove brackets.

7.4.20.2 Replacement. Replacement of the RANK power supply is the reverse of the removal procedures with the following cautions:

1. Hook up black and white ac wires to the load side of the filter, opposite the same color wire on the line side.

2. Slide power supply as far to the rear as possible when mounting the power supply to the keyboard housing.

3. Adjust power supply position for optimum fit to avoid intensity control knob rubbing on top cover.

7.4.21 RANK (FA 10095/3) Spacebar and Lamp

Use paragraphs 7.4.21.1 and 7.4.21.2 along with figure 7-29 to remove and replace the RANK spacebar and lamp.

7.4.21.1 Removal

1. Remove the RANK from its station. Reference paragraph 7.4.17.1.

2. Remove the five Phillips-head screws (1) (three on bottom front edge and one at each top rear corner) that secure top cover to the base, and remove cover (2).

3. Carefully remove the metal space bar retaining clip (3), located along the front edge of space bar, by pulling the ends of the clip away from the retainers (4) at each end of the space bar.

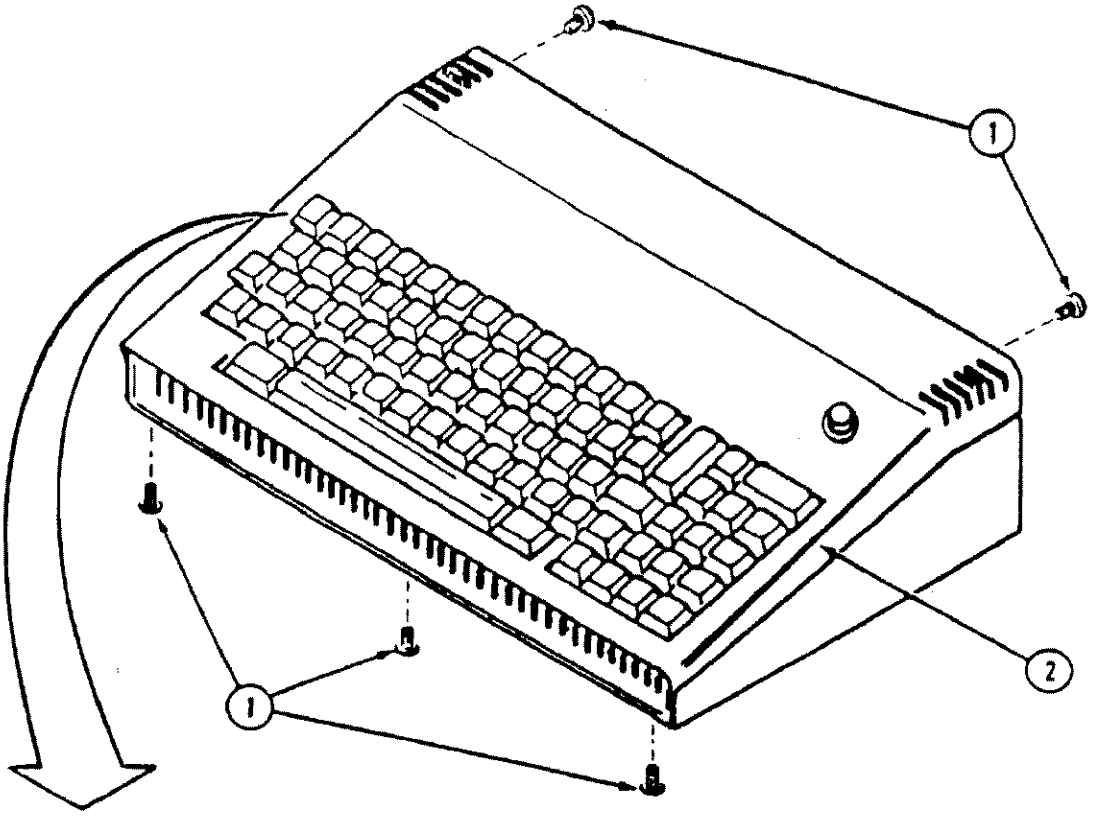
4. Pull space bar (5) straight up, and remove.

5. Push down on white plastic key shaft (6) until lamp can be grasped, and pull lamp straight up to remove.

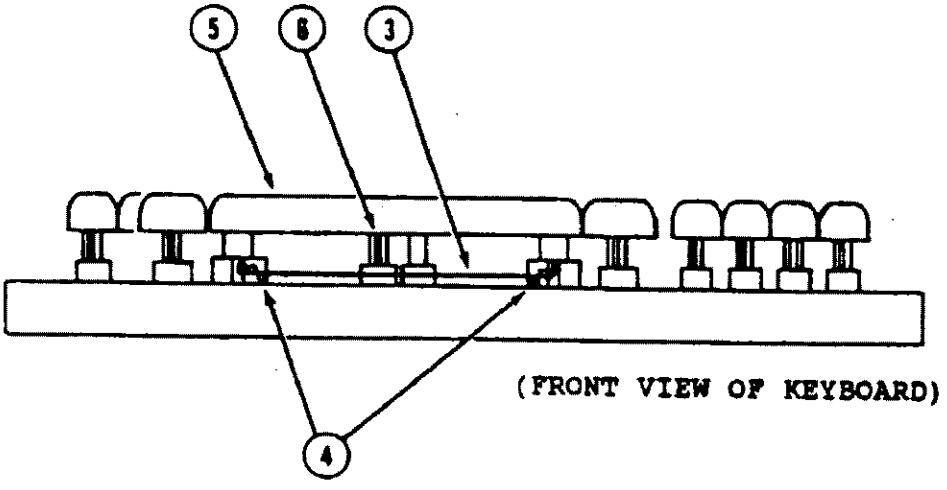
7.4.21.2 Replacement. Replacement of the RANK spacebar and lamp is the reverse of the removal procedure.

NOTE

When locking the spacebar retaining clip, the spacebar must be pressed down for clip ends to align with holes in spacebar metal end posts.



(KEYBOARD)



(FRONT VIEW OF KEYBOARD)

FIGURE 7-29. RANK (FA 10095/3) SPACEBAR AND LAMP REMOVAL AND REPLACEMENT

7.4.22 RFSP

Use paragraphs 7.4.22.1 and 7.4.22.2 along with figure 7-30 (FA 10095/2, figure 7-31 (FA 10095/11), or figure 7-32 (FA 10095/14) to remove and replace the RFSP.

7.4.22.1 Removal

1. Turn associated BC board power switch to the OFF position.
2. Turn RFSP power switch (1) to the OFF position.
3. Disconnect the ac power cord (2) from its source.
4. For FA 10095/2 and FA 10095/11 continue with step 5 of this paragraph. For FA 10095/14 continue with step 6.
5. Open RFSP top cover (3), open both tractor feed paper locks (4), and remove paper from RFSP (FA 10095/2 and FA 10095/11).
6. Open RFSP (FA 10095/14) right hand cover (3), lift printhead lever (4), and remove paper from RFSP (7). Disconnect data cable (5) from rear of unit, and remove RFSP (including power cord).

7.4.22.2 Replacement. Replacement is the reverse of the removal procedures.

7.4.23 CRT

Use paragraphs 7.4.23.1 and 7.4.23.2 along with figure 7-33 (FA 10095/4), figure 7-34 (FA 10095/12) or figure 7-34A (FA 10095/18) to remove and replace the CRT.

7.4.23.1 Removal

1. Turn associated BC board power switch to the OFF position.
2. Turn CRT power switch (1) to the OFF position.
3. Disconnect the ac power cord (2) from its source.
4. Disconnect data cable (3) from back of CRT (main port), and remove CRT (including power cord) from its station.

7.4.23.2 Replacement. Replacement is the reverse of the removal procedures.

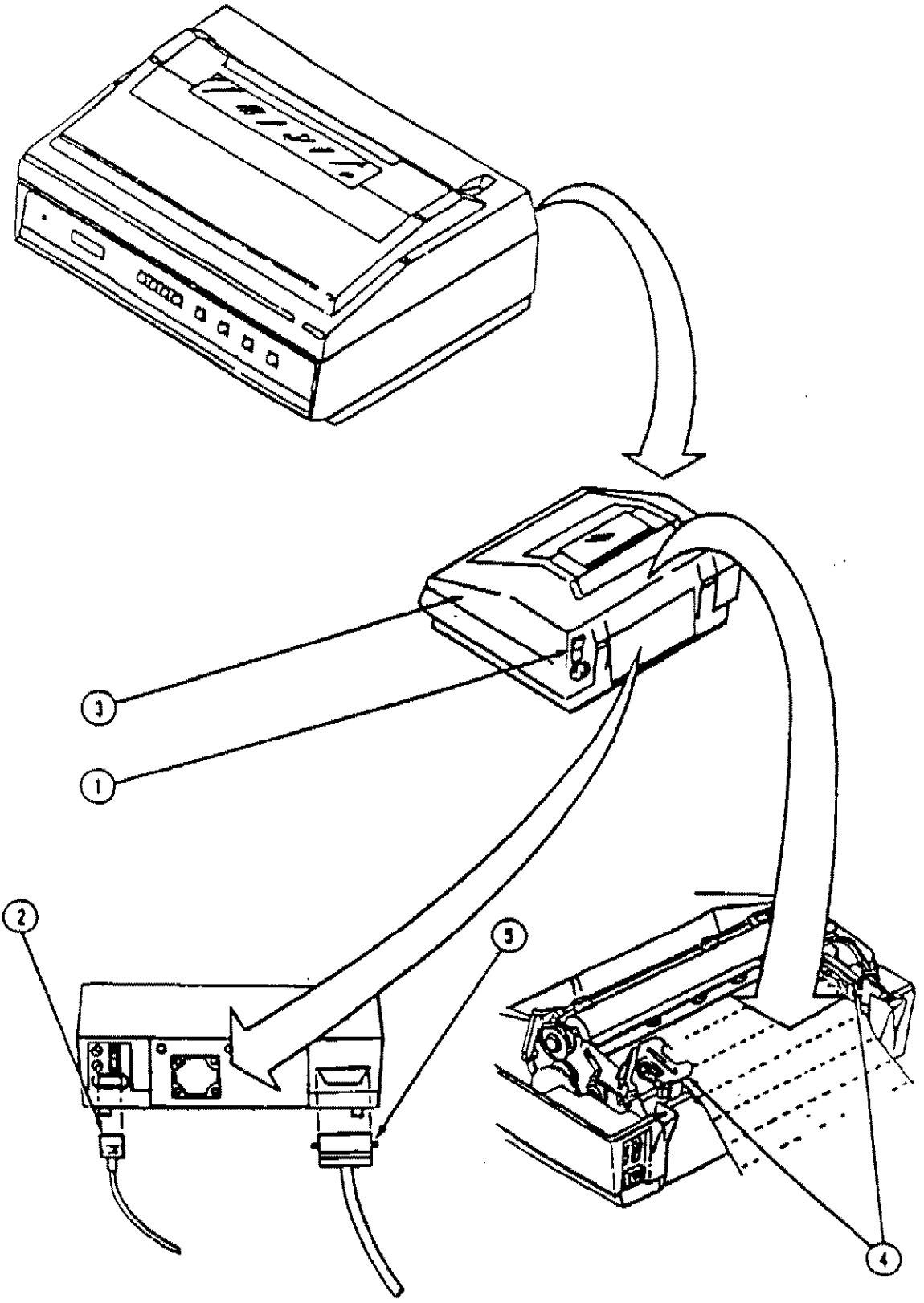


FIGURE 7-30. RFSP (FA 10095/2) REMOVAL AND REPLACEMENT

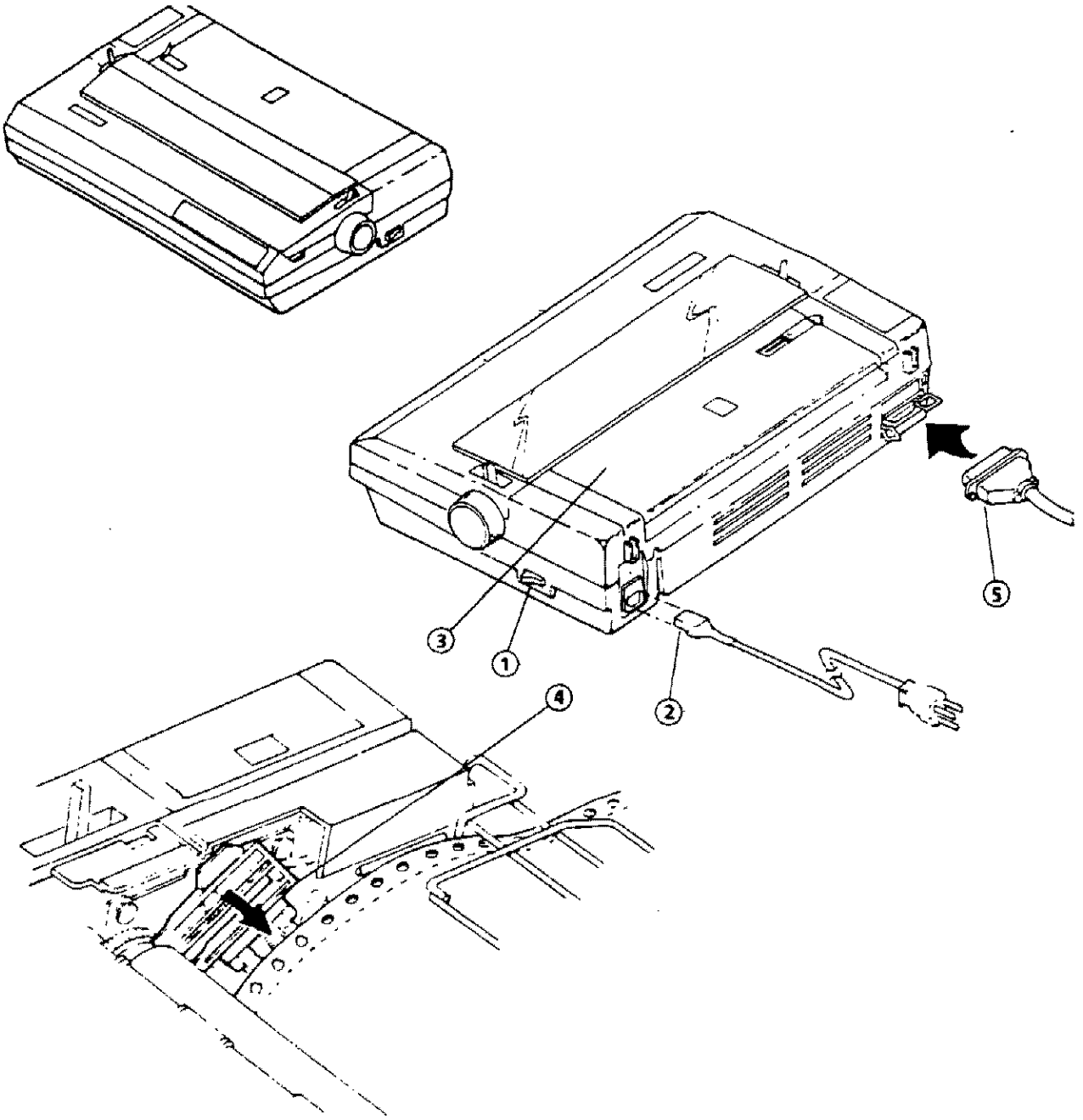


FIGURE 7-31. RFSP (FA 10095/11) REMOVAL AND REPLACEMENT

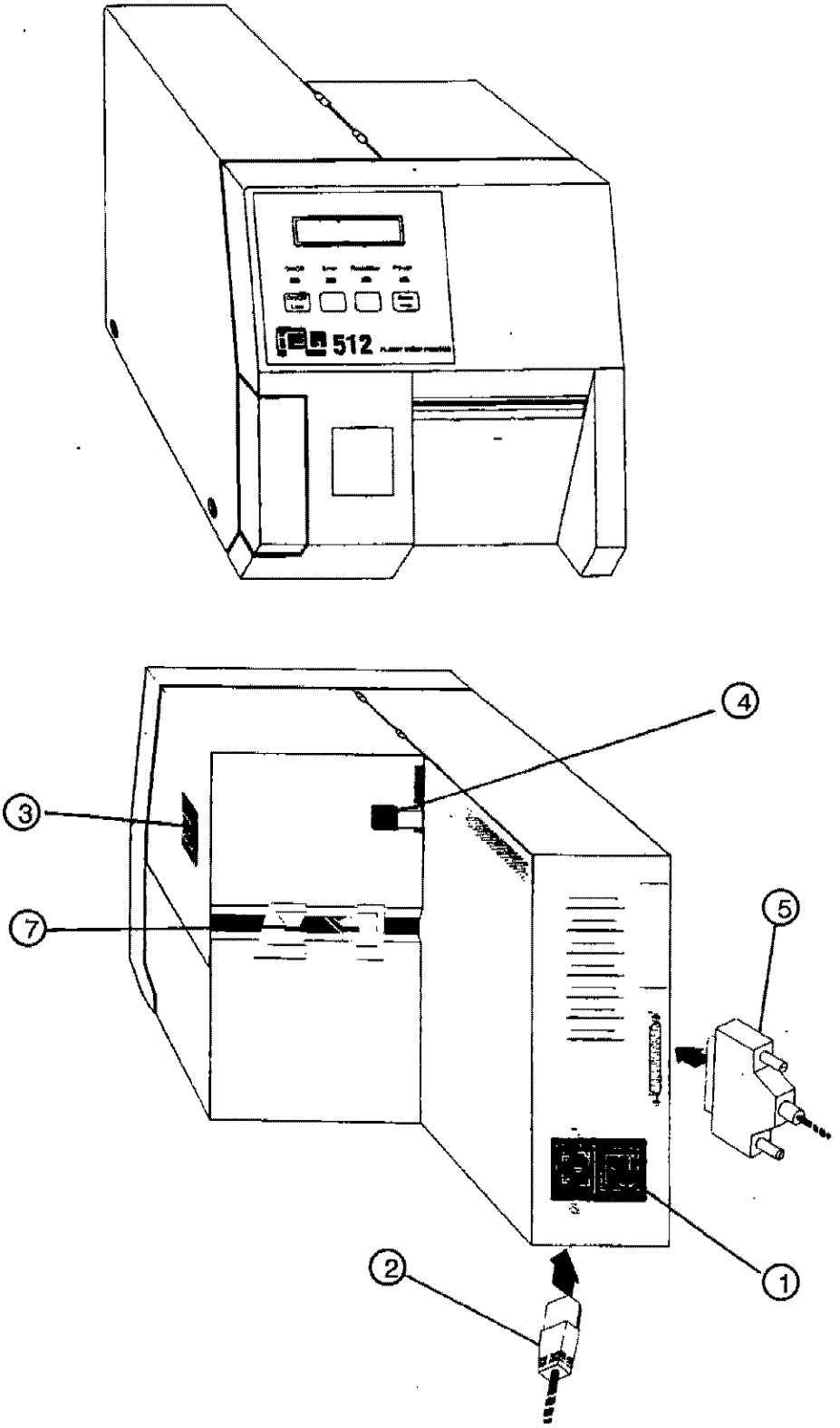


FIGURE 7-32. RFSP (FA 10095/14) REMOVAL AND REPLACEMENT

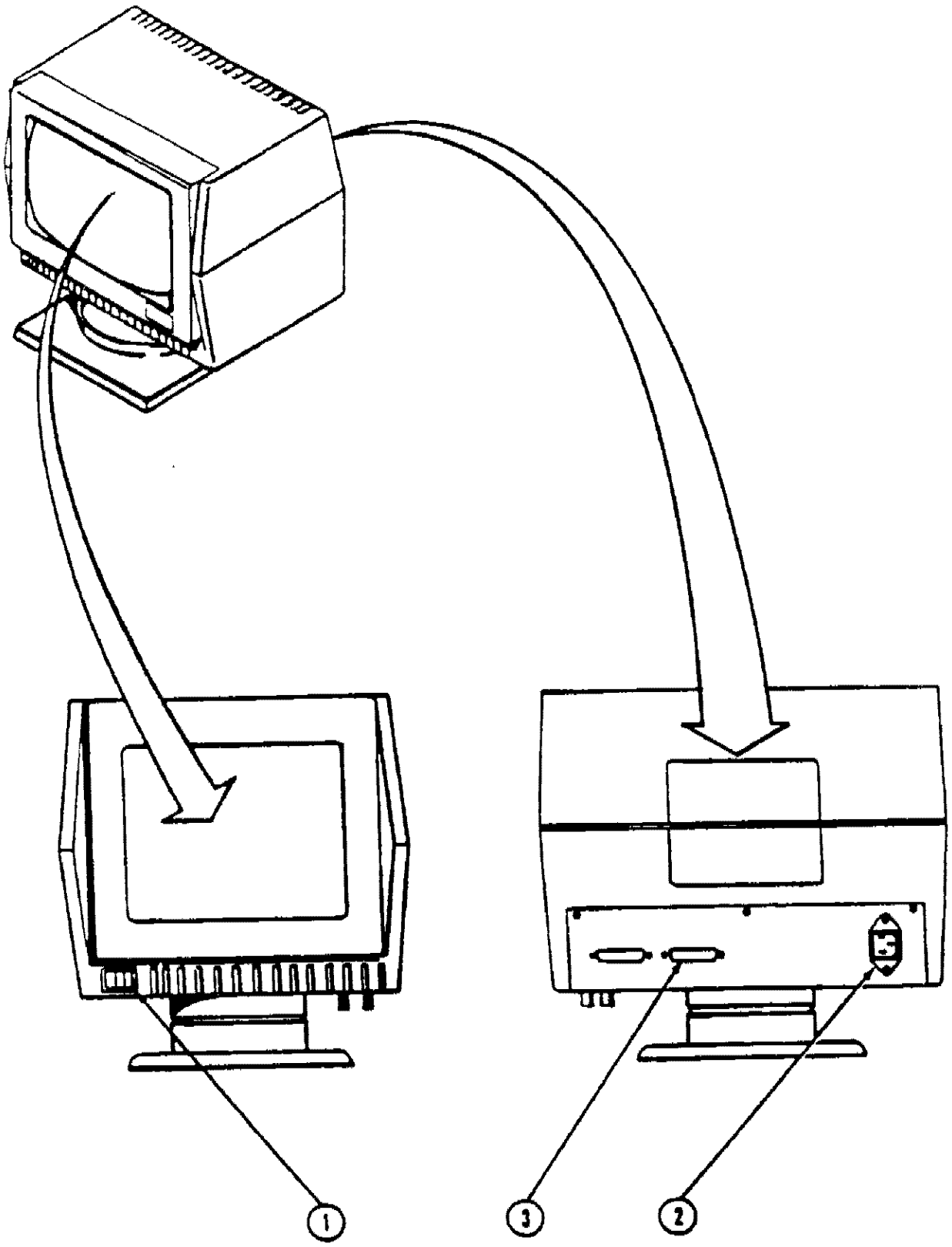


FIGURE 7-33. CRT (FA 10095/4) REMOVAL AND REPLACEMENT

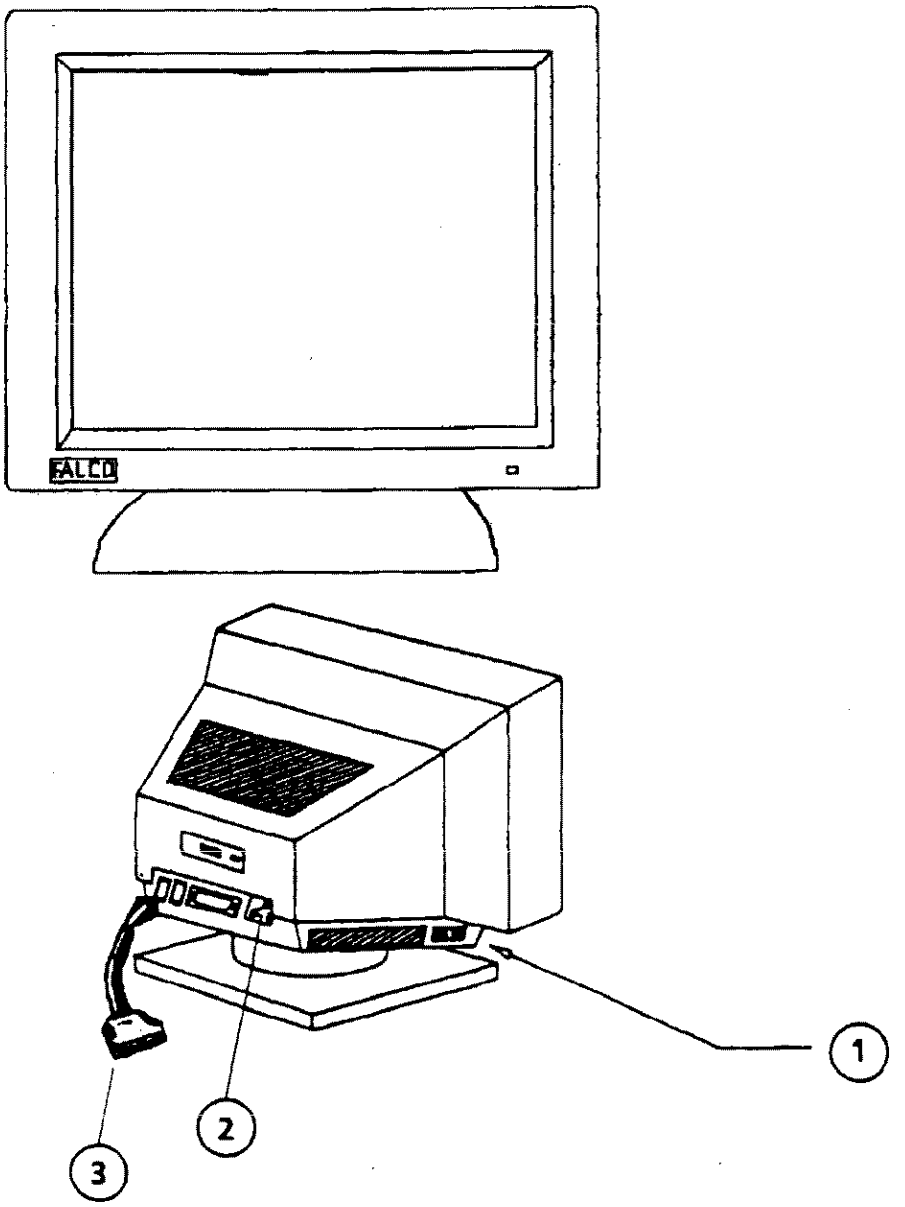


FIGURE 7-34. CRT (FA 10095/12) REMOVAL AND REPLACEMENT

7.4.24 RFSP (FA 10095/14 Printhead

Use paragraphs 7.4.24.1 and 7.4.24.2 along with figure 7-35 to remove and replace the thermal printhead for FA 10095/14.

7.4.24.1 Removal

1. Remove power cord from printer.
2. Open the right hand side door.
3. Disconnect the printhead (2) from the two connectors (3).
4. Push the printhead lever up and set the printhead to the maintenance position (see paragraph 6.4.7.2.1).

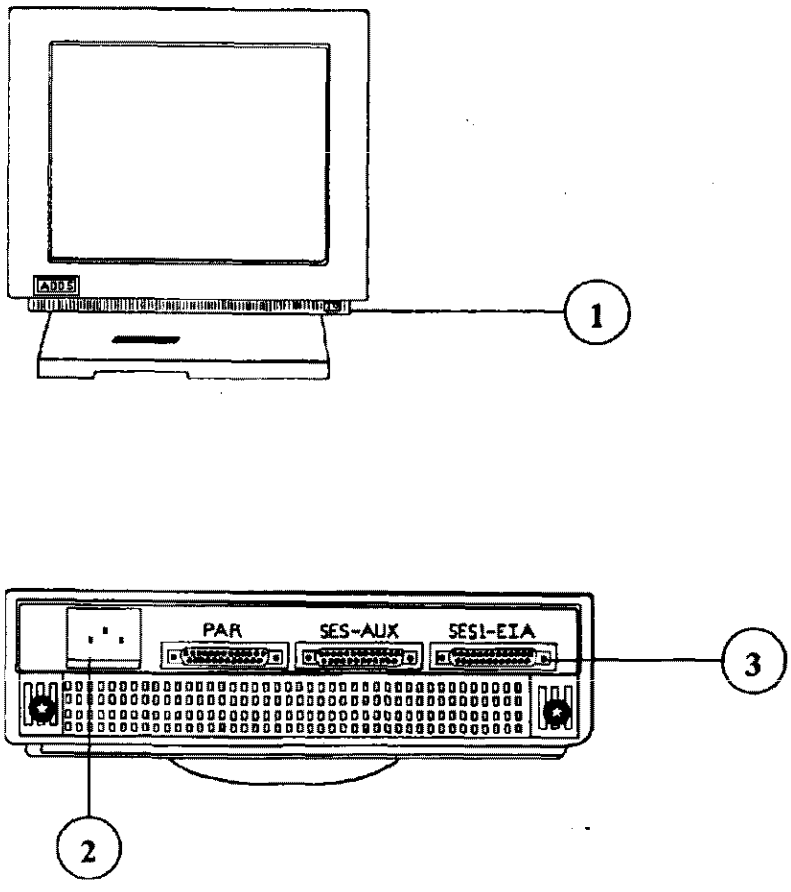


FIGURE7-34A. CRT (FA 10095/18) REMOVAL AND REPLACEMENT

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5. Remove the ground lead (4) using a 7-mm open-end wrench.

6. Remove the retaining ring (5) and pull the printhead (2) off its shaft.

CAUTION

Do not let printhead fly forward.

7. Remove the anti-static brush (1) from the printhead.

8. Retain ground screw (6) and retaining ring for replacement printhead.

9. Remove excess paper dust from interior of printer (refer to paragraph 6.4.7.2.3 for cleaning procedures).

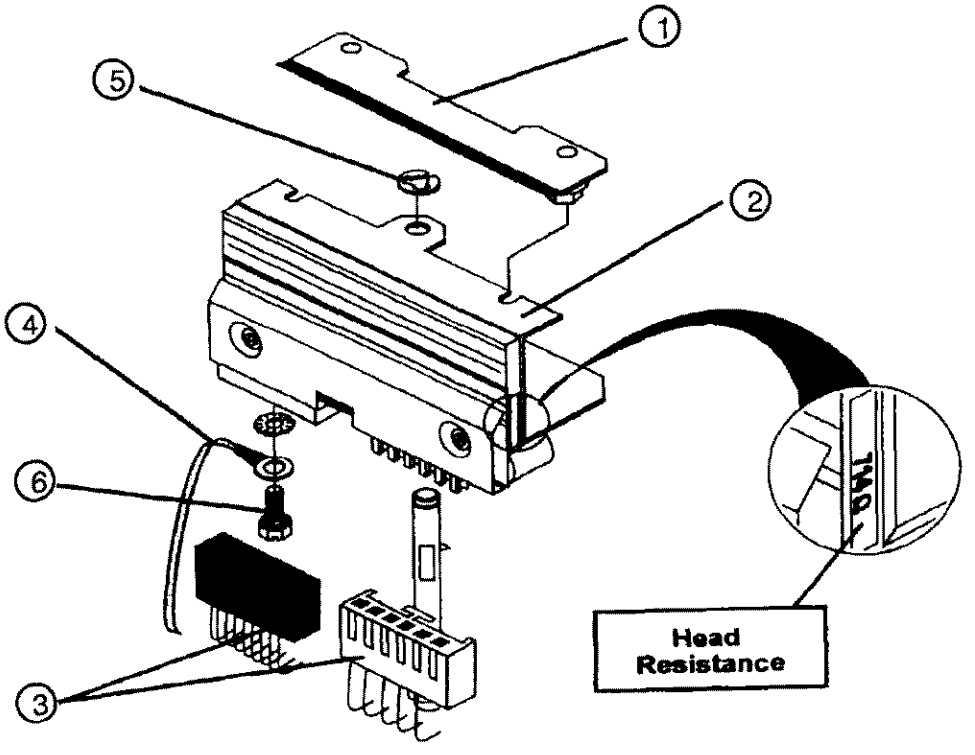

FIGURE 7-35. PRINTHEAD RESISTANCE

7.4.24.2 Replacement. Replacement is the reverse of the removal procedures. Whenever the printhead is changed, it is imperative to enter the resistance value of the new printhead. The resistance value is clearly marked on each printhead (see figure 7-31).

7.4.24.3 Adjustment

1. Power ON printer.

2. After printer finishes its self-test cycle, load paper stock. This procedure can not be accomplished without paper loaded into the printer.

3. Press the On/Off **Line** key to select the offline mode. Allow alarm' to stop.

4. Enter the configuration menu of the printer by pressing the front panel keys in the following order: **B — A — Blank Strip — B** (six times). Refer to figure 7-36 for layout of front panel keys.

5. After a short delay the display will read **PASSWORD? 00000.** Press the **On/Off Line** key.

6. The front panel will read **EMULATION PARAMETERS.** Press the **A** key 4 times.

7. The front panel will read **HARDWARE PARAMETERS.** Press the **B** key once.

8. The front panel will read **HEAD RESISTANCE** XXX.. Enter the correct resistance value for the printhead. The resistance value is clearly marked on the printhead (see figure 7-31). Use the **Blank Strip** key to change the value of the digit highlighted by the blinking cursor. Use the **A** key to move the cursor to the next digit.

9. After setting the correct resistance, press the **On/Off Line** key twice. The front panel will read **VALIDATION? NO.**

10. Press the **Blank Strip** key. The front panel will read **VALIDATION? PERMANENT.**

11. Press the **On/Off Line** key. After a short delay the front panel will read **IER 512 OFF LINE.**

12. Test the print quality by printing the printhead adjustment test document. Press the front panel keys in the following order:. **B — A — Blank Strip — B** (4 times).

13. If this document shows a weak print contrast, the following adjustments need to be performed.

14. Open right hand side door.

15. Push printhead lever up and set the printhead to the maintenance position (see paragraph 6.4.7.2.1).

16. Hold shaft (item 2, figure 7-37) using a 5.5-mm open-end wrench 1.

17. Use a 10-mm open-end wrench 3 to rotate nut 4 clockwise or counterclockwise one quarter turn.

18. Print again the printhead adjustment test document. See step 12 above of this paragraph.

19. If the print contrast has improved, continue turning nut 4 in the same direction one quarter turn.

20. If the print contrast is weaker, turn nut 4 one quarter turn in the opposite direction.

21. Repeat above adjustment until the best possible contrast has been obtained.

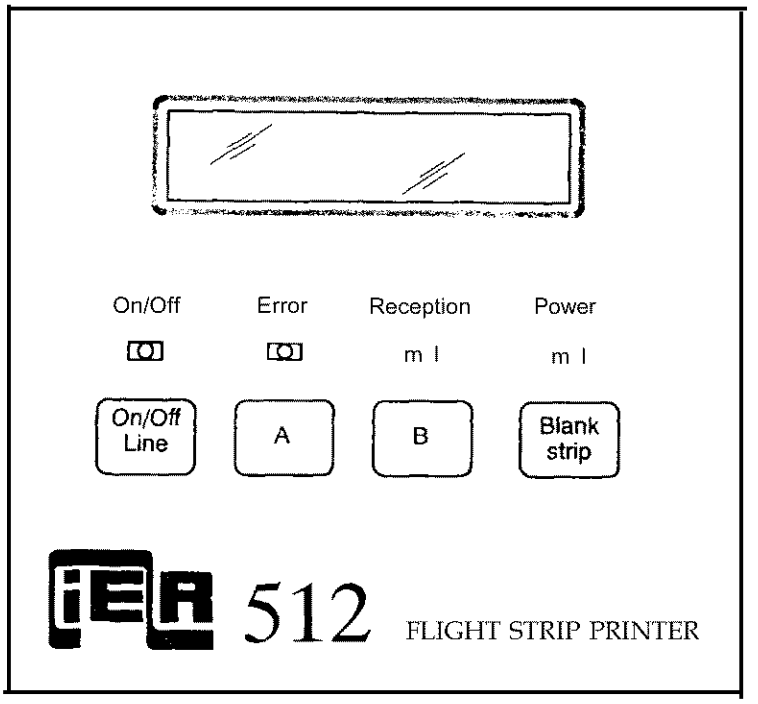

FIGURE 7-36. LAYOUT OF FRONT PANEL KEYS

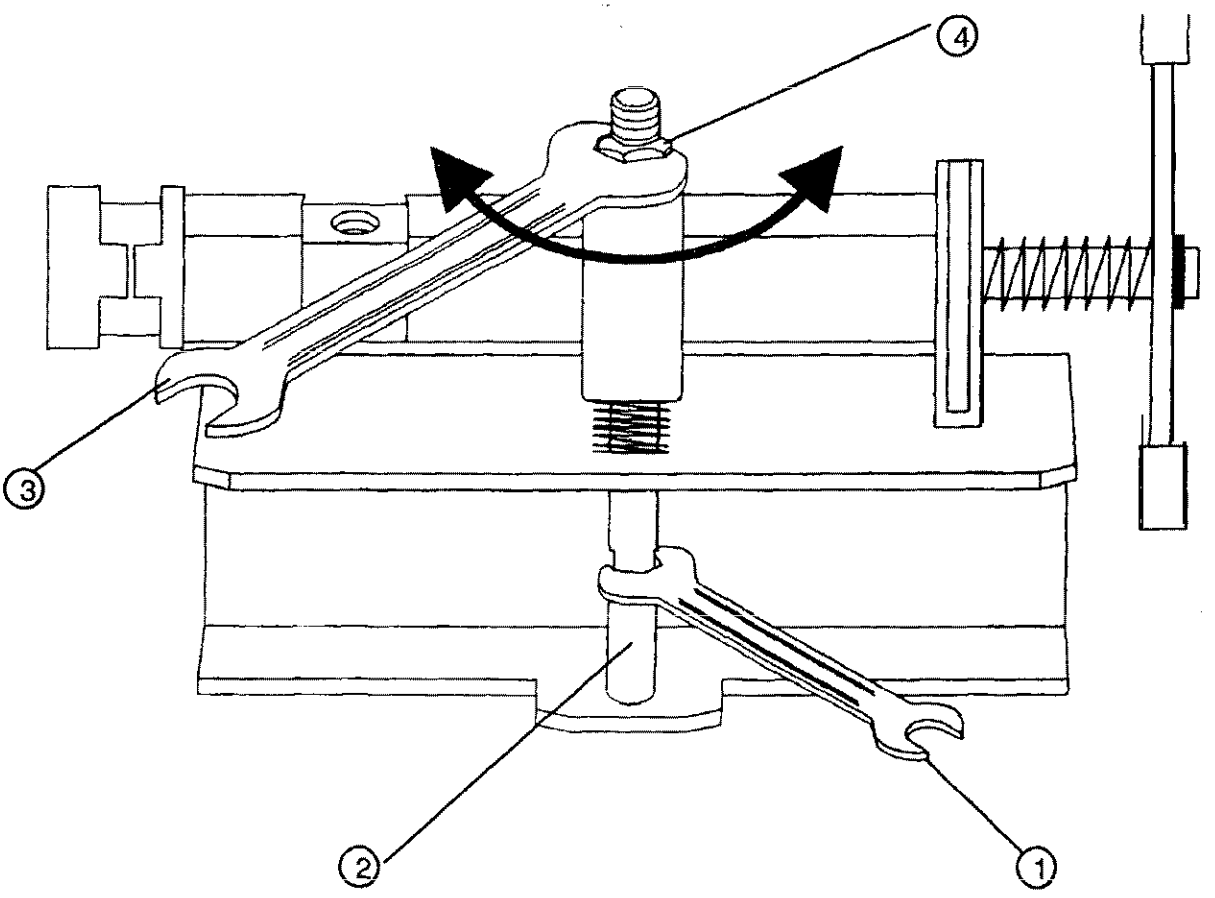

FIGURE 7-37. PRINT CONTRAST ADJUSTMENT

7.4.25 RFSP (FA 10095/14) Fuse

Use paragraphs 7.4.25.1 and 7.4.25.2 to remove and replace the fuse for FA 10095/14.

7.4.25.1 Removal

1. Remove power cord from printer.
2. Remove left hand side cover.
3. Remove plastic protection plate located near rear of printer.
4. Remove fuse located in the lower left hand corner of the board mounted near rear of printer.

7.4.25.2 Replacement. Replacement is the reverse of the removal procedure.

7.4.26 RFSP (FA 10095/14) Platen Roller

Use paragraphs 7.4.26.1 and 7.4.26.2 to remove and replace the platen roller for FA 10095/14.

7.4.26.1 Removal

NOTE

All instructions are in reference to the technician facing the front of the printer.

1. Remove left side cover by removing the two screws on the left side, one in the rear, and loosening the nut inside of the printer above the printhead. See figure 6-12.
2. Remove the right side cover by removing the three retaining screws under the printer.
3. Remove all connectors from the motherboard located on the left side of the printer. There are seven connectors in all and be sure to make note of where all are connected.
4. Remove the four retaining nuts at the four corners of the motherboard and remove it from the mounting posts.
5. Remove the retaining post from the upper left-hand corner of the motherboard mounting plate.
6. Remove the three retaining screws at the bottom of the mounting plate. Note that a 5.5-mm wrench will have to be used to hold the nut under the printer while the screw is turned from the top.
7. Move the mounting plate away from the printer to allow enough room for the platen roller to slide out.
8. On right side of the printer, remove the retaining clip and bearing collar from the end of the platen roller.
9. Note the drive belt tension before removal of the belt.
10. Loosen the top mounting nut of the drive motor (1) (figure 7-38) and slide the motor forward to relieve the tension on the drive belt.

11. Remove the drive belt and then remove the platen roller.
12. Remove the bearing from the right mounting hole (2).
13. Remove the retaining clip, bearing collar, and bearing from the new platen roller assembly. Do not remove the gear assembly.

7.4.26.2 Replacement

1. Insert the new bearing into the right mounting hole.
2. Install the new platen roller.
3. Install the bearing collar and retaining clip.
4. Install the drive belt and push back on the drive motor to apply tension. Adjust the tension to what was noted in step 9 of paragraph 7.4.26.1. Beware that too much tension will cause the motor to bind and too little will cause the belt to slip. When the desired tension is found, tighten drive motor mounting nut.
5. Reassemble printer in reverse order.
6. Power up, load paper, and print test messages as needed to verify proper operation of the printer.

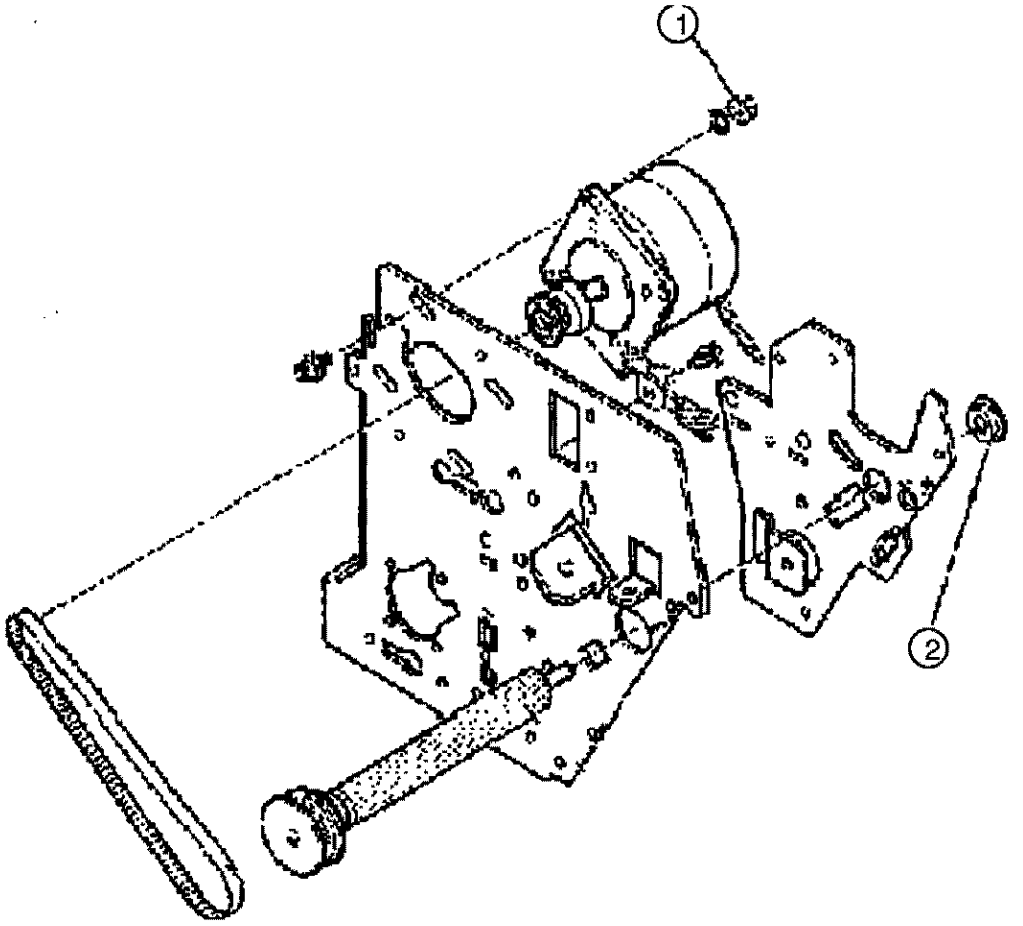

FIGURE 7-38. RFSP (FA 10095/14) PLATEN ROLLER REMOVAL

7.4.27 RFSP (FA 10095/14) Cutter Guide

Use paragraphs 7.4.22.1 and 7.4.22.2 along with figure 7-39 to remove and replace the cutter guide in RFSP (FA 10095/14).

7.4.27.1 Removal

1. Remove the printer from service.
2. Lift the upper right-hand cover of the printer with the technician facing the printer and power removed.
3. Remove the lower right-hand cover by removing the three screws under the printer that secure the edge of the cover.
4. Remove the two screws securing the plastic cutter guide ① but do not remove the guide yet. The plastic cutter guide ① is located toward the front of the printer, made of white plastic, and held in place by two screws.
5. Apply pressure to the front of the cutter blade ② and remove the old guide. It is important to continue applying pressure until the new guide is in place. This is needed so that the blade does not disengage from the cutter gear that moves the blade up to cut.

7.4.27.2 Replacement

1. Insert the new guide.
2. Secure the new guide with the two guide screws and reassemble the printer in reverse order.
3. Power up, load paper, and print test messages as needed to verify proper cutting of the test messages.

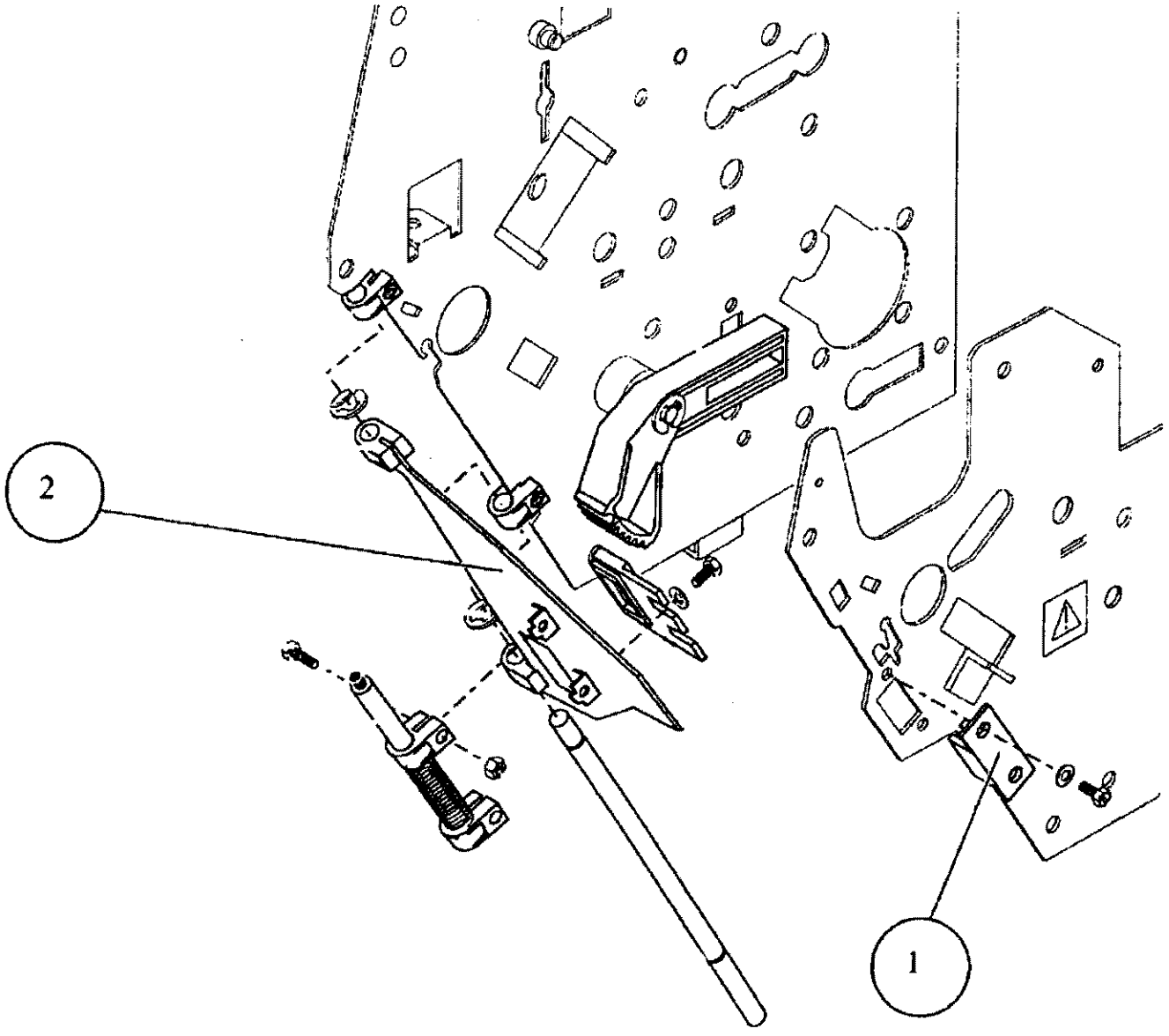

FIGURE 7-39. RFSP (FA 10095/14) CUTTER GUIDE REMOVAL AND REPLACEMENT

8.0 PARTS LIST

8.1 INTRODUCTION

This section contains descriptive and source data necessary for procurement of replaceable parts used in the FDIO system. It contains a parts list table and a list of manufacturers.

8.2 PARTS LIST TABLE

The parts list table contains the six columnar designations described below, preceded by an item number. The item number indicates sequence in this list and is used for reference purposes only.

Column Designations	Description
Item Number	Indicates sequence of item in parts list
Reference Designation	Reference Designation in accordance with ANSI Y32.16.
Indenture Letter	Indenture letter for the system, set, group, unit, assembly, sub-assembly, or part as prescribed in Specification FAA-G-1210.
Part Name and Description	Item name as prescribed in Specification FAA-G-1210.
Manufacturer's Code Number	Five-digit code assigned to the manufacturer of the part.
Manufacturer's Part Number	Catalog number, type number, or drawing number by which Wespercorp (FSG) identifies the part.
Notes	Left blank for FAA field use.

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0001	1	A	CCU/CCU CABINET ASSY	65519	F64000623	
0002	1A1 (1A3)	B	MULTIBUS ASSY, CCU CPU W/TERM BOARD	65519	F64000789-001	
0003		C	CHASSIS MULTIBUS MODIFIED	65519	F82000514	
0004	1A1A2A1	C	INTEL SBC 88/45 ASSY, MODIFIED	65519	F60002607	
0005		D	INTEL SBC 88/45 PWB ASSEMBLY	65519	F52000551	
0006		D	ASSY CABLE CONFIG JMPR 3 POS	65519	F62002498	
0007		E	CONN MINI RECEP BERG 47745-000	95871	F23001860	
0008		E	WIRE 28AWG UL 1007 9928-13	09047	F28001246	
0009		E	SLVG FIT105-1 1/16 BLACK	09047	F28001170	
0010		D	CA ASSY CONF JPR 2POS 4.5	65519	F62002290-001	
0011		E	CONNECTOR — Same as Item 0007			
0012		E	WIRE — Same as Item 0008			
0013		E	SLVG BLACK — Same as Item 0009			
0014		D	CONN 2 POS JMPR BERG 6547	95871	F23001597	
0015		D	CA ASSY CONF JPR 2POS 1.5	65519	F62002290-002	
0016		E	CONN — Same as Item 0007			
0017		E	WIRE — Same as Item 0008			
0018		E	SLVG — Same as Item 0009			
0019	1A1A2A2	C	ASSY UTILITY BOARD ASSEMBLY ENH	65519	F60003118	
0020	U1, U8	D	IC 7406J5406J HEX INV CER	81349	F17100002	
0021	U27, U38, U39	D	IC 74LS32J/54LS32J	01295	F17006735	
0022	U18, U47	D	IC 74LS11J/54LS11J TP 3-IN AND	01295	F17006727	
0023	TB1	D	TERMINAL BLOCK TRW 2-17-2	20806	F26100000	
0024	U4, U64	D	IC 7407J HEX BUFFER	01295	F17002114	
0025	U10	D	IC 74LS86J/54LS86J QD 2-IN XOR	01295	F17006750	
0026	U51	D	IC 74LS161J/54LS161J CNTR 4BIT	01295	F17006289	
0027	U59	D	IC 74LS367J/54LS367J H BFR 3ST	01295	F17006842	
0028	U32	D	IC 8031AH CERAMIC 8BIT MICRO	34649	F17006388	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0029	U16, U9	D	IC 74LS244J/54LS244J OCTA	01295	F17006826	
0030	U25, U33	D	IC 74LS374J/54LS374J OTL D FLP	01295	F17006875	
0031	U23	D	IC 74LS373J/54LS373J OCT D F/F	01295	F17006297	
0032	U35, U43, U50	D	IC 74LS74/54LS74J DUAL D FLIP	01295	F17006743	
0033	U55	D	IC 74LS109J/54LS109J DL JK FLP	01295	F17006768	
0034	U54	D	IC 74HC4020J/54HC4020J CNTR	27014	F17006305	
0035	U60, U61	D	IC 74LS240J/54LS240J OCTAL BFR	01295	F17006800	
0036	U62	D	IC D8287 OCTAL XCVR CERAMIC	34649	F17006958	
0037	U46, U63	D	IC 74LS138J/54LS138J DCDR/MUX	01295	F17006263	
0038	U3, U17, U26, U34 U41, U53	D	IC HM6264LP-12 CERAMIC CMOS RAM	81349	F17006404	
0039	U40, U45, U48, U52	D	IC 74LS08J/54LS08J QD 2-IN AND	01295	F17006719	
0040	U36, U37	D	IC 8255A-5 PROG PER INT CERAM	04649	F17006966	
0041	U6, U12, U20-U22, U30	D	IC 75124J TRIP IBM RCVR CERAM	01295	F17006891	
0042	U28, U31	D	IC 74LS280J/54LS280J PRTY COMP	01295	F17006834	
0043	U5, U7, U11, U13, U14, U19, U29, U44	D	IC 75123J DUAL IBM XMTR CERAM	01295	F17006883	
0044	OSC1	D	OSC 11.059MHZ M-TRON	10144	F22000806	
0045	U42, U56, U57	D	IC 74LS04J/54LS04J HEX INVERT	01295	F17006693	
0046	R10	D	RES, 470, 1/4 W, 5%	81349	F14000103	
0047	R3, R9, R11	D	RES 10 K 5% 1/4 W	81349	F14000939	
0048	R8	D	RES 8.2 K 5% 1/4 W	81349	F14000954	
0049	R1, R2, R4, R5, R6 R15	D	RES 1 K OHM 1/4 W 5%	81349	F14001002	
0050	U58	D	IC.74LS20J/54LS20J — FC	81349	F17100005	
0051	U2	D	IC 74LS241	81349	F17002098	
0052	R7, R12-R14,	D	RES 4.7 K 5% 1/4 W R16-R18	81349	F14000947	
0053	C22, C32, C33	D	CAP 10UF 20 V 150D106X9020	81349	F15001282	
0054	DS4-DS8	D	LED 555-2303 DIALCO GREEN	05200	F21000161	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0055	C1-C21, C23-C31, C34	D	CAP .1UF 50 V 923CZ5U104M0	81349	F15002686	
0056	DS1-DS3	D	LED 555-2403 DIALCO YELLOW	05200	F21100000	
0057	W1-W6	D	CONN — Same as Item 0014			
0058	U15	D	IC Z8530 SERIAL COMM CONT	81349	F17005877	
0059		D	PWB/PWM UTILITY BD ENH	65519	F76001619	
0060	W1-W6	D	CONN 1X2 BERG STIK	95871	F23001696	
0061		D	SCHEM UTILITY BD ENH	65519	F75001545	
0062		D	CARD EJTR SCANBE S-200WH	06401	F49000607	
0063	U24	D	IC SOC 24 POS RN	06776	F23001142	
0064	U3, U17, U26, U34, U53	D	IC SOC 28 POS RN	06776	F23001159	
0065	U15, U32, U36, U37	D	IC SOC 40 POS RN	06776	F23001167	
0066	RN1, RN2, RN3	D	RES PACK 4.7 K CTS750-101-R4.7K	57921	F14000962	
0067	CR1	D	DIODE IN5817 MOTOROLA	04713	F11100000	
0068	U49	D	IC. 74LS21J/54LS21J — FC	81349	F17100004	
0069	1A1A2A3	C	ASSY FDIO TERMINATOR BOARD	65519	F60002664	
0070	RP1-RP7	D	RESP 5-RES	91673	F14000996	
0071		D	PWB/PWM FDIO TERMINATOR BOARD	65519	F76001692	
0072		D	SCHEM FDIO TERMINATOR BOARD	65519	F75001602	
0073	1A1A1	C	MULTIBUS FRONT PANEL ASSEMBLY	65519	F64000847	
0074		D	PANEL, MULTIBUS CARD CAGE	65519	F82000712	
0075		D	BRACKET-PANEL (R)	65519	F82000720-001	
0076		D	BRACKET-PANEL (L)	65519	F82000720-002	
0077		D	PIVOT PLATE, MULTIBUS PANEL	65519	F82000738	
0078		D	RETAINER 82-32-101-20 SOUTHCO	94222	F42000976	
0079	1A1A1A2	D	PWB ASSY — FNT PNL CONT BD	65519	F60002466	
0080		E	CONN — Same as Item 0014			
0081	U101	E	IC- Same as Item 0024			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0082	J102	E	CONN 14PIN BERG 66207-011	95871	F23001225	
0083	J101	E	CONN 50PIN BERG 66207-026	95871	F23001217	
0084	W1, W2, W3, W4	E	CONN — Same as Item 0060			
0085	C101	E	CAPACITOR 22MF 15 V 162D22X9015EE2	56289	F15001274	
0086		E	SPACER AMATOM 9224A115-17	06540	F42000471	
0087	R101	E	POT 10 K SNGL TURN 3386P BOURNS	57921	F14000095	
0088		E	KEYPAD GRAYHILL 89YY3620B-502	81073	F29000643	
0089	RN1	E	RES 4.7 K SIP CTS 750-61-R4.7K	06470	F14000889	
0090		E	NUT, HEX 4-40	10516	F46000139	
0091		E	PWB/PWM — FNT PNL CONT BD	65519	F76001536	
0092		E	FNT PNL CONT PNL SCHEMATIC DIAG	65519	F75001461	
0093		D	KEPNUT 4-40	30829	F46000089	
0094		D	SCREW, PAN HD 4-40X3/8 STEEL	01608	F47000302	
0095		D	WASHER, AMATOM 2704-19993-N126	06540	F48000129	
0096		D	CABLE ASSEMBLY, DISPLAY	65519	F62001946	
0097	P1, P2	E	CONN 14 PIN SOCKET — FC	95871	F23001944	
0098		E	CABLE 28AWG STRAND 3M 3365/14	53387	F28000875	
0099		E	WRAP-IT RICHCO WIT-18R	06915	F42000992	
0100		E	MARKER PLATE, PANDUIT MP-250	06383	F49000623	
0101		D	CABLE ASSY, 88/45 BD/FNT PANEL	65519	F62001888	
0102		E	CONN 50POS BERG 66900-350	95871	F23001514	
0103	P2	E	CONN EDGE 50POS BERG 66317-050	95871	F23001498	
0104		E	CABLE 28 AWG STRAND 3M 3365/50	53387	F23001048	
0105		E	MARKER — Same as Item 0100			
0106		E	WRAP-IT — Same as Item 0099			
0107	1A1A1ALM1	D	SONALERT PNL MNT SNP2 MALLORY	37942	F29000650	
0108		D	ASSY FNT PNL DISPLAY	65519	F60002680	
0109	1A1A1A1	E	H2572/LCD MODULE	52531	F21000179	
0110		E	CONN 2X7 MALE PIN — FC	95871	F23007917	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0111		D	SOUTHCO FASTNER 82-13-200-16	94222	F42000984	
0112		D	SPACER AMATOM 9225A115-17	06540	F42000463	
0113		D	SPACER — Same as Item 0086			
0114		D	WASHER, FLAT NO. 4	01608	F48000160	
0115		D	CABLE ASSY SONALERT FRONT	65519	F62002456	
0116		E	CONTACT BERG 48254-00/482	95871	F23001746	
0117		E	CONN 2 POS BERG 65039-035	95871	F23001894	
0118		E	WIRE 20AWG UL 1007 BLACK	09047	F28000941	
0119		E	WIRE 20AWG UL 1007 RED	09047	F28000966	
0120		D	NUT — Same as Item 0090			
0121		D	WASHER NYLON HH SMITH	83330	F48000178	
0122		D	LOCTITE THREADLOCKER	05972	F49001027	
0123		D	TAB FASTON .250X.032 — FC	05972	F26001669	
0124		D	BRACKET, MULTIBUS CARD CAGE "L"	65519	F82000647	
0125		D	BRACKET, MULTIBUS CARD CAGE "R"	65519	F82000654	
0126		D	SCREW SLOTTED HEX HD 6-32X1/4	01608	F47004171	
0127		D	SPACER 3/8 IN. DLCBS-CN RICHCO	06915	F42000398	
0128		D	SCREW 4-40X1/2 PHPH MS51957-14	30829	F47000252	
0129		D	WASHER — Same as Item 0095			
0130	1A1A2A2, U24	C	PROM SET, UTILITY BD	65519	F18000786	
0131		D	PROM UTILITY BD	65519	F17017096	
0132		E	IC D2732A EPROM 4KX8 CERAMIC	34649	F17006933	
0133		E	LABEL PROM UTILITY FSE	65519	F74000373-013	
0134		E	PROGRAM UTIL BD PROM REV 1.1	65519	F68000496	
0135	1A1A2A1 U49, U50, U89, U90	C	PROM SET CCU-CPU	65519	F18000737	
0136	U49	D	PROM CCU-1	65519	F17017005	
0137		E	IC, EPROM 27128	34649	F17002106	
0138		E	LABEL PROM CCU-1	65519	F74000373-001	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0139		E	PROGRAM CCU-1 REV 3.3	65519	F68000355	
0140	U50	D	PROM CCU-2	65519	F17017013	
0141		E	IC — Same as Item 0137			
0142		E	LABEL PROM CCU-2	65519	F74000373-002	
0143		E	PROGRAM CCU-2 REV 3.3	65519	F68000363	
0144	U89	D	PROM CCU-3	65519	F17017021	
0145		E	IC — Same as Item 0137			
0146		E	LABEL PROM CCU-3	65519	F74000373-003	
0147		E	PROGRAM CCU-3	65519	F68000371	
0148	U90	D	PROM CCU-4	65519	F17007139	
0149		E	IC — Same as Item 0137			
0150		E	LABEL PROM CCU-4	65519	F74000373-004	
0151		E	PROGRAM CCU-4 REV 3.3	65519	F68000538	
0152	1A1A2A1A1	C	PWB ASSY FDIO FP I/F BOARD	65519	F60002292	
0153	U2	D	IC — Same as Item 0040			
0154	U5	D	IC, 8279-5 PROM KEY/DISPL CERAMIC	34649	F17006982	
0155	U4	D	IC — Same as Item 0032			
0156	U1	D	IC, NMC9817 2K x 8 E SQUARED	27014	F17007022	
0157	U3	D	IC, 74LS00J/54LS00J QUAD NAND	01295	F17006685	
0158	R1-R3	D	RES — Same as Item 0052			
0159	C2-C6	D	CAP — Same as Item 0055			
0160	C1	D	CAP — Same as Item 0085			
0161	J2	D	CONNECTOR 36 POS LMP01VH18A01	05574	F23008105	
0162		D	PWM/PWB — FP INTERFACE BOARD	65519	F76001502	
0163		D	SCHEM — FP INTERFACE BOARD FDIO	65519	F75001438	
0164		D	IC — Same as Item 0064			
0165		C	CA ASSY CONF JPR 2POS 1.5	65519	F62002290-002	
0166		D	CONN — Same as Item 0007			
0167		D	WIRE — Same as Item 0008			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0168		D	SLVG — Same as Item 0009			
0169		C	SCREW, PAN HD, 4-40X.25 — FC	01608	F47000492	
0170		C	KEPNUT — Same as Item 0093			
0171		C	NAMEPLATE, CCU	65519	F74000555	
0172		C	KEPNUT 6-32 502-060800-01	30829	F46000097	
0173		C	CABLE ASSY, MULTIBUS FR PN	65519	F62002613	
0174		D	QDLG FEM 22-18AWG .25X.03	83330	F26001677	
0175		D	WIRE — Same as Item 0118			
0176		D	RING LUG 22-18AWG NO.6	83330	F26001685	
0177		D	MARKER PLATE — Same as Item 0100			
0178		D	WRAP-IT — Same as Item 0099			
0179		C	LOCTITE — Same as Item 0122			
0180	1A2 (1A4)	B	MULTIBUS ASSY — CCU CPU W/O TERM Same as Items 0003 — 0068, 0073 — 0179	65519	F64000789-002	
0181			ITEM DELETED 6/4/86			
0182			ITEM DELETED 6/4/86			
0183			ITEM DELETED 6/4/86			
0184	1A5 — A8	B	BUS CONNECTOR TOP ASSY	65519	F64000540	
0185		C	WASHER, NYLON H.H.SMITH NO. 2670	83330	F48000152	
	A1 — A16	C	PWB ASSY BUS CONN BD ENH		F60002540	

NOTE

FOR BUS CONNECTOR BOARD PARTS BREAKDOWN REFER TO ITEMS 1104 THROUGH 1143.

0186	A17	C	PWB ASSY BUS CONN BK PLANE	65519	F60002557	
0187	U1, U2	D	PWB ASSY, LAN TERM ADPTR	65519	F60008672	
0188		E	PWM/PWB, LAN TERM ADPTR	65519	F76001684	
0189	U1, U2	E	IC 75157J CERAMIC DUAL LN RCVR	01295	F17006313	
0190		E	SCO PINS 8PIN AUGPT708AG1	94222	F23008220	
0191	R1, R3, R4, R6	E	RES — Same as Item 0049			
0192	R2, R5	E	RES 120 OHM 1/4 W, RC07GF1	81349	F14001390	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0193		D	SCHEM BUS CONN BKPLN-ENH	65519	F75001560	
0194	U3-U34	D	IC 74HC157J/53HC157J	81349	F17005992	
0195	U35, U36	D	IC 75158JG CERAM DUAL LN	07263	F17006321	
0196	R2, R4	D	RES 100 OHM 1/4 W 5% RC07GF101J	81349	F14000855	
0197	R5-R36	D	RES 22K 1/4 W 5% RCO7GF223J	81349	F14000871	
0198	K1-K4	D	RELAY AROMAT DS4E-S-DCSV	61529	F20000535	
0199	CR7-CR10	D	DIODE IN4148	09295	F11000239	
0200	I1, I4, I5, I6	D	LED RED 5 V DIALITE 550-0504	05200	F21000187	
0201	J1-J16	D	CONN 34 PIN VERT CRD 6695Z-017	01933	F23001613	
0202	P1-P16	D	CONN AMP 9 PIN 745066-6	00779	F23001191	
0203	C3-C36	D	CAPACITOR .01MF 100 V CK05BX103K	81349	F15000441	
0204	U3-U34	D	IC SOC 16 POS RN ICA-163-S-TG	09824	F23001126	
0205	U1, U2, U35, U36	D	IC SOC 8 POS RN ICA-083-S-TG	09824	F23001100	
0206	P17-P20	D	RIGHT ANGLE HDR 4 WALL	09824	F23009087	
0207	K1-K4	D	SOCKET 14P SIP CA-S14STL-10SD	09824	F23001647	
0208	C37	D	CAP 100UF 10 V T392E107M010AS	81349	F15000433	
0209	P21, P22	D	DIODE IN5820	07263	F11000051	
0210		D	CONN 10PIN MOLEX 09-66-5103	27264	F23001662	
0211	I2, I3, I7, I8	D	LED RED 12 V DIALITE 550-0604	05200	F21000195	
0212		D	PWB/PWM BUS CONN BKPLN-ENH	65519	F76001635	
0213		D	SCHEM — Same as Item 0193			
0214		D	STANDOFF 9723-B-0440	06540	F42001024	
0215		D	KEPNUT — Same as Item 0093			
0216		D	WASHER — Same as Item 0114			
0217		D	WASHER — Same as Item 0121			
0218	C1, C2	D	CAP .01MF 50 V	81349	F15001266	
0219		C	PANEL RT SIDE BUS CD CAGE MOD	65519	F82000761-001	
0220		C	PANEL LT SIDE BUS CD CAGE MOD	65519	F82000761-002	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0221		C	CARD CAGE SCANBE 31170	18677	F41000464	
0222		C	SCREW — Same as Item 0126			
0223		C	DES STRIP, BUS CONN CARD	65519	F79002028	
0224	1B5 — B8	B	POWER SUPPLY ASSY, (2) MULTI	65519	F64000714	
0225		C	CHASSIS POWER SUPPLY	65519	F82000779	
0226		C	SUPPORT POWER SUPPLY	65519	F82000589	
0227		C	PANEL P/S DUAL	65519	F82000555	
0228		C	CABLE ASSY, PS, M/V, DC INTCON 2	65519	F62002399	
0229	P5	D	CONN 9 POS MOL 19-09-2092 PLUG	27264	F23001423	
0230	J1	D	TERM MALE MOL 02-09-2103	27264	F26001529	
0231		D	CONN 9POS MOL 19-09-1091 RECP	27264	F23001415	
0232		D	TERM FEMALE MOL 02-09-1103	27264	F26001537	
0233		D	WIRE 16AWG UL 1007 BLACK	09047	F28000974	
0234		D	WIRE 16AWG UL 1007 BLUE	09047	F28000990	
0235		D	WIRE 16AWG UL 1007 VIOLET	09047	F28001097	
0236		D	WIRE 16AWG UL 1007 GREY	09047	F28001071	
0237		D	WIRE 16AWG UL 1007 ORANGE	09047	F28001089	
0238		D	WIRE 16AWG UL 1007 RED	09047	F28001014	
0239		D	MARKER PLATE — Same as Item 0100			
0240		D	WRAP-IT — Same as Item 0099			
0241	A1PS2, A2PS1	C	POWER SUPPLY ASSEMBLY, 5 V, DC, (M)	65519	F64000888	
0242		D	POWER SUPPLY 5 V 12 A PWR1	54407	F51000446	
0243		D	CABLE ASSY, PS, 5 V, TX	65519	F62002423	
0244	P6	E	CONN 3 POS MOL 19-09-2032 PLUG	27264	F23001407	
0245		E	TERM MALE — Same as Item 0230			
0246		E	WIRE 16AWG UL 1007 WHITE	09047	F28000982	
0247		E	WIRE BLACK — Same as Item 0233			
0248		E	PLATE — Same as Item 0100			
0249		E	WRAP-IT — Same as Item 0099			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0250		D	STANDOFF, .25 HEX X 2.625 LG.	06540	F42000430	
0251		D	COVER, POWER SUPPLY (S/V)	65519	F82000548	
0252		D	SCREW SLOTTED HEX HD 6-32	01608	F47004189	
0253		D	SCREW SLOTTED HEX HD 8-32X1/2	01608	F47004205	
0254		D	WASHER, FLAT, PLAIN NO. 8	06540	F48000145	
0255		D	WASHER, SPLIT, LOCK NO. 8	06540	F48000137	
0256		D	NUT, HEX 8-32	10516	F46000071	
0257		D	GRMT, CATERPILLER HHS 2692		F29000189	
0258		D	BRACKET, POWER SUPPLY (M/V) (F)	65519	F82000530-001	
0259		D	BRACKET, POWER SUPPLY (M/V) (R)	65519	F82000530-002	
0260		D	CABLE ASSY POW SUP M/V 5VDC (2)	65519	F62002381	
0261	J5	E	CONN 9 POS MOL 19-09-1092 RECP	27264	F23001449	
0262		E	TERM FEMALE — Same as Item 0232			
0263	P7	E	CONN 4 POS MOL 19-09-2042 PLUG	27264	F23001464	
0264		E	TERM MALE — Same as Item 0230			
0265		E	WIRE BLACK — Same as Item 0233			
0266		E	WIRE BLUE — Same as Item 0234			
0267		E	WIRE VIOLET — Same as Item 0235			
0268		E	WIRE GREY — Same as Item 0236			
0269		E	WIRE ORANGE — Same as Item 0237			
0270		E	WIRE RED — Same as Item 0238			
0271		E	MARKER PLATE — Same as Item 0100			
0272		E	WRAP-IT — Same as Item 0099			
0273	J4	E	CONN 4 POS MOL 19-09-1042 RECP	27264	F23001456	
0274		E	WRAP-IT — Same as Item 0099			
0275		D	SCREW HH SLOT ZP 8-32X1/4	01608	F47004239	
0276	A1PS1, A2PS2	C	POWER SUPPLY ASSY, 12 V dc	54407	F64000797	
0277		D	PWR SUP ±12V ACDC ECV12D1.7	08742	F51000479	
0278		D	CABLE ASSY PS 12 V dc	65519	F62002373	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0279	J7	E	CONN — Same as Item 0273			
0280		E	TERM — Same as Item 0232			
0281		E	MARKER PLATE — Same as Item 0100			
0282		E	WRAP-IT — Same as Item 0099			
0283		E	WIRE BLACK — Same as Item 0233			
0284		E	WIRE GREY — Same as Item 0236			
0285		E	WIRE BLUE — Same as Item 0234			
0286		D	CABLE ASSY, PS, 12 V, TX	65519	F62002357	
0287	J8	E	CONN 3POS MOL 19-09-1032 RECP	27264	F23001431	
0288		E	TERM FEMALE — Same as Item 0232			
0289		E	WRAP-IT — Same as Item 0099			
0290		E	MARKER PLATE — Same as Item 0100			
0291		E	WIRE BLACK — Same as Item 0233			
0292		E	WIRE WHITE — Same as Item 0246			
0293		D	STANDOFF, HEX AMATOM 8236-SS-0632	06540	F42001016	
0294		D	COVER, POWER SUPPLY (12 V)	65519	F82000886	
0295		D	SCREW — Same as Item 0252			
0296		D	SCREW — Same as Item 0253			
0297		D	WASHER — Same as Item 0254			
0298		D	WASHER — Same as Item 0255			
0299		D	NUT — Same as Item 0256			
0300		D	GRMT — Same as Item 0257			
0301		D	BRACKET, POW SUP (12 V) (F)	65519	F82000829	
0302		D	BRACKET, POW SUP (12 V) (R)	65519	F82000837	
0303		D	WRAP-IT — Same as Item 0099			
0304		C	CABLE ASSY, CIRCUIT BREAKER M/V	65519	F62002340	
0305	A1CB1, A2CB1	D	CIRCUIT BRKR, HEIN TXIP02L05WH2	74185	F24000424	
0306	P3, P8	D	CONN — Same as Item 0244			
0307		D	TERM — Same as Item 0230			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0308	P4	D	CONN — Same as Item 0263			
0309		D	PLATE — Same as Item 0100			
0310		D	WRAP-IT — Same as Item 0099			
0311		D	SLVG FIT105-1/4 BLACK SHRING	09047	F28001196	
0312		D	SLVG FIT105-1/8 BLACK SHRING	09047	F28001188	
0313		D	WIRE BLACK — Same as Item 0233			
0314		D	WIRE — Same as Item 0119			
0315		D	WIRE — Same as Item 0246			
0316		D	WIRE — Same as Item 0118			
0317		C	HANDLES, W/3 MTG CTRS BUD H9168	10187	F49000789	
0318		C	CABLE ASSY, PS M/V TX INTCON 1	65519	F62002365	
0319	J2	D	CONN 3POS MOL 19-09-1031 RECP	27264	F23001399	
0320	J3, J6	D	CONN — Same as Item 0287			
0321		D	TERM FEMALE — Same as Item 0232			
0322		D	WIRE WHITE — Same as Item 0246			
0323		D	WIRE BLACK — Same as Item 0233			
0324		D	PLATE — Same as Item 0100			
0325		D	WRAP-IT — Same as Item 0099			
0326		C	SCREW — Same as Item 0253			
0327		C	WASHER, NO 6 STAR MS3533-7	30829	F48000301	
0328		C	WIRING DIAG PWR SPLY DUAL	65519	F83000240	
0329	1A9/B9	B	FAN ASSEMBLY, QUAD	65519	F64000920	
0330		C	CABLE ASSY, FAN ASSEMBLY	65519	F62002241-002	
0331		D	COND PWR SUPPLY CORD 17	70903	F28001030	
0332		D	TERM — Same as Item 0230			
0333	P1	D	CONN — Same as Item 0244			
0334		D	RGLG BLUE 10 STUD HHS 487	01298	F26001560	
0335		D	PLATE — Same as Item 0100			
0336		D	WRAP-IT — Same as Item 0099			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0337		C	QUAD FAN ASSEMBLY	12831	F49000805	
0338		C	CONN — Same as Item 0319			
0339		C	TERM — Same as Item 0232			
0340		C	KEPNUT — Same as Item 0172			
0341		C	WIRING DIAG FAN ASSY QUAD	65519	F83000141	
0342	1B11(B12)	B	AC DISTRIBUTION PANEL ASSY	65519	F64000763	
0343		C	PANEL, FRONT, AC DISTRIBUTION	65519	F82000605	
0344		C	PANEL, REAR, AC DISTRIBUTION	65519	F82000621	
0345		C	HOUSING, AC DISTRIBUTION	65519	F82000613	
0346	J1	C	RECEPT HUBBELL 4716-C	74545	F23001837	
0347	F1	C	FILTER, HOPKINS F85066	02777	F29000171	
0348	CB1, CB2	C	CIRCUIT BRKR, HEIN TX1P15U00WH2	74185	F24000440	
0349	J2-J6	C	RECEPTACLE, GRAINGERS 6X064	25795	F23008154	
0350	DS1	C	INDICATOR, GEN INST 5100-832	71744	F21000203	
0351		C	LENS CAP, GEN INST 25P-607 AMBER	84353	F21000211	
0352		C	LAMP, NEON GEN INST BZA	84353	F21000229	
0353		C	SCREW — Same as Item 0252			
0354		C	KEPNUT — Same as Item 0340			
0355		C	WIRE, 1 FT. 12GA SOLID BLACK	09047	F28001329-001	
0356		C	WIRE, 1 FT. 12GA SOLID WHITE	09047	F28001311-001	
0357		C	WIRE 14AWG GREEN UL 1015	09047	F28001345	
0358		C	SCREW, PHPH, 6-32X1/2, ZNC	30829	F47000500	
0359		C	WASHER, FLAT, NO.6	30829	F48000293	
0360		C	SLVG — Same as Item 0311			
0361		C	SLVG FIT105-3/8 BLACK	09047	F28001204	
0362		C	RING LUG 16-14AWG NO.8	83330	F26001602	
0363		C	QDLG FEM 16-14AWG .25X.03	83330	F26001586	
0364		C	QDLG FEM 12-10AWG .25X.03	83330	F26001594	
0365		C	SPADE LUG 12-10AWG NO.8	83330	F26001610	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0366		C	WIRING DIAG AC PWR DIST	65519	F83000133	
0367		C	WIRE WHITE — Same as Item 0246			
0368		C	WIRE BLACK — Same as Item 0233			
0369	1B10	B	GPI/GPO PANEL ASSY W/2 PCB	65519	F64000771-002	
0370		C	PWB ASSY GPI/GPO INTERFACE BD	65519	F60002631	
0371	J1, J2	D	RECEPTACLE AMP 206838-1	00779	F23007842	
0372		E	CONTACT SOCKET AMP 66461-7	00779	F23007875	
0373		E	CONTACT PIN AMP 66460-7	00779	F23007867	
0374		D	STANDOFF, .188 DIA.X .719 LG.	06540	F42001032	
0375		D	SCREW PAN HEAD 6-32X3/8 LG.	06540	F47000427	
0376		D	PWB/PWM GPI/GPO INTERFACE BD	65519	F76001668	
0377		D	SCHEM GPI/GPO INTERFACE BOARD	65519	F75001594	
0378		C	PANEL, GPI/GPO	65519	F82000811	
0379		D	SCREW — Same as Item 0375			
0380		C	STANDOFF, AMATOM 8219SS0632	06540	F42001040	
0381		B	SUB-ASSEMBLY CABINET, RFI	65519	F64000946-002	
0382		C	CABINET RFI STAND METAL 50106	90249	F41000175	
0383		C	BUS BAR, SIGNAL GND	65519	F82000670	
0384		C	KEPNUT, 8-32	30829	F46000154	
0385		C	NAMEPLATE, FDIO	65519	F74000506	
0386		C	SCREW — Same as Item 0094			
0387		C	KEPNUT — Same as Item 0093			
0388		C	WASHER NYLON HH SMITH 2665	83330	F48000186	
0389		C	LOGO PLATE, CABINET	65519	F47000233	
0390		C	SCREW SLOTTED HEX HD 8-32X.625	06540	F47000468	
0391		C	CABINET LEVELER LONG	90249	F49001191	
0392	1B3 — B4	B	POWER SUPPLY ASSY, (2) SINGLE	65519	F64000748	
0393		C	CHASSIS — Same as Item 0225			
0394		C	PWR SUPPLY — Same as Item 0226			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0395		C	PANEL P/S DUAL — Same as Item 0227			
0396		C	CABLE ASSY, AC, REAR PANEL (S/V)	65519	F62002167	
0397	J3, J6	D	CONN — Same as Item 0287			
0398	J1	D	CONN — Same as Item 0319			
0399		D	WIRE — Same as Item 0233			
0400		D	WIRE — Same as Item 0246			
0401		D	WRAP-IT — Same as Item 0099			
0402		D	TERM — Same as Item 0232			
0403		D	PLATE — Same as Item 0100			
0404	1B3A1PS2 (A2PS1)	C	POWER SUPPLY ASSEMBLY, DC, S/V (S)	65519	F64000805	
0405		D	PS 5 V 12 A — Same as Item 0242			
0406		D	CABLE ASSY, POWER SUPPLY, AC	65519	F62001987	
0407	P6	E	CONN — Same as Item 0244			
0408		E	TERM — Same as Item 0230			
0409		E	WIRE BLACK — Same as Item 0233			
0410		E	WIRE WHITE — Same as Item 0246			
0411		E	WRAP-IT — Same as Item 0099			
0412		E	PLATE — Same as Item 0100			
0413		D	CABLE ASSY POWER SUPPLY DC S/V	65519	F62001995	
0414	J5	E	CONN — Same as Item 0261			
0415		E	TERM — Same as Item 0232			
0416	J4	E	CONN — Same as Item 0273			
0417		E	WIRE BLACK — Same as Item 0233			
0418		E	WIRE VIOLET — Same as Item 0235			
0419		E	WIRE ORANGE — Same as Item 0237			
0420		E	WIRE RED — Same as Item 0238			
0421		E	WRAP-IT — Same as Item 0099			
0422		E	PLATE — Same as Item 0100			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0423		D	STANDOFF — Same as Item 0250			
0424		D	COVER, — Same as Item 0251			
0425		D	SCREW — Same as Item 0252			
0426		D	SCREW — Same as Item 0253			
0427		D	WASHER — Same as Item 0254			
0428		D	WASHER — Same as Item 0255			
0429		D	NUT — Same as Item 0256			
0430		D	GRMT — Same as Item 0257			
0431		D	BRACKET — Same as Item 0258			
0432		D	BRACKET — Same as Item 0259			
0433		D	WRAP-IT — Same as Item 0099			
0434		C	CABLE — Same as Items 0228 — 0240			
0435		C	SCREW — Same as Item 0275			
0436		C	CABLE ASSY — CIRCUIT BREAKER S/V	65519	F62002175	
0437	CB1	D	CIRCUIT BRKR — Same as Item 0305			
0438	P3	D	CONN — Same as Item 0244			
0439	P4	D	CONN — Same as Item 0263			
0440		D	WIRE — Same as Item 0233			
0441		D	WIRE — Same as Item 0314			
0442		D	WIRE BLACK — Same as Item 0118			
0443		D	WRAP-IT — Same as Item 0099			
0444		D	TERM — Same as Item 0230			
0445		D	PLATE — Same as Item 0100			
0446		D	SLVG — Same as Item 0312			
0447		D	SLVG — Same as Item 0311			
0448		C	HANDLES — Same as Item 0317			
0449		C	SCREW — Same as Item 0252			
0450		C	SCREW — Same as Item 0253			
0451		C	WASHER — Same as Item 0327			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0452		C	WIRING DIAG PWR SPLY DUAL	65519	F83000265	
0453		B	CABLE ASSY ICL INTERCONNECT	65519	F62002449	
0454	P1, P2	C	CONN 10 POS EDGE BERG6631	95871	F23001712	
0455		C	CABLE 28 AWG STRND 3M 3365/10	53387	F28000867	
0456		C	PLATE — Same as Item 0100			
0457		C	WRAP-IT — Same as Item 0099			
0458		B	CABLE ASSY, F/S INTERCONNECT	65519	F62001847	
0459	P1, P2	C	CONN EDG 14 POS BERG 6631	95871	F23001241	
0460		C	CA — Same as Item 0098			
0461		C	MARKER PLATE — Same as Item 0100			
0462		C	WRAP-IT — Same as Item 0099			
0463		B	CABLE ASSY, GPI/GPO INTERFACE	65519	F62001821	
0464	P1-P4	C	CONN 40 POS BERG 66317-040	95871	F23001258	
0465		C	WRAP-IT RICHCO WIT	06915	F42000968	
0466		C	CABLE 28AWG STRAND 3M 3365/40	53387	F28000925	
0467		C	MARKER PLATE — Same as Item 0100			
0468		B	CABLE ASSY, MULTIBUS CARD CAGE	65519	F62001979	
0469	P1	C	CONN — Same as Item 0229			
0470		C	TERM — Same as Item 0230			
0471	P6, P8	C	CONN INS DISP MOL 09-07-2-06-8	27264	F23001472	
0472		C	KEY POLARIZING MOLEX15-04-0288	27264	F23001480	
0473		C	WIRE — Same as Item 0233			
0474		C	WIRE — Same as Item 0238			
0475		C	WIRE — Same as Item 0236			
0476		C	WIRE — Same as Item 0237			
0477		C	WIRE — Same as Item 0234			
0478		C	WIRE — Same as Item 0235			
0479		C	WRAP-IT — Same as Item 0099			
0480		C	PLATE — Same as Item 0100			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0481		C	SPLICE, WIRE AMP	00779	F26001636	
0482		C	QDLG — Same as Item 0363			
0483		C	HARNESS RAP, RICHO HR3-3/16-R	06915	F28001162	
0484		B	CABLE ASSY BUS CONN CARD CAGE	65519	F62002266	
0485	P1	C	CONN — Same as Item 0229			
0486	P2	C	CONN INS DISP MOL 09-07-2-10-6	27264	F23001803	
0487		C	TERM — Same as Item 0230			
0488		C	WIRE BLACK — Same as Item 0233			
0489		C	WIRE RED — Same as Item 0238			
0490		C	WIRE BLUE — Same as Item 0234			
0491		C	WIRE GREY — Same as Item 0236			
0492		C	WIRE VIOLET — Same as Item 0235			
0493		C	HARNESS — Same as Item 0483			
0494		C	PLATE — Same as Item 0100			
0495		C	WRAP-IT — Same as Item 0099			
0496		C	SPLICE — Same as Item 0481			
0497		C	QDLG — Same as Item 0363			
0498		C	WIRE ORANGE — Same as Item 0237			
0499		C	KEY — Same as Item 0472			
0500		B	CABLE ASSY-LAN PCB INT	65519	F62002993	
0501		C	CONN HOUSING 10 POS	00779	F23009079	
0502		C	5 COND. CABLE — FC	16428	F28002087	
0503		C	LAN INTERFACE PCB ASSY	65519	F60003128	
0504		D	LAN INTERFACE PWB/PWM	65519	F76001700	
0505		D	STRAIGHT 4 WALL HDR — FC	00779	F23009129	
0506		D	26 POS EDGE PCB CONN — FC	00779	F23009111	
0507		D	SCHEMATIC, LAN INTERFACE	05519	F75001636	
0508		C	SLVG — Same as Item 0361			
0509		C	SLVG — Same as Item 0311			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0510		C	PLATE — Same as Item 0100			
0511		C	WRAP-IT — Same as Item 0099			
0512		C	EJECTION COVER — FC	00779	F23009145	
0513		C	BACK COVER — FC	00779	F23009137	
0514		B	CABLE ASSY AC PWR INTERNAL	65519	F62002241-001	
0515		C	PS CORD — Same as Item 0331			
0516		C	TERM — Same as Item 0230			
0517	P1, P2	C	CONN — Same as Item 0244			
0518		C	RGLG — Same as Item 0334			
0519		C	PLATE — Same as Item 0100			
0520		C	WRAP-IT — Same as Item 0099			
0521		B	KIT, CABLE ENTRY (TALL)	65519	F64001027-002	
0522		C	HOUSING, CABLE ENTRY (TALL)	65519	F82000860-002	
0523		C	GASKET, EMI, COVER PLATE	65519	F82001017	
0524		C	GUIDE TALL	65519	F82000803-002	
0525		C	CLAMP, LOWER CAB.CABLE ENT	65519	F82000795	
0526		C	CLAMP, UPPER CAB.CABLE ENT	65519	F82000787	
0527		C	GASKET, EMI, CABLE (1/4)	65519	F82001025	
0528		C	GASKET, EMI.CABLE (1/2)	65519	F82001041	
0529		C	CHANNEL, CABLE SHIELDING	65519	F82001082	
0530		C	COVER PLATE, CABINET	65519	F82000852	
0531		C	GASKET, EMI, HOUSING	65519	F82001280	
0532		C	COUPLING-SCREW-IN		F49001068	
0533		C	FLEX CONDUIT, 3/4-CA ENTRY	65519	F82001330	
0534		C	COUPLING 3/4 — FC		F49001050	
0535		C	PULL BOXES, BOWERS 4X4X11		F49001043	
0536		C	WIRE CONNECTOR — FC		F49001076	
0537		C	CABLE ASSY, AC POWER	65519	F62002258	
0538		D	PWR CORD BELDEN 19206	16428	F28001154	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0539	P1	D	CONN BODY HUBBELL 4729-C	08793	F23001829	
0540		D	PLATE — Same as Item 0100			
0541		D	WRAP-IT — Same as Item 0099			
0542		C	COUPLING, GALVANIZED, 3/4		F49001092	
0543		C	BOLT, HEX HEAD 1/4-20X1.5	06608	F47000476	
0544		C	SCREW, PHPH, 10-32X1/2	30829	F47004254	
0545		C	SCREW, CABLE CLAMP	65519	F82001348	
0546		C	BOLT HEX — Same as Item 0543			
0547		C	NUT, UNISTRUT	06364	F46000162	
0548		C	WASHER, FLAT, NO.10 — FC	01608	F48100000	
0549		B	BRACKET, SUPPORT, FAN HSG	65519	F82001249	
0550		B	BRACKET, STATUS SHEET	65519	F82001256	
0551		C	WINDOW, STATUS SHEET	65519	F82001264	
0552		C	NOTE PAD, POST-IT, 3X5 — FC	28218	F49001019	
0553		B	KIT DRAWING, FRONT, PAIR	65519	F79001921	
0554		B	KIT DRAWING, REAR, PAIR	65519	F79001939	
0555		B	SCREW — Same as Item 0544			
0556		B	SCREW 10-32 STD METAL	01608	F47000286	
0557		B	SCREW, PHPH, 6-32X1/2, ZNC	30829	F47004122	
0558		B	WASHER, SPLIT LOCK, NO.10	01608	F48000319	
0559		B	CLAMP, CABLE, RICHCO N6	06915	F49000813	
0560		B	SCREW — Same as Item 0253			
0561		B	KEPNUT — Same as Item 0384			
0562		B	TAB, FASTON, .250X.032 — FC	05972	F26001644	
0563		B	SCREW, PHPH 10-32X1/4 — FC	30829	F47004247	
0564		B	SLIDES, PR., POWER SUPPLY	12879	F49000680	
0565		B	SLIDE MTG BRKTS(4)	12879	F49000748	
0566		B	SCREW — Same as Item 0275			
0567		B	WIRING DIAG CCU/CCU CABINET	65519	F83000208	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0568		B	CABLE ASSY-LAN CARD CAGE	65519	F62003009	
0569		C	CONN — Same as Item 0501			
0570		C	CA — Same as Item 0502			
0571		C	SLVG — Same as Item 0311			
0572		C	PLATE — Same as Item 0100			
0573		C	WRAP-IT — Same as Item 0099			
0574		C	COVER — Same as Item 0512			
0575		C	COVER — Same as Item 0513			
0576		B	NAMEPLATE, PS, DUAL MV, 12V	65519	F74000357	
0577		B	NAMEPLATE, PS, DUAL SV, 5V	65519	F74000332	
0578		B	ADHESIVE 3M 847 — FC	04963	F49001035	
0579		B	WRAP-IT Same as Item 0099			
0580	2	A	PCU/PCU CABINET ASSY	65519	F64000631	
0581	2A1 (2A3)	B	MULTIBUS ASSY, PCU CPU W/TERMINATOR	65519	F64000789-003	
0582		C	CHASSIS — Same as Item 0003			
0583		C	INTEL SBC 88/45 ASSY MOD Same as Items 0004 — 0018			
0584	2A1A2A2	C	UTILITY BD ASSY ENH Same as Items 0019 — 0068			
0585		C	ASSY FDIO TERM BD Same as Items 0069 — 0072			
0586	2A1A1	C	MULTIBUS FP ASSY Same as Items 0073 — 0129			
0587	2A1A2A2, U24	C	PROM SET UTILITY Same as Items 0130 — 0134			
0588	2A1A2A1, U49, U50 U89, U90	C	PROM SET PCU-CPU	65519	F18000745	
0589	U49	D	PROM PCU-1	65519	F17017039	
0590		E	IC EPROM — Same as Item 0137			
0591		E	LABEL PROM PCU-1	65519	F74000373-005	
0592		E	PROGRAM PCU-1	65519	F68000389	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0593	U50	D	PROM PCU-2	65519	F17017047	
0594		E	IC EPROM — Same as Item 0137			
0595		E	LABEL PROM PCU-2	65519	F74000373-006	
0596		E	PROGRAM PCU-2	65519	F68000397	
0597		D	PROM PCU-3	65519	F17017054	
0598	2A1A2A2, U89	E	IC EPROM — Same as Item 0137			
0599		E	LABEL PROM PCU-3	65519	F74000373-007	
0600		E	PROGRAM PCU-3	65519	F68000405	
0601	U90	D	PROM PCU-4	65519	F17007147	
0602		E	IC EPROM — Same as Item 0137			
0603		E	LABEL PROM PCU-4	65519	F74000373-008	
0604		E	PROGRAM PCU-4 REV 3.3	65519	F68000546	
0605	2A1A2A1A1	C	PWB ASSY FP I/F Same as Items 0152 — 0164			
0606		C	CA ASSY — Same as Items 0165 — 0168			
0607		C	SCREW — Same as Item 0169			
0608		C	KEPNUT — Same as Item 0170			
0609		C	NAMEPLATE, PCU	65519	F74000763	
0610		C	KEPNUT — Same as Item 0172			
0611		C	CABLE ASSY — Same as Items 0173 — 0178			
0612		C	LOCTITE — Same as Item 0179			
0613	2A2 (2A4)	B	MULTIBUS ASSY, PCU CPU W/O TERM	65519	F64000789-004	
0614		C	CHASSIS — Same as Item 0003			
0615		C	INTEL SBC 88/45 ASSY Same as Items 0004 — 0018			
0616		C	ASSY UTILITY BD Same as Items 0019 — 0068			
0617	2A2A1	C	MULTIBUS FP ASSY Same as Items 0073 — 0129			
0618	2A1A2A2, U24	C	PROM SET UTILITY Same as Items 0130 — 0134			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0619		C	PROM SETS PCU CPU Same as Items 0588 — 0604			
0620		C	PWB ASSY — Same as Items 0152 — 0164			
0621		C	CA ASSY — Same as Items 0165 — 0168			
0622		C	SCREW — Same as Item 0169			
0623		C	KEPNUT — Same as Item 0170			
0624		C	NAMEPLATE — Same as Item 0609			
0625		C	KEPNUT — Same as Item 0172			
0626		C	CA ASSY — Same as Items 0173 — 0178			
0627		C	LOCTITE — Same as Item 0179			
0628		B	BUS CONN TOP ASSY Same as Items 0184 — 0223 and Items 1104 through 1143 for A1 — A16 Bus Connector board parts breakdown.			
0629		B	FAN ASSY QUAD Same as Items 0329 — 0341			
0630		B	AC DIST ASSY Same as Items 0342 — 0368			
0631		B	GPI/GPO ASSY Same as Items 0369 — 0380			
0632		B	SUB ASSY CAB RFI Same as Items 0381 — 0391			
0633		B	PWR (2) SIN Same as Items 0392 — 0452			
0634		B	CA ASSY ICL Same as Items 0453 — 0457			
0635		B	CA ASSY FS Same as Items 0458 — 0462			
0636		B	CA ASSY GPI/GPO Same as Items 0463 — 0467			
0637		B	CA ASSY MULTI PWR Same as Items 0468 — 0483			
0638		B	CA ASSY BC PWR Same as Items 0484 — 0499			
0639		B	CA ASSY LAN Same as Items 0500 — 0513			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0640		B	CA ASSY AC PWR Same as Items 0514 — 0520			
0641		B	KIT CA ENTRY Same as Items 0521 — 0548			
0642		B	BRACKET FAN — Same as Item 0549			
0643		B	BRACKET STATUS Same as Items 0550 — 0552			
0644		B	KIT, DRAW, FRONT — Same as Item 0053			
0645		B	KIT, DRAWING, REAR	65519	F79001996	
0646		B	HDWR — Same as Items 0555 — 0566			
0647		B	WIRING DIAG PCU/PCU CABINET	65519	F83000216	
0648		B	CA ASSY LAN Same as Items 0568 — 0575			
0649		B	NAMEPLATE — Same as Item 0577			
0650		B	ADHESIVE — Same as Item 0578			
0651		B	WRAP-IT — Same as Item 0099			
0652	3	A	CCU/PCU CABINET ASSY	65519	F64000649	
0653	3A1	B	MULTIBUS ASSY W/TERM Same as Items 0002 — 0179			
0654	3A2	B	MULTIBUS ASSY — CCU CPU W/O TERM Same as Items 0003 — 0068, 0073 — 0179	65519	F64000789-003	
0655	3A5 — A6	B	BUS CONN TOP ASSY Same as Items 0184 — 0223 and Items 1104 through 1143 for A1 — A16 Bus Connector board parts breakdown.			
0656	3B7, B8	B	PWR (2) MULTI Same as Items 0224 — 0328			
0657	3A9, B9	B	FAN ASSY QUAD Same as Items 0329 — 0341			
0658	3B11, B12	B	AC DIST ASSY Same as Items 0342 — 0368			
0659	3B10	B	GPI/GPO ASSY Same as Items 0369 — 0380			
0660		B	SUB ASSY CAB RFI Same as Items 0381 — 0391			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0661	3B3 — B4	B	PWR (2) SIN — Same as Items 0392 — 0452			
0662		B	CA ASSY ICL — Same as Items 0453 — 0457			
0663		B	CA ASSY FS — Same as Items 0458 — 0462			
0664		B	CA ASSY GPI/GPO Same as Items 0463 — 0467			
0665		B	CA ASSY MULTI PWR Same as Items 0468 — 0483			
0666		B	CA ASSY BC PWR Same as Items 0484 — 0499			
0667		B	CA ASSY LAN Same as Items 0500 — 0513			
0668		B	CA ASSY AC PWR Same as Items 0514 — 0520			
0669		B	KIT CA ENTRY Same as Items 0521 — 0548			
0670		B	BRACKET FAN — Same as Item 0549			
0671		B	BRACKET STATUS Same as Items 0550 — 0552			
0672		B	KIT, DRAW, FRONT — Same as Item 0553			
0673		B	HDWR — Same as Items 0555 — 0566			
0674		B	WIRING DIAG — Same as Item 0567			
0675		B	CA ASSY LAN Same as Items 0568 — 0575			
0676		B	NAMEPLATE — Same as Item 0576			
0677		B	NAMEPLATE — Same as Item 0577			
0678		B	ADHESIVE — Same as Item 0578			
0679		B	WRAP-IT — Same as Item 0099			
0680	3A3	B	MULTIBUS ASSY PCU CPU W/TERM Same as Items 0581 — 0612			
0681	3A4	B	MULTIBUS ASSY PCU CPU W/O TERM Same as Items 0613 — 0627			
0682	3A7, A8	B	BUS CONN TOP ASSY Same as Items 0184 — 0223			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0683	3A9, B9	B	FAN ASSY QUAD Same as Items 0329 — 0341			
0684	3B11, B12	B	AC DIST ASSY Same as Items 0342 — 0368			
0685	3B10	B	GPI/GPO ASSY Same as Items 0369 — 0380			
0686		B	SUB ASSY CAB RFI Same as Items 0381 — 0391			
0687	3B5, B6	B	PWR (2) SIN Same as Items 0392 — 0452			
0688		B	CA ASSY ICL Same as Items 0453 — 0457			
0689		B	CA ASSY FS Same as Items 0458 — 0462			
0690		B	CA ASSY GPI/GPO Same as Items 0463 — 0467			
0691		B	CA ASSY MULTI PWR Same as Items 0468 — 0483			
0692		B	CA ASSY BC PWR Same as Items 0484 — 0499			
0693		B	CA ASSY LAN Same as Items 0500 — 0513			
0694		B	CA ASSY AC PWR Same as Items 0514 — 0520			
0695		B	KIT CA ENTRY Same as Items 0521 — 0548			
0696		B	BRACKET FAN — Same as Item 0549			
0697		B	BRACKET STATUS Same as Items 0550 — 0552			
0698		B	KIT, DRAW, FRONT — Same as Item 0553			
0699		B	HDWR — Same as Items 0555 — 0566			
0700		B	WIRING DIAG PCU — Same as Item 0647			
0701		B	CA ASSY LAN Same as Items 0568 — 0575			
0702		B	NAMEPLATE — Same as Item 0577			
0703		B	ADHESIVE — Same as Item 0578			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0704		B	WRAP-IT — Same as Item 0099			
0705	4	A	CCU CABINET ASSY	65519	F64000656	
0706	4A1	B	MULTIBUS CCU CPU W/TERM Same as Items 0002 — 0179			
0707	4A2	B	MULTIBUS ASSY — CCU CPU W/O TERM Same as Items 0003 — 0068, 0073 — 0179			
0708	4A3 (A4)	B	BUS CONN TOP ASSY — Same as Items 0184 — 0223 and Items 1104 through 1143 for A1 — A16 Bus Connector board parts breakdown.			
0709	4B4 — B5	B	POWER — Same as Items 0224 — 0328			
0710	4A5/B6	B	FAN — Same as Items 0329 — 0341			
0711	4B11, B12	B	AC — Same as Items 0342 — 0368			
0712	4B10	B	GPI/GPO PANEL ASSY	65519	F64000771-001	
0713	A2	C	PWB — Same as Items 0370 — 0380			
0714		B	CA SUB ASSY — Same as Items 0381 — 0391			
0715	4B3	B	PWR (2) SIN — Same as Items 0392 — 0452			
0716		B	CA ICL — Same as Items 0453 — 0457			
0717		B	CA FS — Same as Items 0458 — 0462			
0718		B	CA GPI/GPO — Same as Items 0463 — 0467			
0719		B	CA MULTI PWR Same as Items 0468 — 0483			
0720		B	CA BC PWR — Same as Items 0484 — 0499			
0721		B	CA LAN — Same as Items 0500 — 0513			
0722		B	CA AC PWR — Same as Items 0514 — 0520			
0723		B	KIT — Same as Items 0521 — 0548			
0724		B	BRACKET FAN — Same as Item 0549			
0725		B	BRACKET STATUS Same as Items 0550 — 0552			
0726		B	KIT, DRAW, FRONT — Same as Item 0553			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0727		B	HDWR — Same as Items 0555 — 0566			
0728		B	WIRING DIAG CCU CABINET	65519	F83000182	
0729		B	CA ASSY LAN — Same as Items 0568 — 0575			
0730		B	NAMEPLATE — Same as Item 0576			
0731		B	NAMEPLATE — Same as Item 0577			
0732		B	ADHESIVE — Same as Item 0578			
0733		B	WRAP-IT — Same as Item 0099			
0734	5	A	PCU CABINET ASSY	65519	F64000664	
0735	5A1	B	MULTIBUS ASSY PCU CPU W/TERM Same as Items 0581 — 0612			
0736	5A2	B	MULTIBUS ASSY PCU CPU W/O TERM Same as Items 0613 — 0627			
0737	5A3, A4	B	BUS CONN TOP ASSY Same as Items 0184 — 0223 and Items 1104 through 1143 for A1 — A16 Bus Connector board parts breakdown.			
0738	5A5, B6	B	FAN ASSY QUAD Same as Items 0329 — 0341			
0739	5B11, B12	B	AC DIST ASSY Same as Items 0342 — 0368			
0740	5B10	B	GPI/GPO PANEL ASSY — Same as Item 0712			
0741		C	PWB — Same as Items 0370 — 0380			
0742		B	SUB ASSY CAB RFI Same as Items 0381 — 0391			
0743	5B3, B5	B	PWR (2) SIN — Same as Items 0392 — 0452			
0744		B	CA ASSY ICL — Same as Items 0453 — 0457			
0745		B	CA ASSY FS — Same as Items 0458 — 0462			
0746		B	CA ASSY GPI/GPO Same as Items 0463 — 0467			
0747		B	CA ASSY MULTI PWR Same as Items 0468 — 0483			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0748		B	CA ASSY BC PWR Same as Items 0484 — 0499			
0749		B	CA ASSY LAN Same as Items 0500 — 0513			
0750		B	CA ASSY AC PWR Same as Items 0514 — 0520			
0751		B	KIT CA ENTRY Same as Items 0521 — 0548			
0752		B	BRACKET FAN — Same as Item 0549			
0753		B	BRACKET STATUS Same as Items 0550 — 0552			
0754		B	KIT, DRAW, FRONT — Same as Item 0644			
0755		B	KIT, DRAW, REAR — Same as Item 0645			
0756		B	HDWR — Same as Items 0555 — 0566			
0757		B	WIRING DIAGRAM PCU	65519	F83000174	
0758		B	CA ASSY LAN — Same as Items 0568 — 0575			
0759		B	NAMEPLATE — Same as Item 0577			
0760		B	ADHESIVE — Same as Item 0578			
0761		B	WRAP-IT — Same as Item 0099			
0762	6	A	RCU CABINET ASSY	65519	F64000672	
0763	6A2	B	MULTIBUS ASSY RCU CPU	65519	F64000789-005	
0764		C	CHASSIS — Same as Item 0003			
0765	6A2A2A1	C	INTEL 88/45 ASSY Same as Items 0004 — 0018			
0766	6A2A1	C	MULTIBUS FP ASSY Same as Items 0073 — 0129			
0767		C	PROM SET RCU REV 3.6	65519	F18000752	
0768		D	PROM RCU-1	65519	F17017062	
0769		E	IC EPROM — Same as Item 0137			
0770		E	LABEL PROM RCU-1	65519	F74000373-009	
0771		E	PROGRAM RCU-1 REV 3.6	65519	F68000413	
0772		D	PROM RCU-2	65519	F17017070	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0773		E	IC EPROM — Same as Item 0137			
0774		E	LABEL PROM RCU-2	65519	F74000373-010	
0775		E	PROGRAM RCU-2 REV 3.6	65519	F68000421	
0776		D	PROM RCU-3	65519	F17017088	
0777		E	IC EPROM — Same as Item 0137			
0778		E	LABEL PROM RCU-3	65519	F74000373-011	
0779		E	PROGRAM RCU-3 REV 3.6	65519	F68000439	
0780		D	PROM RCU-4	65519	F17007154	
0781		E	IC EPROM — Same as Item 0137			
0782		E	LABEL PROM RCU-4	65519	F74000373-012	
0783		E	PROGRAM RCU-4 REV 3.6	65519	F68000553	
0784	6A2A2A1A1	C	PWB ASSY FP I/F Same as Items 0152 — 0164			
0785		C	CA ASSY CONF JPR Same as Items 0165 — 0168			
0786		C	SCREW — Same as Item 0169			
0787		C	KEPNUT — Same as Item 0170			
0788		C	NAMEPLATE, RCU	65519	F74000514	
0789		C	KEPNUT — Same as Item 0172			
0790		C	CA ASSY MULTIBUS FP Same as Items 0173 — 0178			
0791		C	LOCTITE — Same as Item 0179			
0792	6A3	B	POWER SUPPLY ASSY, (1) MULTI	65519	F64000722	
0793		C	PWR CHASSIS — Same as Item 0225			
0794		C	PWR SUPPORT — Same as Item 0226			
0795		C	PS PANEL- Same as Item 0811			
0796		C	CA ASSY PS MV DC Same as Items 0228 — 0240			
0797		C	CA ASSY PS MV TX Same as Items 0318 — 0325			
0798		C	PWR ASSY 12 V dc Same as Items 0276 — 0303			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0799		C	HANDLES — Same as Item 0317			
0800		C	CA ASSY CB — Same as Items 0304 — 0316			
0801		C	SCREW — Same as Item 0275			
0802		C	PWR ASSY 5 V (1) MULTI Same as Items 0241 — 0274			
0803		D	RES — Same as Item 0049			
0804		C	SCREW — Same as Item 0326			
0805		C	WASHER — Same as Item 0327			
0806		C	WIRING DIAG PWR SUPPLY SINGLE	65519	F83000232	
0807	6A5	B	BC TOP ASSY — Same as Items 0184 — 0223 and Items 1104 through 1143 for A1 — A16 Bus Connector board parts breakdown.			
0808	6A4	B	POWER SUPPLY ASSY, (1) SIN	65519	F64000755	
0809		C	PWR CHASSIS — Same as Item 0225			
0810		C	PWR SUPPORT — Same as Item 0226			
0811		C	PANEL PS SINGLE	65519	F82000563	
0812		C	CA ASSY AC REAR — Same as Item 0396			
0813		D	CONN — Same as Item 0229			
0814		D	CONN — Same as Item 0338			
0815		D	WIRE BLACK — Same as Item 0368			
0816		D	WIRE WHITE — Same as Item 0246			
0817		D	WRAP-IT — Same as Item 0099			
0818		D	CONN — Same as Item 0232			
0819		D	MARKER PLATE — Same as Item 0100			
0820		C	PWR ASSY DC — Same as Item 0404			
0821		D	PWR 5 V 12 A — Same as Item 0405			
0822		D	CA ASSY PS — Same as Item 0406			
0823		E	CONN — Same as Item 0244			
0824		E	CONN — Same as Item 0230			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0825		E	WIRE BLACK — Same as Item 0368			
0826		E	WIRE WHITE — Same as Item 0246			
0827		E	WRAP-IT — Same as Item 0099			
0828		E	MARKER PLATE — Same as Item 0100			
0829		D	CA ASSY PS — Same as Item 0413			
0830		E	CONN — Same as Item 0261			
0831		E	CONN — Same as Item 0232			
0832		E	CONN — Same as Item 0273			
0833		E	WIRE BLACK — Same as Item 0368			
0834		E	WIRE VIOLET — Same as Item 0235			
0835		E	WIRE ORANGE — Same as Item 0237			
0836		E	WIRE RED — Same as Item 0238			
0837		E	WRAP-IT — Same as Item 0099			
0838		E	MARKER PLATE — Same as Item 0100			
0839		D	STANDOFF — Same as Item 0250			
0840		D	COVER PS (S/V) — Same as Item 0251			
0841		D	SCREW — Same as Item 0252			
0842		D	SCREW — Same as Item 0253			
0843		D	WASHER — Same as Item 0254			
0844		D	WASHER SPLIT — Same as Item 0255			
0845		D	NUT — Same as Item 0256			
0846		D	GRMT — Same as Item 0257			
0847		D	BRACKETS — Same as Items 0258 — 0259			
0848		D	WRAP-IT — Same as Item 0099			
0849		D	RES — Same as Item 0049			
0850		C	CA ASSY PS MV DC Same as Items 0228 — 0240			
0851		C	SCREW HH — Same as Item 0275			
0852		C	CA ASSY CB — Same as Item 0436			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0853		D	CIRCUIT BRKR — Same as Item 0305			
0854		D	CONN — Same as Item 0244			
0855		D	CONN — Same as Item 0263			
0856		D	WIRE BLACK — Same as Item 0233			
0857		D	WIRE RED — Same as Item 0119			
0858		D	WIRE BLACK — Same as Item 0118			
0859		D	WRAP-IT — Same as Item 0099			
0860		D	CONN — Same as Item 0230			
0861		D	MARKER PLATE — Same as Item 0100			
0862		D	SLVG 1/8 — Same as Item 0312			
0863		D	SLVG 1/4 — Same as Item 0311			
0864		C	HANDLES — Same as Item 0317			
0865		C	SCREW — Same as Item 0253			
0866		C	WASHER — Same as Item 0327			
0867		C	WIRING DIAG PWR SUPPLY SINGLE	65519	F83000257	
0868	6A6	B	FAN ASSEMBLY DUAL	65519	F64000938	
0869		C	CA ASSY FAN — Same as Items 0330 — 0336			
0870		C	DUAL FAN ASSEMBLY	12831	F49000862	
0871		C	CONN — Same as Item 0338			
0872		C	CONN — Same as Item 0339			
0873		C	KEPNUT — Same as Item 0340			
0874		C	WIRING DIAG FAN ASSY DUAL	65519	F83000158	
0875		B	SUB-ASSY CABINET RFI REMO	90249	F64000946-001	
0876		C	CAB RFT STAND Same as Items 0382 — 0390			
0877	6A9	B	AC DIST PANEL ASSY Same as Items 0342 — 0368			
0878		B	CA ASSY LAN — Same as Items 0500 — 0513			
0879		B	CABLE ASSY, RCU MODEM	65519	F62002639	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0880		C	CONN 26 POS	95871	F23001340	
0881		C	CONN D 25 POS SHELL	95871	F23001670	
0882		C	CABLE 28 AWG STRAND	53387	F28000891	
0883		C	PLATE CONN MODEM INTERFACE	65519	F82001009	
0884		C	MARKER PLATE — Same as Item 0100			
0885		C	WRAP-IT — Same as Item 0099			
0886		C	STANDOFF — Same as Item 0214			
0887		C	KEPNUT — Same as Item 0093			
0888		B	CA ASSY MULTIBUS — Same as Item 0468			
0889		C	CONN — Same as Item 0229			
0890		C	CONN — Same as Item 0230			
0891		C	CONN — Same as Item 0471			
0892		C	KEY — Same as Item 0472			
0893		C	WIRE — Same as Items 0233 — 0238			
0894		C	WRAP-IT — Same as Item 0099			
0895		C	MARKER PLATE — Same as Item 0100			
0896		C	CONN SPLICE — Same as Item 0481			
0897		C	CONN — Same as Item 0363			
0898		C	SLVG 3/16 — Same as Item 0483			
0899		B	CA ASSY BC CARD Same as Items 0484 — 0499			
0900		B	CAE ASSY AC — Same as Items 0514 — 0520			
0901		B	KIT, CABLE ENTRY (SHORT)	65519	F64001027-001	
0902		C	HOUSING, CABLE ENTRY (SHORT)	65519	F82000860-001	
0903		C	GASKET — Same as Item 0523			
0904		C	GUIDE SHORT	65519	F82000803-001	
0905		C	KIT HDWR — Same as Items 0525 — 0542			
0906		C	SCREW PHPH 1/4-20 X 1	30829	F47100000	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0907		C	SCREW, PHPH — Same as Item 0544			
0908		C	SCREW, CABLE — Same as Item 0545			
0909		C	CONN — Same as Item 0362			
0910		C	NUT — Same as Item 0547			
0911		C	WASHER — Same as Item 0548			
0912		C	WASHER SPLIT — Same as Item 0255			
0913		C	SCREW — Same as Item 0560			
0914		C	KEPNUT — Same as Item 0561			
0915		B	BRACKET — Same as Items 0550 — 0552			
0916		B	KIT DRAWING, RCU	65519	F79001962	
0917		B	HDWR ITEMS — Same as Items 0555 — 0565			
0918		B	SCREW — Same as Item 0126			
0919		B	WRAP-IT — Same as Item 0099			
0920		B	WIRING DIAG RCU CABINET A	65519	F83000166	
0921		B	NAMEPLATE, PS MV, 12, 5 V	65519	F74000340	
0922		B	NAMEPLATE, PS, SV, 5 V	65519	F74000324	
0923		B	ADHESIVE 3M 847 — FC	N/A	F49001035	
0924	6A2A2A2	B	PWB ASSY, 16 K RCU MEMORY	65519	F60100001	
0925	R1-R7	C	RES — Same as Item 0052			
0926	C16, C17	C	CAP 10UF 25 V	81349	F15000409	
0927	C1-C13	C	CAP — Same as Item 0055			
0928	U13	C	IC 74LS245	01295	F17002130	
0929	U8	C	IC — Same as Item 0024			
0930	U3, U9	C	IC — Same as Item 0037			
0931	U4, U5	C	IC — Same as Item 0038			
0932	U2	C	IC — Same as Item 0157			
0933	U1, U10, U11, U12	C	IC — Same as Item 0029			
0934		C	CONN 2X8 STIK II —FC	95871	F23100001	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0935	DS1, DS2	C	LED GREEN — Same as Item 0054			
0936		C	CARD EJTR — Same as Item 0062			
0937		C	PWB RCU MEMORY EXPANSION	65519	F76100001	
0938		C	SOCKET — Same as Item 0064			
0939	W1	C	CONN 1X3	95871	F23001589	
0940		C	CONN — Same as Item 0014			
0941		C	SCHEMATIC 16 K RCU MEMORY	65519	F75100002	
0942	7	A	RCU CABINET ASSY, EXPANDED	65519	F64000680	
0943	7A2	B	MULTIBUS ASSY RCU CPU Same as Item 0763			
0944		C	CHASSIS — Same as Item 0003			
0945	7A2A2A1	C	INTEL 88/45 ASSY Same as Items 0004 — 0018			
0946	7A2A1	C	MULTIBUS FP ASSY Same as Items 0073 — 0129			
0947		C	PROM SET RCU Same as Items 0767 — 0783			
0948		C	PWB ASSY FP I/F Same as Items 0152 — 0164			
0949		C	CA ASSY CONF JPR Same as Items 0165 — 0168			
0950		C	SCREW — Same as Item 0169			
0951		C	KEPNUT — Same as Item 0170			
0952		C	NAMEPLATE — Same as Item 0788			
0953		C	KEPNUT — Same as Item 0172			
0954		C	CA ASSY MULTIBUS FP Same as Items 0173 — 0178			
0955		C	LOCTITE — Same as Item 0179			
0956	7A3	B	PWR ASSY (1) MULTI Same as Item 0792			
0957		C	PWR CHASSIS — Same as Item 0225			
0958		C	PWR SUPPORT — Same as Item 0226			
0959		C	PANEL P/S SIN — Same as Item 0796			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0960		C	CA ASSY PS MV DC Same as Items 0228 — 0240			
0961		C	CA ASSY PS MV TX Same as Items 0318 — 0325			
0962		C	PWR ASSY 12 V dc Same as Items 0276 — 0303			
0963		C	HANDLES — Same as Item 0317			
0964		C	CA ASSY CB — Same as Items 0304 — 0316			
0965		C	SCREW — Same as Item 0275			
0966		C	PWR ASSY 5 V (1) MULTI Same as Items 0241 — 0274			
0967		D	RES — Same as Item 0804			
0968		C	SCREW — Same as Item 0326			
0969		C	WASHER — Same as Item 0327			
0970		C	WIRING DIAG — Same as Item 0807			
0971	7A5, A6	B	BC TOP ASSY — Same as Items 0184 — 0223 and Items 1104 through 1143 for A1 — A16 Bus Connector board parts breakdown			
0972	7A4	B	PWR ASSY (2) SIN — Same as Item 0392			
0973		C	PWR CHASSIS — Same as Item 0225			
0974		C	PWR SUPPORT — Same as Item 0226			
0975		C	PANEL PS DUAL — Same as Item 0227			
0976		C	CA ASSY AC REAR — Same as Item 0396			
0977		D	CONN — Same as Item 0229			
0978		D	CONN — Same as Item 0338			
0979		D	WIRE BLACK — Same as Item 0368			
0980		D	WIRE WHITE — Same as Item 0246			
0981		D	WRAP-IT — Same as Item 0099			
0982		D	CONN — Same as Item 0232			
0983		D	MARKER PLATE — Same as Item 0100			
0984		C	PWR ASSY DC — Same as Item 0404			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
0985		D	PWR 5 V 12 A — Same as Item 0405			
0986		D	CA ASSY PS — Same as Item 0406			
0987		E	CONN — Same as Item 0244			
0988		E	CONN — Same as Item 0230			
0989		E	WIRE BLACK — Same as Item 0368			
0990		E	WIRE WHITE — Same as Item 0246			
0991		E	WRAP-IT — Same as Item 0099			
0992		E	MARKER PLATE — Same as Item 0100			
0993		D	CA ASSY PS — Same as Item 0413			
0994		E	CONN — Same as Item 0261			
0995		E	CONN — Same as Item 0232			
0996		E	CONN — Same as Item 0273			
0997		E	WIRE BLACK — Same as Item 0368			
0998		E	WIRE VIOLET — Same as Item 0235			
0999		E	WIRE ORANGE — Same as Item 0237			
1000		E	WIRE RED — Same as Item 0238			
1001		E	WRAP-IT — Same as Item 0099			
1002		E	MARKER PLATE — Same as Item 0100			
1003		D	STANDOFF — Same as Item 0250			
1004		D	COVER PS (S/V) — Same as Item 0251			
1005		D	SCREW — Same as Item 0252			
1006		D	SCREW — Same as Item 0253			
1007		D	WASHER — Same as Item 0254			
1008		D	WASHER SPLIT — Same as Item 0255			
1009		D	NUT — Same as Item 0256			
1010		D	GRMT — Same as Item 0257			
1011		D	BRACKETS — Same as Items 0258 — 0259			
1012		D	WRAP-IT — Same as Item 0099			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1013		D	RES — Same as Item 0049			
1014		C	CA ASSY PS MV DC Same as Items 0228 — 0240			
1015		C	SCREW HH — Same as Item 0275			
1016		C	CA ASSY CB — Same as Item 0436			
1017		D	CIRCUIT BRKR — Same as Item 0305			
1018		D	CONN — Same as Item 0244			
1019		D	CONN — Same as Item 0263			
1020		D	WIRE BLACK — Same as Item 0233			
1021		D	WIRE RED — Same as Item 0119			
1022		D	WIRE BLACK — Same as Item 0118			
1023		D	WRAP-IT — Same as Item 0099			
1024		D	CONN — Same as Item 0230			
1025		D	MARKER PLATE — Same as Item 0100			
1026		D	SLVG 1/8 — Same as Item 0312			
1027		D	SLVG 1/4 — Same as Item 0311			
1028		C	HANDLES — Same as Item 0317			
1029		C	SCREW — Same as Item 0252			
1030		C	SCREW — Same as Item 0253			
1031		C	WASHER — Same as Item 0327			
1032		C	WIRING DIAG — Same as Item 0452			
1033	7A7	B	FAN ASSEMBLY DUAL — Same as Item 0868			
1034		C	CA ASSY FAN — Same as Items 0330 — 0336			
1035		C	DUAL FAN ASSEMBLY — Same as Item 0870			
1036		C	CONN — Same as Item 0338			
1037		C	CONN — Same as Item 0339			
1038		C	KEPNUT — Same as Item 0340			
1039		C	WIRING DIAG FAN — Same as Item 0874			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1040		B	CAB RFI — Same as Item 0875			
1041		C	CAB RFT STAND Same as Items 0382 — 0390			
1042	7A9	B	AC DIST PANEL ASSY Same as Items 0342 — 0368			
1043		B	CA ASSY LAN Same as Items 0500 — 0513			
1044		B	CA ASSY RCU MODEM Same as Items 0879 — 0883			
1045		C	MARKER PLATE — Same as Item 0100			
1046		C	WRAP-IT — Same as Item 0099			
1047		C	STANDOFF — Same as Item 0214			
1048		C	KEPNUT — Same as Item 0093			
1049		B	CA ASSY MULTIBUS — Same as Item 0468			
1050		C	CONN — Same as Item 0229			
1051		C	CONN — Same as Item 0230			
1052		C	CONN — Same as Item 0471			
1053		C	KEY — Same as Item 0472			
1054		C	WIRE — Same as Items 0233 — 0238			
1055		C	WRAP-IT — Same as Item 0099			
1056		C	MARKER PLATE — Same as Item 0100			
1057		C	CONN SPLICE — Same as Item 0481			
1058		C	CONN — Same as Item 0363			
1059		C	SLVG 3/16 — Same as Item 0483			
1060		B	CA ASSY BC CARD Same as Items 0484 — 0499			
1061		B	CAE ASSY AC — Same as Items 0514 — 0520			
1062		B	KIT — Same as Item 0901			
1063		C	HOUSING — Same as Item 0902			
1064		C	GASKET — Same as Item 0523			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1065		C	GUIDE — Same as Item 0904			
1066		C	KIT HDWR — Same as Items 0525 — 0542			
1067		C	SCREW — Same as Item 0906			
1068		C	SCREW, PHPH — Same as Item 0544			
1069		C	SCREW, CABLE — Same as Item 0545			
1070		C	CONN RING LUG — Same as Item 0910			
1071		C	NUT — Same as Item 0547			
1072		C	WASHER — Same as Item 0548			
1073		C	WASHER SPLIT — Same as Item 0255			
1074		C	SCREW — Same as Item 0560			
1075		C	KEPNUT — Same as Item 0561			
1076		B	BRACKET — Same as Items 0550 — 0552			
1077		B	KIT DRAWING, RCU EXPANDED	65519	F79001970	
1078		B	HDWR ITEMS — Same as Items 0555 — 0565			
1079		B	SCREW — Same as Item 0275			
1080		B	WRAP-IT — Same as Item 0099			
1081		B	WIRING DIAG RCU (EXP) CABINET	65519	F83000224	
1082		B	CA ASSY LAN — Same as Items 0568 — 0575			
1083		B	NAMEPLATE — Same as Item 0921			
1084		B	NAMEPLATE — Same as Item 0577			
1085		B	ADHESIVE — Same as Item 0578			
1086	7A2A2A2	B	PWB ASSY 16 K — Same as Item 0924			
1087	R1-R7	C	RES — Same as Item 0052			
1088	C16, C17	C	CAP — Same as Item 0926			
1089	C1-C13	C	CAP — Same as Item 0055			
1090	U13	C	IC — Same as Item 0928			
1091	U8	C	IC — Same as Item 0024			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1092	U3, U9	C	IC — Same as Item 0037			
1093	U4, U5	C	IC — Same as Item 0038			
1094	U2	C	IC — Same as Item 0157			
1095	U1, U10, U11, U12	C	IC — Same as Item 0029			
1096		C	CONN — Same as Item 0934			
1097	DS1, DS2	C	LED GREEN — Same as Item 0054			
1098		C	CARD EJTR — Same as Item 0062			
1099		C	PWB RCU MEM EXP — Same as Item 0937			
1100		C	SOCKET — Same as Item 0064			
1101		C	CONN — Same as Item 0939			
1102		C	CONN — Same as Item 0014			
1103		C	SCHEMATIC 16 K — Same as Item 0941			
1104	A1-A16	C	PWB ASSY BUS CONN BD — ENH	65519	F60002540	
1105	U8, U14	D	IC 74HC367J/54HC367J — FC	01295	F17007040	
1106	U3	D	IC 74HC373J/54HC373J DTYPE F/F	01295	F17005943	
1107	S2	D	SW 7 POS DIP	00520	F20000584	
1108	U1	D	IC D8031AH CERAMIC 8BIT MICRO	34649	F17006388	
1109	Y1	D	OSC 11.059MHZ M-TRON	10144	F22000806	
1110	U6	D	IC HM6264LP-12 CERAMIC CMOS RAM	12830	F17006404	
1111	U5	D	OC Z8530 SERIAL COMM CONTR	81349	F17005877	
1112	U13	D	IC 75150J DUAL LINE DRIVER	01295	F17005885	
1113	U7	D	IC 75189AJ CERAM QUAD LN RCVR	12830	F17006362	
1114	U4	D	IC D2764A CERAMIC 8KX8 UV		F17006370	
1115	U15	D	IC 74HC00J/54HC00J QUAD/2 NAND	01295	F17006255	
1116	U10	D	IC 74HC4020J/54HC4020J CNTR	81349	F17006305	
1117	U11	D	IC 75157J CERAMIC DUAL LN RCVR	07263	F17006313	
1118	U12	D	IC 75158J CERAMIC DUAL LN DRIVER	81349	F17006321	
1119	U9	D	IC 74HC123J/54HC123J DUAL RTRG	01295	F17005976	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1120	C3-C10, C17	D	CAP .1UF 50 V 923CZ5U104M050B	81349	F15002686	
1121	C1	D	CAP 10UF 20 V 150D106X9020B2	81349	F15001282	
1122	C13, C14	D	CAP 10UF 25 V 500D106G025BB7	81349	F15000409	
1123	C11, C12	D	CAP 1500PF CK05BX152M KEMET	03200	F15000417	
1124	C15, C16	D	CAP 100PF CK05BX101M KEMET	03200	F15000425	
1125	C2	D	CAP 100UF 10 V T392E107M010AS	81349	F15000433	
1126	CR1-CR4	D	DIODE IN4148	09295	F11000239	
1127	I1-I3	D	LED 555-2303 DIALCO GREEN	05200	F21000161	
1128	CR5, CR6	D	DIODE IN5820	07263	F11000051	
1129	RN1	D	RESP 10 K CTS750-81-R10K	12569	F14000921	
1130	RN2, RN3	D	RESP 5.6 K 6A562	34095	F14001770	
1131	R2, R3	D	RES 100 K 1/4 W 5% RC07GF104J	81349	F14000848	
1132	R4	D	RES 100 OHM 1/4 W 5% RC07GF101J	81349	F14000855	
1133	R1	D	RES 8.2 K 5% 1/4 W RC07GF822J	81349	F14000954	
1134	E4-E9	D	CONN 2X6 CA-D06SP100-230X-455	04187	F23001555	
1135	P1	D	CONN 34P R ANDLE HDR 65461-006	95871	F23001563	
1136	E1	D	CONN 1X2 CA-S02SP100-230X-455	04187	F23001571	
1137	E2, E3	D	CONN 1X3 CA-S03SP100-230X-455	04187	F23001589	
1138	S1	D	SW 2 POS 573-H PC MONT TOGGLE	00520	F19000348	
1139	E1, E3, E6	D	CONN 2 POS JMPR BERG 65474-002		F23001597	
1140	F1, F2	D	PICOFUSE 2A	01298	F24000465	
1141		D	PWB-PWM BUS CONN BD — ENH	65519	F76001627	
1142		D	SCHEM BUS CONN BD — ENH	65519	F75001552	
1143	U2	D	IC AMPAL16R4 AMD — FC		F17007030	
1144		A	RFSP ASSEMBLY	65519	F64001019	
1145		B	PRINTER CENTRONICS MODEL	50163	F52000577	
1146		B	RIBBON CASSETTE	50163	F52002060	
1147		B	RIBBON CASSETTE	65519	F52002600	
1148		B	COVER ASSEMBLY, PRINTER	65519	F64000961	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1149		C	SUBASSEMBLY, PRINTER COVER	65519	F64001068	
1150		D	COVER PRINTR, 64003085-200	50163	F41000472	
1151		D	INSERT ADHESIVE BONDED	N/A	F64000144	
1152		E	INSERT PRINTER COVER	65519	F82000222	
1153		E	WINDOW PRINTER COVER	65519	F82000144	
1154		E	ADHESIVE SUPERBONDER 4205	N/A	F49000222	
1155		E	ADHESIVE ACCELERATOR	N/A	F49000144	
1156		D	FASTENER, PUSH-ON TYPE, .12	89032	F42000497	
1157		C	LAMP	N/A	F21000252	
1158		C	INVERTER	N/A	F29000213	
1159		C	ADHESIVE, DEVCON, 5-MIN EPO	N/A	F49001134	
1160		C	MOUNT, CABLE TIE — FC	06915	F49001142	
1161		C	WRAP-IT — Same as Item 0099			
1162		C	CONN HOUSING 3POS	00779	F23008238	
1163		C	CONN TERM PIN	00779	F26001651	
1164		C	WIRE 20AWG UL 1007 WHITE	09047	F28000958	
1165		C	ADHESIVE, DOW CORNING — FC	N/A	F49001217	
1166		B	LOGO PLATE, PRINTER	65519	F74000266	
1167		B	NAMEPLATE, RFSP	65519	F74000522	
1168		B	ADHESIVE — Same as Item 0578			
1169		A	CATHODE RAY TUBE ASSEMBLY	65519	F64001001	
1170		B	CRT DISPLAY FAME 111 MOD	07002	F52000569	
1171		B	LOGO PLATE, CRT	65519	F74000258	
1172		B	NAMEPLATE, CRT	65519	F74000548	
1173		B	SCREW — Same as Item 0094			
1174		B	KEPNUT — Same as Item 0093			
1175		B	DRILL TEMPLATE-CRT	65519	F49001001	
1176		A	RANK TOP ASSY	65519	F64000565	
1177		B	HOUSING, KEYBOARD	65519	F82000449	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1178		B	WELDMENT, FRONT PANEL/COVE	65519	F82001058	
1179		B	REAR PANEL, KEYBOARD	65519	F82000423	
1180		B	SUPPORT, KEYBOARD, RH	65519	F82000464-001	
1181		B	SUPPORT, KEYBOARD, LH	65519	F82000464-002	
1182		B	BRACKET POTENTIOMETER	65519	F82001066	
1183		B	NAMEPLATE, RANK	65519	F74000530	
1184		B	RANK KEYBOARD	00685	F52000544	
1185		C	KEY LAMP	55335	F21000237	
1186		C	MWL LAMP	55335	F21000260	
1187		B	PWR SUPPLY	54407	F51000461	
1188		B	FILTER — Same as Item 0347			
1189		B	BRACKET POWER SUPPLY	65519	F82001074	
1190		B	BRACKET, KEYBOARD HSG	65519	F82000472	
1191		B	KEPNUT — Same as Item 0172			
1192		B	CABLE ASSY KBD INTRNL DAT	65519	F62002555	
1193		C	CONN 26 POS	95871	F23007776	
1194		C	CONN — Same as Item 0116			
1195		C	CABLE 2TWPR 24AWG SHIELD	65519	F28000933	
1196		C	CONN D 25 PIN SOCKET	13556	F23001928	
1197		C	CONN CONTACT SOCKET	13556	F23009095	
1198		C	MARKER PLATE — Same as Item 0100			
1199		C	WRAP-IT — Same as Item 0099			
1200		B	CONN SWG SHELL	13556	F23007883	
1201		B	STRAIN RELIEF, HH SMITH 82	83330	F49000854	
1202		B	CABLE ASSY KYBD AC EXTRNL	65519	F62002563	
1203		C	CA PS — Same as Item 0331			
1204		C	CONN RING LUG — Same as Item 0910			
1205		C	CONN — Same as Item 0363			
1206		C	MARKER PLATE — Same as Item 0100			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1207		C	WRAP-IT — Same as Item 0099			
1208		B	CABLE ASSY KYBD AC INTRNL	65519	F62002571	
1209		C	WIRE BLACK — Same as Item 0233			
1210		C	WIRE WHITE — Same as Item 0246			
1211		C	CONN RING LUG — Same as Item 0910			
1212		C	WRAP-IT — Same as Item 0099			
1213		B	BUMPER, HH SMITH 2451 — FC	83330	F49000987	
1214		B	CRKT BRK, 2AMP	73135	F24000473	
1215		B	CABLE ASSY KYBD DC	65519	F62002589	
1216		C	CONN 4 POS MOLX	27264	F23007925	
1217		C	CONN 8 POS MOLX	27264	F23007933	
1218		C	WIRE RED — Same as Item 0238			
1219		C	WIRE BLACK — Same as Item 0233			
1220		C	WIRE BLUE — Same as Item 0234			
1221		C	MARKER PLATE — Same as Item 0100			
1222		C	WRAP-IT — Same as Item 0099			
1223		B	CABLE ASSY KBD AC BKR/FLT	65519	F62002597	
1224		C	WIRE BLACK — Same as Item 0233			
1225		C	CONN RING LUG Same as Item 0910			
1226		C	CONN — Same as Item 0363			
1227		C	MARKER PLATE — Same as Item 0100			
1228		C	WRAP-IT — Same as Item 0099			
1229		B	POTENTIOMETER ASSY KYBD	65519	F64001050	
1230		C	POT. 2K	90201	F14001796	
1231		C	KNOB, ALCO KN-500-1/4 — FC	00330	F49000995	
1232		C	WIRE BLACK — Same as Item 0118			
1233		C	WIRE RED — Same as Item 0119			
1234		C	CONN QDLG FEM 22-18AWG .1	06383	F26001628	
1235		C	SLVG 1/8 BLACK — Same as Item 0312			

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1236		B	SCREW PAN HEAD 6-32X1/4 L	01608	F47004221	
1237		B	SCREW — Same as Item 0094			
1238		B	NUT — Same as Item 0090			
1239		B	WASHER — Same as Item 0254			
1240		B	LOCK SCREW ASSY TRW D 204	91934	F47000278	
1241		B	SCREW — Same as Item 0375			
1242		B	WASHER — Same as Item 0388			
1243		B	INTERCONNECTION DIAGRAM, R	65519	F83000273	
1244		B	WASHER — Same as Item 0114			
1245		B	WASHER SPLIT ZINC PLATED	01608	F48000327	
1246		A	CBL ASSY PERIPH RS422 50 FT.	65519	F62001896-001	
1247		A	CBL ASSY PERIPH RS422 75 FT.	65519	F62001896-002	
1248		A	CBL ASSY PERIPH RS422 100 FT.	65519	F62001896-003	
1249		A	CBL ASSY PERIPH RS422 125 FT.	65519	F62001896-004	
1250		A	CBL ASSY PERIPH RS422 150 FT.	65519	F62001896-005	
1251		A	CBL ASSY PERIPH RS422 175 FT.	65519	F62001896-006	
1252		A	CBL ASSY PERIPH RS422 200 FT.	65519	F62001896-007	
1253		A	CBL ASSY PERIPH RS422 225 FT.	65519	F62001896-008	
1254		A	CBL ASSY PERIPH RS422 250 FT.	65519	F62001896-009	
1255		A	CBL ASSY PERIPH RS422 275 FT.	65519	F62001896-010	
1256		A	CBL ASSY PERIPH RS422 300 FT.	65519	F62001896-011	
1257		A	CBL ASSY PERIPH RS422 350 FT.	65519	F62001896-012	
1258		A	CBL ASSY PERIPH RS422 400 FT.	65519	F62001896-013	
1259		A	CBL ASSY PERIPH RS422 450 FT.	65519	F62001896-014	
1260		A	CBL ASSY PERIPH RS422 500 FT.	65519	F62001896-015	
1261		A	CBL ASSY PERIPH RS422 1000 FT.	65519	F62001896-016	
1262		A	CBL ASSY PERIPH RS422 1500 FT.	65519	F62001896-017	
1263		A	CBL ASSY PERIPH RS422 2000 FT.	65519	F62001896-018	
1264		A	CBL ASSY PERIPH RS422 2500 FT.	65519	F62001896-019	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1265		A	CBL ASSY PERIPH RS422 3000 FT.	65519	F62001896-020	
1266		A	CBL ASSY PERIPH RS422 3500 FT.	65519	F62001896-021	
1267		A	CBL ASSY PERIPH RS422 4000 FT.	65519	F62001896-022	
1268		A	CBL ASSY GPI IF.360 50 FT.	65519	F62001797-001	
1269		A	CBL ASSY GPI IF.360 75 FT.	65519	F62001797-002	
1270		A	CBL ASSY GPI IF.360 100 FT.	65519	F62001797-003	
1271		A	CBL ASSY GPI IF.360 125 FT.	65519	F62001797-004	
1272		A	CBL ASSY GPI IF.360 150 FT.	65519	F62001797-005	
1273		A	CBL ASSY GPI IF.360 175 FT.	65519	F62001797-006	
1274		A	CBL ASSY GPI IF.360 200 FT.	65519	F62001797-007	
1275		A	CBL ASSY GPI IF.360 225 FT.	65519	F62001797-008	
1276		A	CBL ASSY GPI IF.360 250 FT.	65519	F62001797-009	
1277		A	CBL ASSY GPI IF.360 275 FT.	65519	F62001797-010	
1278		A	CBL ASSY GPI IF.360 300 FT.	65519	F62001797-011	
1279		A	CBL ASSY GPO IF.360 50 FT.	65519	F62002274-001	
1280		A	CBL ASSY GPO IF.360 75 FT.	65519	F62002274-002	
1281		A	CBL ASSY GPO IF.360 100 FT.	65519	F62002274-003	
1282		A	CBL ASSY GPO IF.360 125 FT.	65519	F62002274-004	
1283		A	CBL ASSY GPO IF.360 150 FT.	65519	F62002274-005	
1284		A	CBL ASSY GPO IF.360 175 FT.	65519	F62002274-006	
1285		A	CBL ASSY GPO IF.360 200 FT.	65519	F62002274-007	
1286		A	CBL ASSY GPO IF.360 225 FT.	65519	F62002274-008	
1287		A	CBL ASSY GPO IF.360 250 FT.	65519	F62002274-009	
1288		A	CBL ASSY GPO IF.360 275 FT.	65519	F62002274-010	
1289		A	CBL ASSY GPO IF.360 300 FT.	65519	F62002274-011	
1290		A	CBL ASSY MODEM RS232 50 FT.	65519	F62001904-001	
1291		A	CBL ASSY MODEM RS232 75 FT.	65519	F62001904-002	
1292		A	CBL ASSY MODEM RS232 100 FT.	65519	F62001904-003	
1293		A	CBL ASSY MODEM RS232 125 FT.	65519	F62001904-004	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1294		A	CBL ASSY MODEM RS232 150 FT.	65519	F62001904-005	
1295		A	CBL ASSY MODEM RS232 175 FT.	65519	F62001904-006	
1296		A	CBL ASSY MODEM RS232 200 FT.	65519	F62001904-007	
1297		A	CBL ASSY MODEM RS232 225 FT.	65519	F62001904-008	
1298		A	CBL ASSY MODEM RS232 250 FT.	65519	F62001904-009	
1299		A	CBL ASSY MODEM RS232 275 FT.	65519	F62001904-010	
1300		A	CBL ASSY MODEM RS232 300 FT.	65519	F62001904-011	
1301		A	CBL ASSY MODEM RS232 350 FT.	65519	F62001904-012	
1302		A	CBL ASSY MODEM RS232 400 FT.	65519	F62001904-013	
1303		A	CBL ASSY MODEM RS232 450 FT.	65519	F62001904-014	
1304		A	CBL ASSY MODEM RS232 500 FT.	65519	F62001904-015	
1305		A	CBL ASSY RCU-MODEM EXT 25 FT.	65519	F62002282-001	
1306		A	CBL ASSY RCU-MODEM EXT 50 FT.	65519	F62002282-002	
1307		A	CBL ASSY RCU-MODEM EXT 75 FT.	65519	F62002282-003	
1308		A	CBL ASSY RCU-MODEM EXT 100 FT.	65519	F62002282-004	
1309		A	CBL ASSY RCU-MODEM EXT 150 FT.	65519	F62002282-005	
1310		A	CBL ASSY RCU-MODEM EXT 200 FT.	65519	F62002282-006	
1311		A	CBL ASSY RCU-MODEM EXT 250 FT.	65519	F62002282-007	
1312		A	CBL ASSY RCU-MODEM EXT 300 FT.	65519	F62002282-008	
1313		A	VIDEO DISPLAY	07002	ANSI/S-11-100A	
1314		A	DOT MATRIX PRINTER	0R905	DZ-9034-3	
1315		A	PRINTER, ADP	96587	IER 512C-FSP	
1316		A	PRINTHEAD, Thermal 80mm	96587	S30350A	
1317		C	PRINTER FUSE	—	19181-124	
1318		C	RETAINING RING	07FA1	5502010	
1319		B	DISPENSER BOX	08125	S81782A	
1320		B	OUTPUT STACKER	08125	P31816A	
1321		A	TOUCHSTONE KEYBOARD	48707	18274	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1322		A	ADDS VIDEO DISPLAY	OPF98	F21671097100	
1323		A	APC SURGE PROTECTOR	O67S1	NET9RM	
1324		A	KEYCAP 1X1 PRNTD, F1	48707	KEYFDIO-FI	
1325		A	KEYCAP 1X1 PRNTD, F2	48707	KEYFDIO-F2	
1326		A	KEYCAP 1X1 PRNTD, F3	48707	KEYFDIO-F3	
1327		A	KEYCAP 1X1 PRNTD, F4	48707	KEYFDIO-F4	
1328		A	KEYCAP 1X1 PRNTD, F5	48707	KEYFDI0-F5	
1329		A	KEYCAP 1X1 PRNTD, F6	48707	KEYFDIO-F6	
1330		A	KEYCAP 1X1 PRNTD, F7	48707	KEYFDIO-F7	
1331		A	KEYCAP 1X1 PRNTD, F8	48707	KEYFDIO-F8	
1332		A	KEYCAP 1X1 PRNTD, F9	48707	KEYFDI0-F9	
1333		A	KEYCAP 1X1 PRNTD, F10	48707	KEYFDIO-F10	
1334		A	KEYCAP 1X1 PRNTD, F11	48707	KEYFDIO-F11	
1335		A	KEYCAP 1X1 PRNTD, F12	48707	KEYFDIO-F12	
1336		A	KEYCAP 1X1 PRNTD, CRCLD+	48707	KEYFDIO-CRCLPLS	
1337		A	KEYCAP 1X1 PRNTD, 1	48707	KEYFDIO-1	
1338		A	KEYCAP 1X1 PRNTD, 2	48707	KEYFDIO-2	
1339		A	KEYCAP 1X1 PRNTD, 3	48707	KEYFDIO-3	
1340		A	KEYCAP 1X1 PRNTD, 4	48707	KEYFDIO-4	
1341		A	KEYCAP 1X1 PRNTD, 5	48707	KEYFDIO-5	
1342		A	KEYCAP 1X1 PRNTD, 6	48707	KEYFDIO-6	
1343		A	KEYCAP 1X1 PRNTD, 7	48707	KEYFDIO-7	
1344		A	KEYCAP 1X1 PRNTD, 8	48707	KEYFDI0-8	
1345		A	KEYCAP 1X1 PRNTD, 9	48707	KEYFDIO-9	
1346		A	KEYCAP 1X1 PRNTD, 0	48707	KEYFDIO-0	
1347		A	KEYCAP 1X1 PRNTD, -	48707	KEYFDIO-MINUS	
1348		A	KEYCAP 1X1 PRNTD, +	48707	KEYFDIO-PLUS	
1349		A	KEYCAP 1X1 PRNTD, DIM	48707	KEYFDIO-DIM	
1350		A	KEYCAP 1X1 PRNTD, BRIGHT	48707	KEYFDIO-BRIGHT	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1351		A	KEYCAP 1X1 PRNTD, CIRCLE	48707	KEYFDIO-CIRCLE	
1352		A	KEYCAP 1X1 PRNTD, Q	48707	KEYFDIO-Q	
1353		A	KEYCAP 1X1 PRNTD, W	48707	KEYFDIO-W	
1354		A	KEYCAP 1X1 PRNTD, E	48707	KEYFDIO-E	
1355		A	KEYCAP 1X1 PRNTD, R	48707	KEYFDIO-R	
1356		A	KEYCAP 1X1 PRNTD, T	48707	KEYFDIO-T	
1357		A	KEYCAP 1X1 PRNTD, Y	48707	KEYFDIO-Y	
1358		A	KEYCAP 1X1 PRNTD, U	48707	KEYFDIO-U	
1359		A	KEYCAP 1X1 PRNTD, I	48707	KEYFDIO-I	
1360		A	KEYCAP 1X1 PRNTD, O	48707	KEYFDIO-O	
1361		A	KEYCAP 1X1 PRNTD, P	48707	KEYFDIO-P	
1362		A	KEYCAP 1X1 PRNTD, @	48707	KEYFDIO-@	
1363		A	KEYCAP 1X1 PRNTD, BACKSPACE	48707	KEYFDIO-BACKSPO	
1364		A	KEYCAP 1X1 PRNTD, LINE INS	48707	KEYFDIO-LINEINS	
1365		A	KEYCAP 1X1 PRNTD, CLRSCRN	48707	KEYFDIO-CLRSCRN	
1366		A	KEYCAP 1X1 PRNTD, LINE DEL	48707	KEYFDIO-LINEDEL	
1367		A	KEYCAP 1X1 PRNTD, TAB L	48707	KEYFDIO-TABL	
1368		A	KEYCAP 1X1 PRNTD, TAB R	48707	KEYFDIO-TABR	
1369		A	KEYCAP 1X1 PRNTD, A	48707	KEYFDIO-A	
1370		A	KEYCAP 1X1 PRNTD, S	48707	KEYFDIO-S	
1371		A	KEYCAP 1X1 PRNTD, D	48707	KEYFDIO-D	
1372		A	KEYCAP 1X1 PRNTD, F	48707	KEYFDIO-F	
1373		A	KEYCAP 1X1 PRNTD, G	48707	KEYFDIO-G	
1374		A	KEYCAP 1X1 PRNTD, H	48707	KEYFDIO-H	
1375		A	KEYCAP 1X1 PRNTD, J	48707	KEYFDIO-J	
1376		A	KEYCAP 1X1 PRNTD, K	48707	KEYFDIO-K	
1377		A	KEYCAP 1X1 PRNTD, L	48707	KEYFDIO-L	
1378		A	KEYCAP 1X1 PRNTD, DWNARR	48707	KEYFDIO-ARROWDWN	
1379		A	KEYCAP 1X1 PRNTD, UPARROW	48707	KEYFDIO-ARROWUP	

Item Number	Ref Desig.	Ind. Let.	Name of Part/ Description	Mfrs. Code Number	Mfrs. Part Number	Notes
1380		A	KEYCAP 1X1 PRNTD, CHAR INS	48707	KEYFDIO-CHARINS	
1381		A	KEYCAP 1X1 PRNTD, CHAR DEL	48707	KEYFDIO-CHARDEL	
1382		A	KEYCAP 1X1 PRNTD, SHIFT	48707	KEYFDIO-SHIFT	
1383		A	KEYCAP 1X1 PRNTD, Z	48707	KEYFDIO-Z	
1384		A	KEYCAP 1X1 PRNTD, X	48707	KEYFDIO-X	
1385		A	KEYCAP 1X1 PRNTD, C	48707	KEYFDIO-C	
1386		A	KEYCAP 1X1 PRNTD, V	48707	KEYFDIO-V	
1387		A	KEYCAP 1X1 PRNTD, B	48707	KEYFDIO-B	
1388		A	KEYCAP 1X1 PRNTD, N	48707	KEYFDIO-N	
1389		A	KEYCAP 1X1 PRNTD, M	48707	KEYFDIO-M	
1390		A	KEYCAP 1X1 PRNTD, STAR	48707	KEYFDIO-STAR	
1391		A	KEYCAP 1X1 PRNTD, DECIMAL	48707	KEYFDIO-DECIMAL	
1392		A	KEYCAP 1X1 PRNTD, SLASH	48707	KEYFDIO-SLASH	
1393		A	KEYCAP 1X1 PRNTD, LEFT ARR	48707	KEYFDIO-ARRWLFT	
1394		A	KEYCAP 1X1 PRNTD, HOME	48707	KEYFDIO-HOME	
1395		A	KEYCAP 1X1 PRNTD, RGT ARR	48707	KEYFDIO-ARRWRGT	
1396		A	KEYCAP 1X1 PRNTD, FIELD DEL	48707	KEYFDIO-FLDDEL	
1397		A	KEYCAP 1X1 PRNTD, VER	48707	KEYFDIO-VER	
1398		A	KEYCAP 1X1 PRNTD, CANCEL	48707	KEYFDIO-CANCEL	
1399		A	KEYCAP 1X1 BLANK	48707	KEYFDIO-BLANK	
1400		A	SPACEBAR 1X8 BLANK BLANK	48707	KEYFDIO-SPACBAR	
1401		A	KEYCAP 1X1-1/2 PRNTD CTRL	48707	KEYFDIO-CONTROL	
1402		A	KEYCAP 1X1-1/2 PRNTD NWLN	48707	KEYFDIO-NEWLINE	
1403		A	KEYCAP 1X2 V PRNTD, ENTER	48707	KEYFDIO-ENTER	
1404		A	KEYCAP REPLACEMENT KIT	48707	15190	
1405		A	KEYBOARD POWER SUPPLY	48707	15423	

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8.3 LIST OF MANUFACTURERS

Mfrs. Code Number	Manufacturer	Address
00779	Amp Inc.	Eisenhower Blvd. Harrisburg, PA 17105
01295	Texas Instruments Inc. Semiconductor Group	P. O. Box 5012 Central Expressway Dallas, TX 75222
01933	Kierulff Electronics Inc.	2585 Commerce Way Los Angeles, CA 90040
2777	Hopkins Engineering Co.	12900 Foothill Blvd. San Fernando, CA 91342
04222	AVX Ceramics Div. of AVX Corp.	19th Ave. South P.O. Box 867 Myrtle Beach, SC 29577
05236	Jonathon Mfg. Corp. Div. of Mite Corp.	1101 S. Acacia Ave. Fullerton, CA 92631
05574	Viking Connectors Inc. Sub of Criton Corp.	21001 Nordhoff St. Chatsworth, CA 91311
06383	Panduit Corp.	17301 Rigeland Tinely Park, IL 60477
06540	Amatom Electronic Hardware Div. of Mite Corp.	446 Blake St. New Haven, CT 06515
06915	Richco Plastic Co.	5825 N. Tripp Ave. Chicago, IL 60646
07002	Falco Data Products	440 Potrero Ave. Sunnyvale, CA 94086
07256	Silicon Transitor Corp.	Katrina Rd. — KSC Way Chelmsford, MA 01824
07261	Avnet Inc.	10916 Washington Blvd. Culver City, CA 90230
07764	Wyle Distribution Computer Products Div.	3200 Magruder Blvd. Hampton, VA 23666
08742	ACDC Electronics Div. of Emerson Elec. Co.	401 Jones Rd. Oceanside, CA 92054

Mfrs. Code Number	Manufacturer	Address
0R905	Diez Management Systems, Inc.	359 Saint Louis Ave. Egg Harbor City, NJ 08215
12556	TRW Cinch Connectors, Nuline	8821 Science Center Drive New Hope, MN 55428
14655	Cornell-Dublier Electronics	2640 Dalrymple Street Sanford, NC 27330
18324	Signetics Corp.	811 E. Argues Sunnyvale, CA 94086
18677	Scanbe Mfg. Co.	3445 Fletcher Ave. El Monte, CA 91731
25795	W. W. Grainger	5959 W. Howard St. Chicago, IL 60648
27014	National Semiconductor	2900 Semiconductor Dr. Santa Clara, CA 95051
27264	Molex Inc. Corporate HQ	2222 Wellington Court Lisle, IL 60532
30829	Samson Products	Ashland, N. E.
31433	Kemet, Union Carbide Corp. Electronics Div.	Hwy 276 S. E. Box 5928 Greenville, SC 29606
34649	Intel Corp.	3585 S. W. 198th Ave. Aloha, OR 97005
37942	Mallory Components Group	3029 E. Washington Box 706 Indianapolis, IN 46206
50163	Genicon/Centronics Data Computer	1 Wall St. Hudson, NH 03051
50507	Unitrode Corporation Micro Networks Division	324 York Street Worchester, MA 01606
51398	Mupac Corporation	646 Summer St. Brockton, MA 51398
53387	3M Electronic Products Div.	3M Center St. Paul, MN 55101

Mfrs. Code Number	Manufacturer	Address
54407	Power One Inc.	Power One Dr. Camarillo, CA 93010
56289	Sprague Electric Co.	125 Marshall St. North Adams, MA 01247
57921	Bourns Inc. Resistive Group	1200 Columbia Ave. Riverside, CA 92507
59993	International Rectifier Semi Conductor Division	233 Kansas Street El Segundo, CA 90245
65519	Federal Systems Group Inc. Division of Wespercorp	1821 East Dyer Rd. Santa Ana, CA 92705
71744	General Instruments Lamp Division	4433 N. Ravens Wood Ave. Chicago, IL 60640
72619	Dialight — Div. of Amperex Electronic Corp.	203 Harrison Pl. Brooklyn, NY 11237
74545	Harvey Hubbell Inc.	584 Derby Millford Rd. Orange, CT 06477
75915	Littlefuse Tractor Littlefuse	800 E Northwest Highway Des Plaines, IL 60016
81073	Grayhill Inc.	561 Hillgrove Ave. P.O. Box 373 La Grange, IL 60525
83330	H. H. Smith Inc.	812 Snekider Ave. Brooklyn, NY 11207
89709	Amphenol Electronics Corp.	2801 S. 25th Avenue Broadway, IL 60153
91833	Keystone Electronics Corp.	49 Blecker Street New York, NY 10012-3769
91929	Micro Switch Div. of Honeywell Inc.	11 W. Spring St. Freeport, IL 61032
94222	Southco	N. Brinton Lake Rd. Concordville, PA 19331

Mfrs. Code Number	Manufacturer	Address
96804	J. W. Miller Bell Industries	19070 Reyes Avenue Box 5825 Compton, CA 90224
92871	Berg Electronics	30 Hunter Lane Camp Hill, PA 17011
—	Acacia Sales Inc.	16592 Milliken Ave. Irvine, CA 92714
—	Aromat	250 Sheffield St. Moutainside, NJ 07092
—	Calif Conn & Cable	5285 Industrial Dr. Huntington Beach, CA 92649
—	Cal Switch	1317 Normandie Ave. Garden Grove, CA 90249
—	Components Direct Inc.	Suite 442 27001 La Paz Rd. Mission Viejo, CA 92671
08125	FAALC	6500 South McArthur Blvd. Oklahoma City, OK 73125
—	Hamilton Electro Sales	Dept. 4-1362 3170 Pullman St. Costa Mesa, CA 92626
—	Hitachi America Ltd.	175 Crossways Pk. W. Woodbury, NY 11797
07FA1	IER Inc.	4004 Beltline Rd. Suite 140, Dallas TX 75244
—	Irvine Fasteners	17982-A Sky Park Circle Irvine, CA 92714
—	JKL Components Corp.	2226 Barry Ave. Los Angeles, CA 90064
—	Mann Southwest	1980 E. McFadden Santa Ana, CA 90705
—	Northwest Electronics	217 Simpson Ave. McCleary, WA 98557

Mfrs. Code Number	Manufacturer	Address
—	Orange Precision Metal Fab	1831 W. Sequoia Orange, CA 92126
—	Sigma Circuits	2970 Airway Costa Mesa, CA 92626
—	Schweber Electronics	17811 Gillette Ave. Irvine, CA 92714
—	Standard Metal Products	1541 W. 132nd St. Gardena, CA 90249
—	Wickmann	4100 Shirley Dr. Atlanta, GA 30336
56708	Zilog Inc.	10340 Bubb Road Cupertino, CA 95014
96587	Print-O-Tape	P. O. Box 308 Libertyville, IL 60048-0308
48707	Touchstone Technology Inc.	955 Buffalo Road P. O. Box 24954 Rochester, NY 14624
OPF98	Boundless Technologies	100 Marcus Boulevard Hauppauge, NY 11788
O67S1	Cartridge Plus Inc.	220 Park Rd. Riva, MD 21140

9.0 INSTALLATION, INTEGRATION, AND CHECKOUT

9.1 INTRODUCTION

This section includes material directly related to the installation, integration, and checkout of the FDIO system. Figure 9-1 shows the location of ARTCC and ATCT sites.

9.2 SITE INFORMATION

Twenty-two ARTCC groups (including the William J. Hughes Technical Center and the Oklahoma City Academy) and 453 ATCT and Instrument Flight Rules (IFR) Rooms remote groups (including military sites) will be surveyed for FDIO equipment installation. These facilities will have an approved Final Site Survey Report with complete installation instructions and drawings containing required information for each individual site. Any special site configurations will be included in the Final Site Survey Report for each location. See table 9-1 for an example index of data found in each survey report.

9.3 INSTALLATION DRAWINGS

All data required to accomplish installation may be found in the FAA and Department of Defense (DOD) approved Final Site Survey Report and Installation Documentation package. Layout details for maintenance, operations area, communications/radar, ATCT TRACON, RAPCON, Ground Controlled Approach (GCA), Radar Air Traffic Control Facility (RATCF) are included in the Final Site Survey Report for each installation. Any space limitations will be referenced in the project deviations section of the survey report; clearance requirements are shown in the physical characteristics section. Facility requirements necessary for the installation of FDIO equipment are also defined in the survey report.

9.4 UNPACKING AND REPACKING

The contractor is responsible for the delivery, offloading, and placement of all FDIO equipment. RCU cabinets will be placed in their permanent locations at the time of arrival by carrier personnel. All other equipment arriving at the installation site will be unloaded from the motor carrier and held in secure storage in as close proximity as possible to the final installation area. Whenever possible, one pallet will contain all peripheral elements and cable containers per installation site requirements (some sites may require more than one pallet). All peripheral units will be unpacked by FSG, Inc. installation personnel. Occupational Safety and Health Administration (OSHA) safety procedures will be implemented during offloading and unpacking.

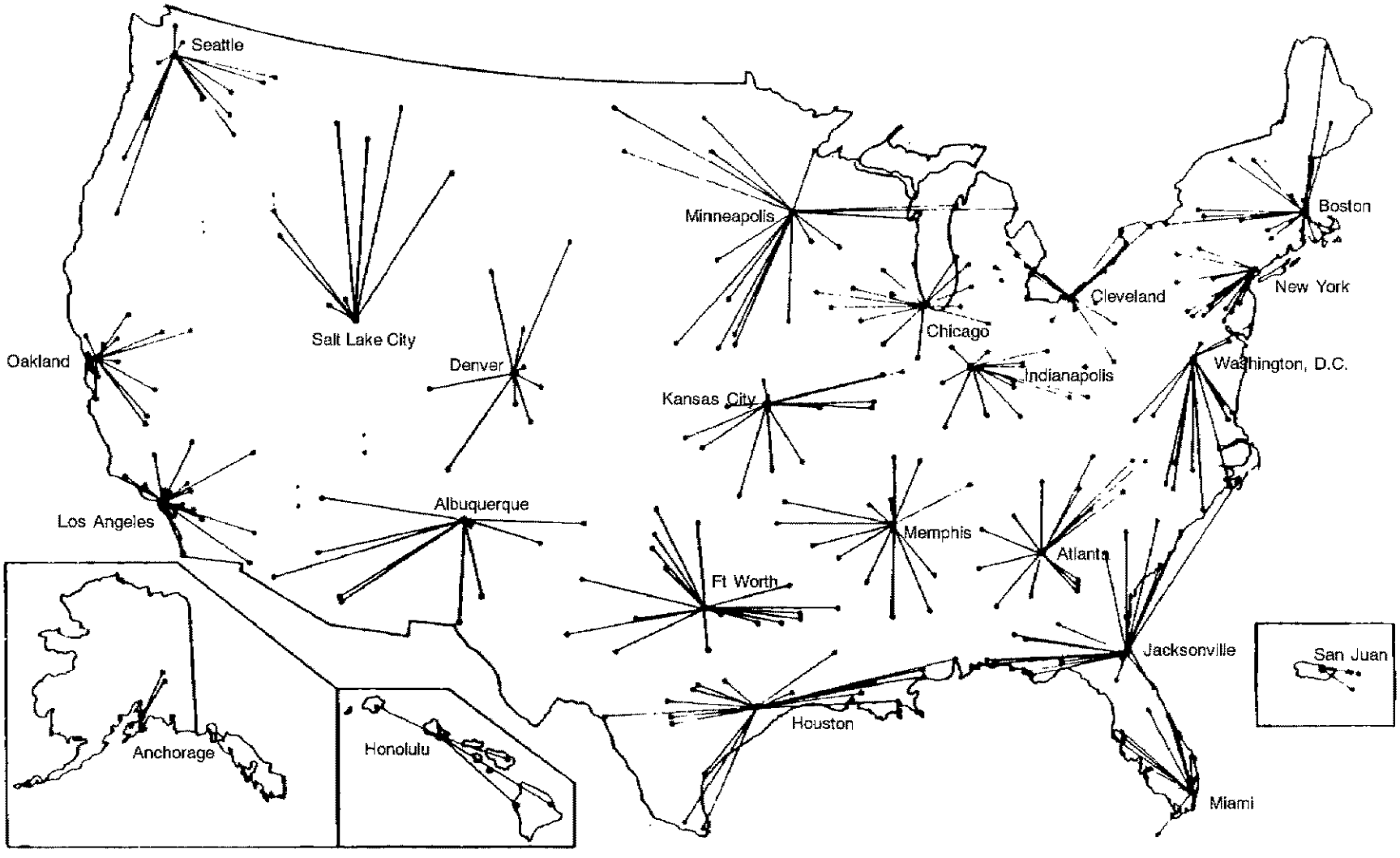

FIGURE 9-1. LOCATION MAP OF ARTCC AND ATCT SITES

TABLE 9-1. EXAMPLE INDEX OF DATA FOUND IN SITE SURVEY REPORTS

A.1	Equipment Room Floor Plan and Maintenance Area for BFL*
A.2	CAB Floor Plan for BFL
A.3	TRACON Console Layout for BFL
B.	FDIO Equipment List for BFL
C.1	Physical Characteristics of FDIO Equipment
C.2	Electrical Characteristics of FDIO Equipment
C.3	FDIO Power Panel Connection Electrical Requirements
D.1	FDIO Cable List for BFL
D.2	FDIO Cable Access Points
D.3	FDIO Cable Routing for BFL
E.1	FDIO Equipment Delivery and Placement Procedures for BFL
E.2	FDIO Equipment Test Requirements
E.3	FDIO Wiring Diagram for BFL
E.4	FDIO Cable Lengths for BFL
F.	Special FDIO Test Equipment
G.	Standard FDIO Test Equipment
H.1	FDIO Scheduling Requirements and Test Plans
H.2	FDIO Implementation Plans for BFL
I.	FDIO Administrative Support Requirements
J.	FDIO Project Support Requirements for BFL
K.	FDIO Project Deviations for BFL

*BFL denotes Bakersfield, CA

Cabinet assemblies and peripheral elements will be configured according to individual site requirements prior to shipping. All equipment in the cabinet assemblies will be securely installed before shipping. FDIO equipment will be shipped by padded van with the exception of Alaska, Hawaii, and Puerto Rico, where the equipment will be shipped via air freight.

9.4.1 Cabinet Packing and Unpacking

Hardware cabinets will be wrapped in conductive bubble wrap and covered with a cardboard container prior to shipping. These protective coverings will be removed by FSG, Inc. installation personnel. Figure 9-2 illustrates cabinet packing and unpacking.

WARNING

Hardware control cabinets weigh between 400-750 pounds each, depending on the configuration. Use extreme caution when moving or setting these units in place.

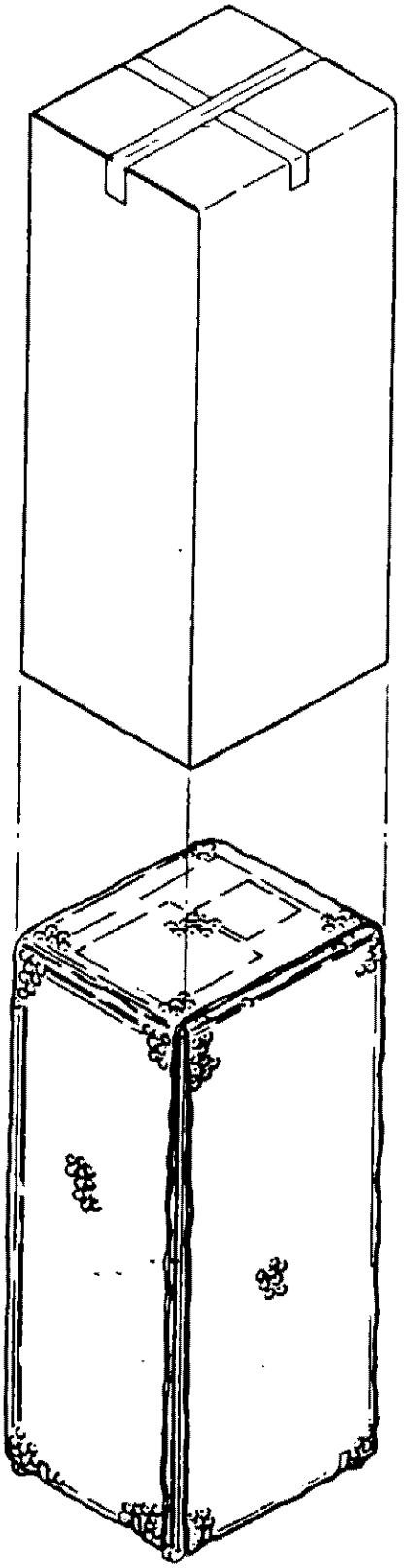

FIGURE 9-2. HARDWARE CABINET PACKING AND UNPACKING

9.4.2 RFSP Packing and Unpacking

RFSP peripheral elements will be packaged in their original shipping container as follows:

1. The packing carton is opened at the top. All packing material will be removed.
2. Wrap the printer in anti-static bag. Fold over end of bag and tape to seal.
3. Place foam end-caps at each side of the printer.
4. Carefully place the printer into the container.
5. Place ribbon box behind printer in shipping carton.
6. Insert printer power cord into anti-static bag. Fold over end of bag and tape to seal. Place behind unit on top of ribbon box.
7. Fold over the four flaps at top of container (large flaps last) and seal with shipping strength tape.
8. Tape or band shipping carton. If using a band, wrap nylon strap around width of carton approximately 6-inches from each edge. Secure each strap with a metal clip.

NOTE

Additional instructions can be found for FA 10095/11 on the shipping carton and in section 1 of the Model 9034/9044 Operating Guide Edition B (October 1988).

The RFSP is unpacked in the reverse order. Care should be used in cutting the top edge of the box so as not to exceed 1/4-inch depth with the cutting edge. Packing materials should be stored inside the box and the box stored in a dry area in case it is ever necessary to transport the printer. Figure 9-3 (FA 10095/2) and Figure 9-4 (FA 10095/11) illustrate RFSP packing and unpacking.

9.4.3 CRT Packing and Unpacking

The CRT peripheral elements will be packaged in their original shipping containers. There are two types of shipping containers for the CRT, one in which the unit is packaged screen down, and one screen to the side. The procedure to pack the CRT is as follows:

1. The packing carton is opened at the top. All packing materials will be removed except the bottom level.
2. Wrap CRT in anti-static bag. Fold over end and tape to seal.
3. Carefully center the CRT, screen down (or to the side depending on the container), in the molded packing.
4. Place molded top level of packing over the CRT when appropriate.
5. Fold over flaps at top of container (large flaps last) and seal with shipping strength tape or band. If bands are used, secure with metal clip.

The CRT is unpacked in the reverse order. Care should be used in cutting the top edge of the box not to exceed 1/4-inch depth with the cutting edge. Packing materials should be stored inside the box and the box stored in a dry area in case it is ever necessary to transport the CRT. Figure 9-5 (FA 10095/4), figure 9-6 (FA 10095/12), and (FA 10095/18) illustrate CRT packing and unpacking. ■

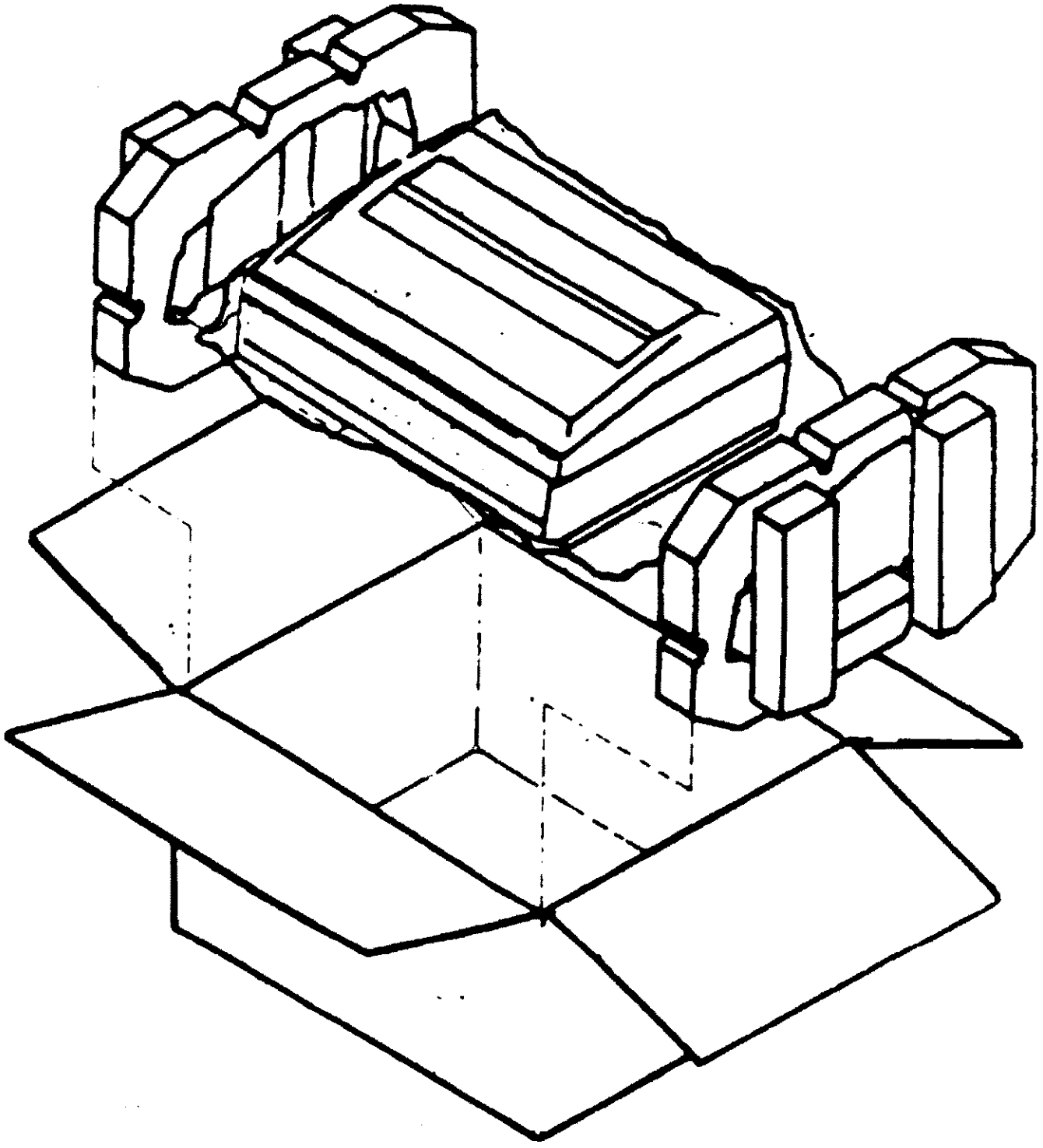

FIGURE 9-3. RFSP (FA 10095/2) PACKING AND UNPACKING

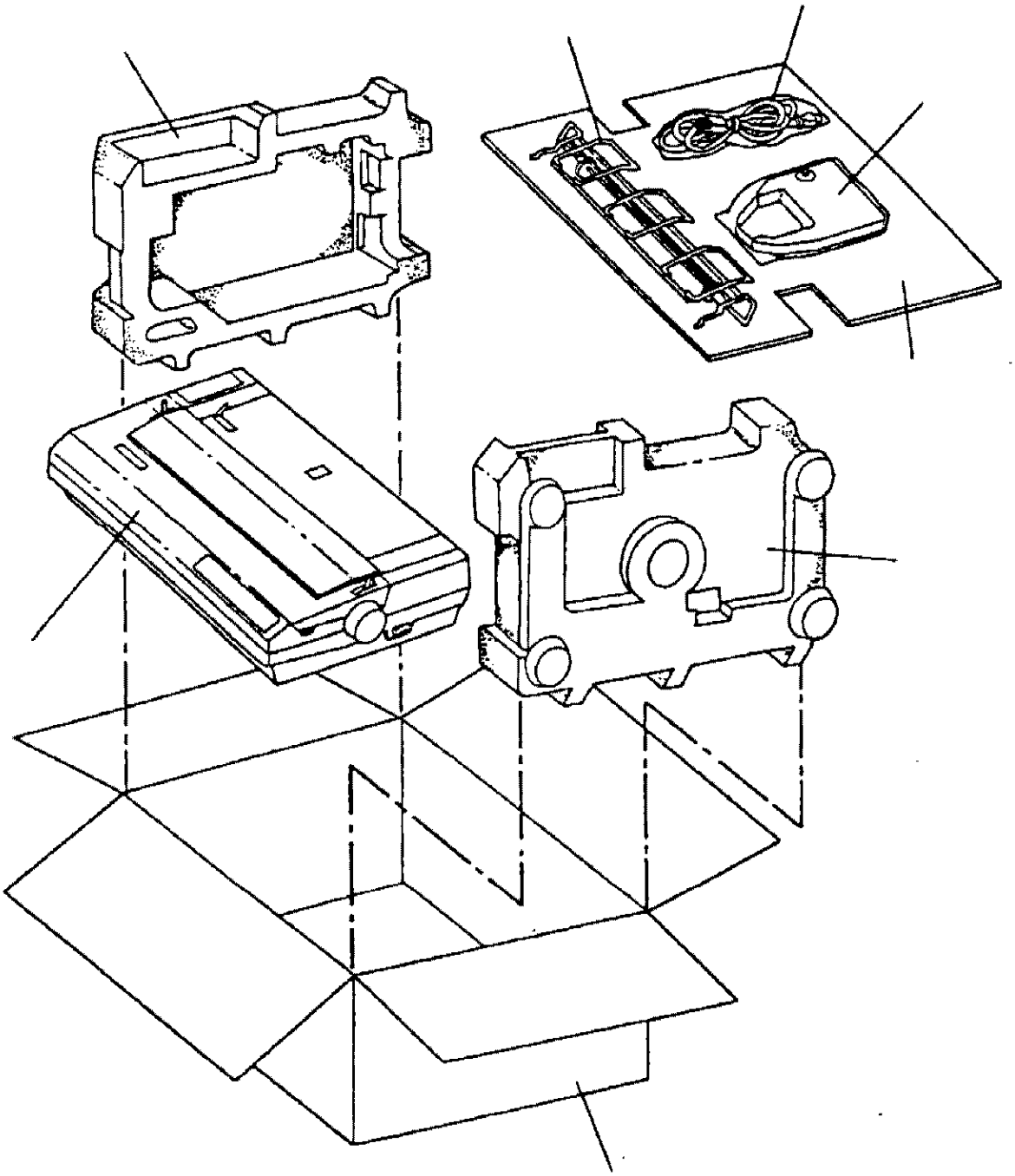

FIGURE 9-4. RFSP (FA 10095/11) PACKING AND UNPACKING

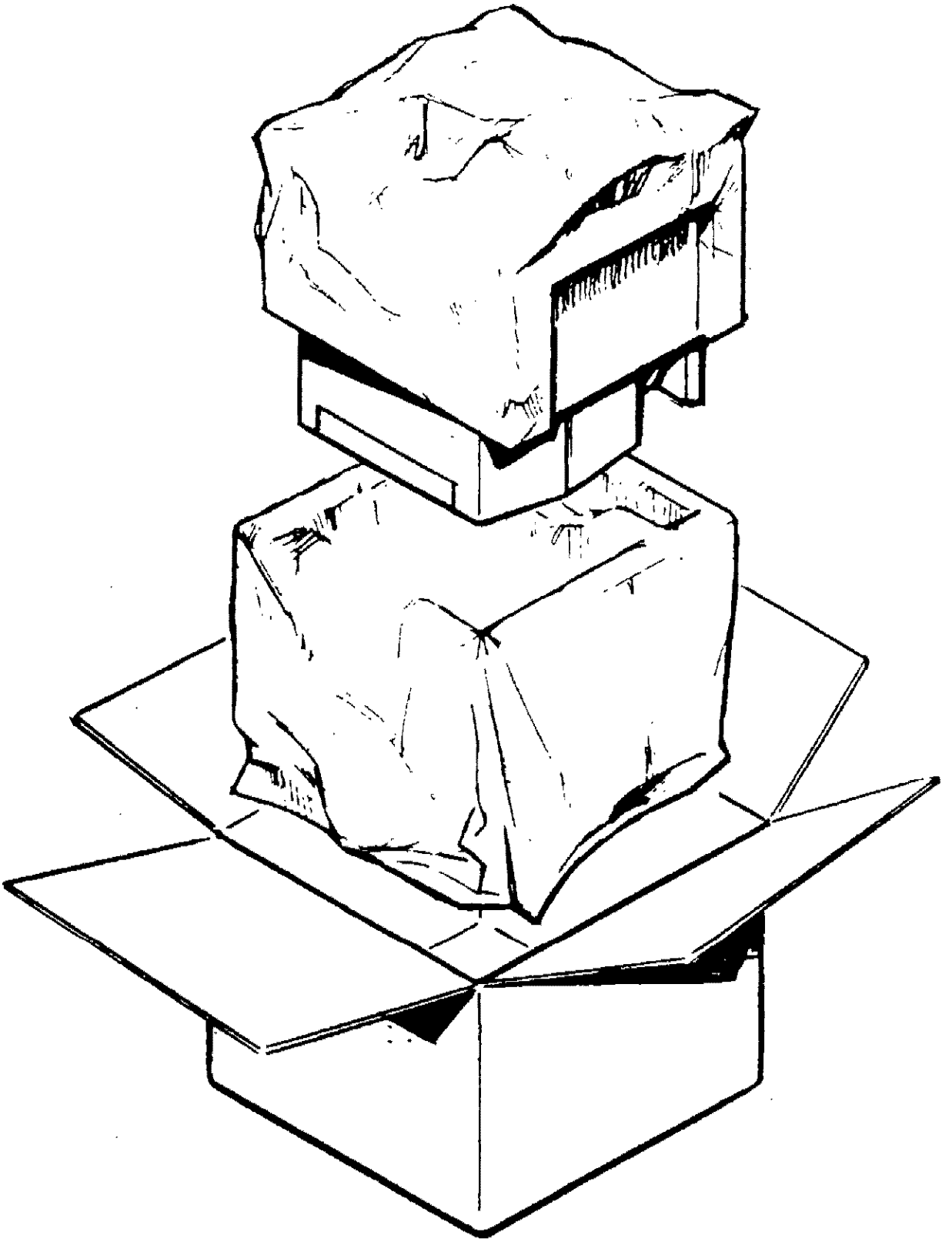

FIGURE 9-5. CRT (FA 10095/4) PACKING AND UNPACKING

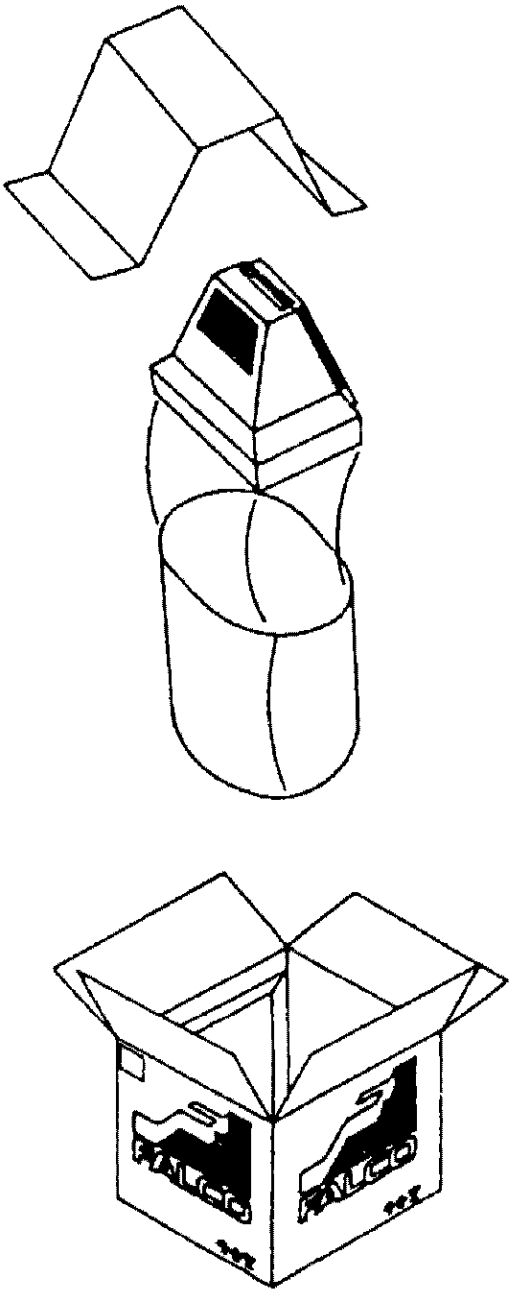

FIGURE 9-6. CRT (FA 10095/12) PACKING AND UNPACKING

9.4.4 RANK Packing and Unpacking

RANK peripheral elements will be packaged inside a commercial grade container provided by FSG, Inc. as follows:

1. The packing carton is opened at the top. Remove all packing material.
2. Wrap unit in bubble wrap and place in shipping container.
3. Close top of container and seal with shipping strength tape.

The RANK is unpacked in the reverse order. Care should be used in cutting the top edge of the box not to exceed 1/4-inch depth with the cutting edge. Packing materials should be stored inside the box and the box stored in a dry area in case it is ever necessary to transport the RANK. Figure 9-7 illustrates RANK packing and unpacking.

9.4.5 Cable Assembly Packing and Unpacking

The cables will be packaged in a commercial grade container provided by FSG, Inc. The box will be mounted on a 4-foot pallet for shipping, along with other peripheral equipment intended for the site. The cables are packed as follows:

1. The packing carton is opened at the top. All packing material will be removed except the bottom level.
2. Center the cable on the bottom level of packing.
3. Place the top level of packing over the cable.
4. Fold over the flaps at the top of the container (large flaps last) and seal with shipping strength tape or band. If bands are used, secure with metal clip.

Cables are unpacked in the reverse order. Care should be used in cutting the top edge of the box not to exceed 1/4-inch depth with the cutting edge. Packing materials should be stored inside the box and the box stored in a dry area in case it is ever necessary to ship the cable assembly. Figure 9-8 illustrates cable packing and unpacking.

NOTE

Cables will be clearly marked at each end for type and installation location.

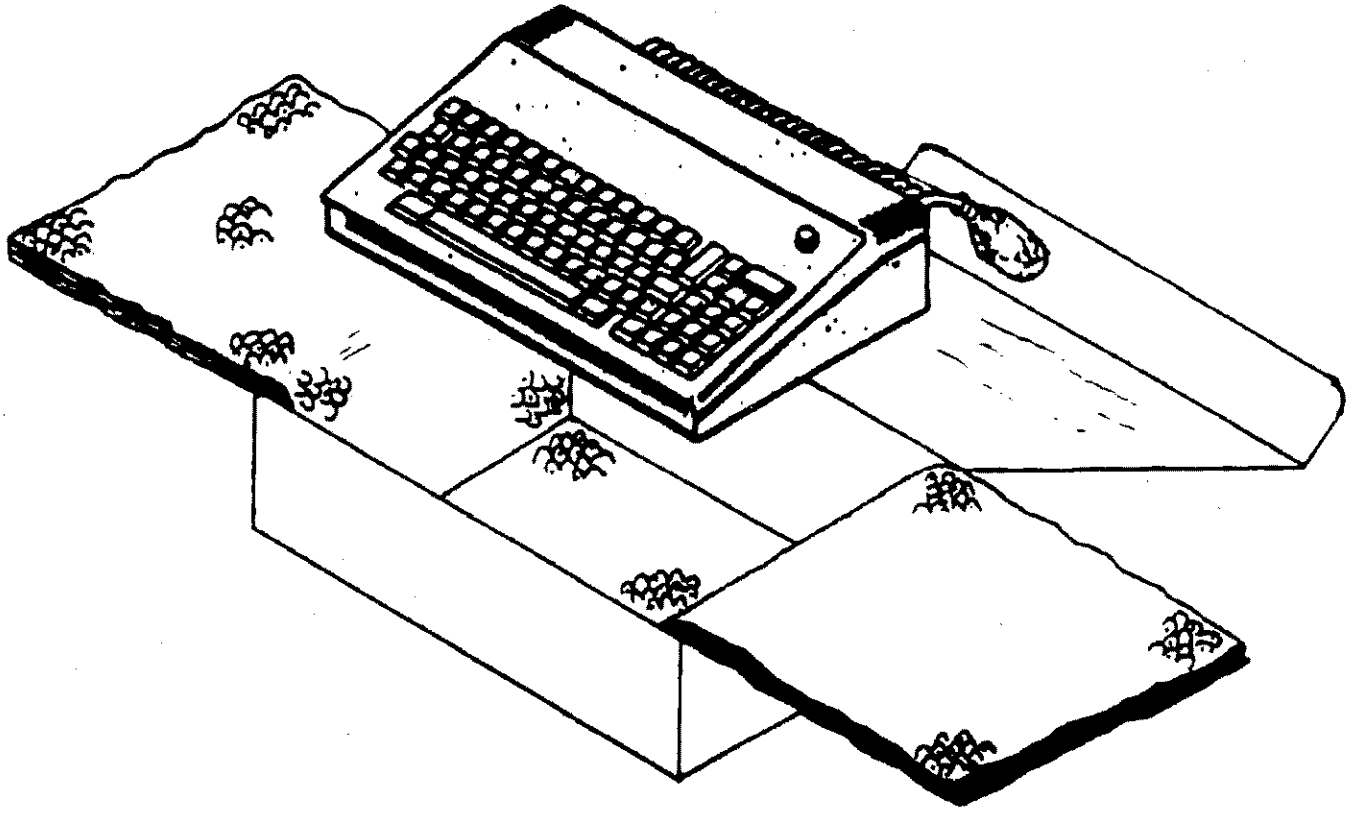

FIGURE 9-7. RANK PACKING AND UNPACKING

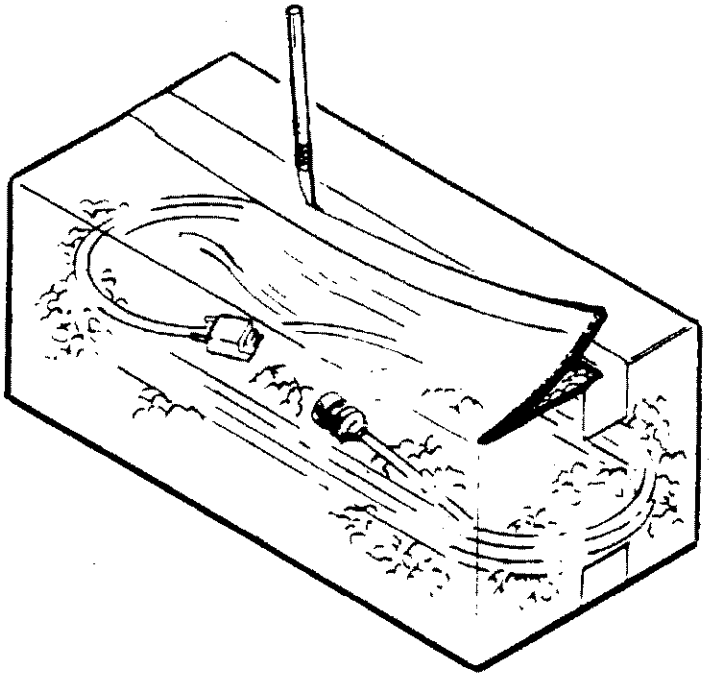

FIGURE 9-8. CABLE ASSEMBLY PACKING AND UNPACKING

9.5 INPUT REQUIREMENT SUMMARY

A summary of the input data contained on the installation drawings is shown in tables 9-2 and 9-3. Environmental considerations are listed on table 9-4.

TABLE 9-2. ELECTRICAL CHARACTERISTICS OF FDIO EQUIPMENT

ELEMENT	MAX CURRENT (AMP)	VOLTAGE	WATTS	POWER FACTOR	SURGE CURRENT (AMP)
CCU	1.62	115 V ac	137.2	0.74	11.75
PCU	1.45	115 V ac	129.2	0.78	11.75
CCU/CCU	3.24	115 V ac	274.4	1.48	16.00
PCU/PCU	2.9	115 V ac	258.4	1.56	16.00
CCU/PCU	3.07	115 V ac	266.4	1.52	16.00
RCU	0.77	115 V ac	68.10	0.76	8.00
RCU Expanded	0.8	115 V ac	68.10	0.76	8.00
RFSP (1)	0.1098	115 V ac	7.185	-.58	1.00
RFSP (2)	.24	120 V ac	12	-.43	5.00
RFSP (5)	.26	120 V ac	17.1	.55	3.00
RANK (6)	0.1054	115 V ac	9.838	0.82	0.70
RANK (7)	2.40	115 V ac	48.00	0.80	3.5
CRT (3)	0.1395	115 V ac	10.02	-.61	1.0
CRT (4)	0.61	115 V ac	40	-.57	7.2
CRT (8)	2.00	115 V ac	46.0	-.51	50.0

NOTE

1. RFSP is the original FDIO printer FA 10095/2
2. RFSP is printer FA 10095/11
3. CRT is the original FDIO video display FA 10095/4
4. CRT is video display FA 10095/12
5. RFSP is printer FA 10095/14
6. RANK is keyboard FA 10095/3
7. RANK is keyboard FA 10095/17
8. CRT is video display FA 10095/18

TABLE 9-3. POWERPANEL CONNECTION ELECTRICAL REQUIREMENTS

ELEMENT	REQUIREMENT
CCU or PCU Cabinet	2 — 115 V ac (± 10%) input
RCU Cabinet	1 — 15 A circuit on essential or critical power, 115 V ac (± 10%) input
RCU Expanded Cabinet	1 — 15 A circuit on essential or critical power, 115 V ac (± 10%) input
RFSP	1 — Government supplied 115 V ac (± 10%) outlet on essential or critical power within 6-feet of each unit. Maximum current rating is 1.04 A.
RANK	1 — Government supplied 115 V ac (± 10%) outlet on essential or critical power within 6-feet of each unit. Maximum current rating is .30 A.
CRT	1 — Government supplied 115 V ac (± 10) outlet on essential or critical power within 6-feet of each unit. Maximum current rating is .43 A.

TABLE 9-4. ENVIRONMENTAL CONSIDERATIONS FOR FDIO EQUIPMENT

Ambient Temperature:		50-100° Fahrenheit
Relative Humidity:		20-80% noncondensing
Heat Dissipation:	CCU/CCU	— 274.4 Watts
	PCU/PCU	— 258.4 Watts
	CCU/PCU	— 266.4 Watts
	CCU	— 137.2 Watts
	PCU	— 129.2 Watts
	RCU	— 68.1 Watts
	RCU Expanded	— 68.1 Watts
	RFSP (1)	— 7.2 Watts
	RFSP (2)	— 12.0 Watts
	RFSP (5)	— 17.1
	RANK	— 9.8 Watts
	CRT (3)	— 10.0 Watts
	CRT (4)	— 40.0 Watts

TABLE 9-4. ENVIRONMENTAL CONSIDERATIONS FOR FDIO EQUIPMENT (Continued)

NOTE

1. RFSP is the original FDIO printer FA 10095/2
2. RFSP is printer FA 10095/11
3. CRT is the original FDIO video display FA 10095/4
4. CRT is video display FA 10095/12
5. RFSP is printer FA 10095/14

9.6 INSTALLATION PROCEDURES

FSG Inc. will initiate a letter to each ARTCC and ATCT 30 days prior to the scheduled installation date to ensure the following central and remote site requirements have been met:

- Modem lines are in place.
- Modem multiplexer is installed and operational.
- Modem is, whenever possible, within 50 cable-feet of designated control cabinet assembly location.
- All cable trays, circuit breakers, and conduit necessary to connect the appropriate cables from the control cabinet assembly to all peripheral locations are installed.
- Console space in operations room is adequate for peripheral elements.
- One 115 V ac (± 10 percent) outlet on essential or critical power is located within 6-feet of each peripheral location.
- Installation date(s) are acceptable.
- Any required console modifications (government furnished) have been completed.

FDIO equipment will be delivered by motor carrier. Control cabinet assemblies will be placed in their permanent locations at time of delivery by carrier personnel. All other equipment will be placed in secure storage in as close proximity as possible to the final installation area.

9.6.1 Central Site Installation Procedures

The procedure for installation at the central sites is as follows:

1. Installation team arrives at site.
2. Utilizing FSG, Inc. equipment, the installation team will inspect applicable ac power and ground sources.
3. The team will visually inspect the CCU and PCU cabinet assemblies for any signs of damage during moving operations.

4. The hardware cabinets will be placed in or near their designated final installation position. Permanent placement will sometimes be accomplished by FAA personnel after installation team leaves (for example, when FDIO equipment physically replaces FDEP equipment).
5. Installation team will run ac power from a GFE breaker panel through GFE conduit and/or cable tray to the CCU and PCU cabinet assemblies.
6. Connection to a GFE ground plane will be made.
7. Power up the CCU and PCU configurations. Ensure dc voltage level is correct.
8. Run offline CCU and PCU internal DIAGs.
9. Run cable(s) from the CCU to the modem. Connect the modems to the lines extending from the CCUs.
10. In conjunction with FAA personnel, run communications DIAGs to test the link from the CCU through the local modem/multiplexer, and through the GFE phone line(s) through the remote modem/multiplexer(s) to each RCU control element as it is installed.
11. Testing of remote sites will begin at this stage. Approximately every other day the installation team will prepare a remote site to be tested with the center.
12. All peripheral elements will be brought to the appropriate PCU cabinet assembly location.
13. Unpack elements in accordance with instructions in section 9.4.
14. Visually inspect the peripheral elements for any signs of damage during moving operations.
15. Power up each element and run self-diagnostics.
16. Connect each peripheral element to its BC port in the PCU cabinet assembly and run the applicable DIAG. Any peripheral that fails at this level will be replaced from contractor stock.
17. Installation team will place all peripherals' permanent signal cables, routing from the PCU through GFE cable trays to the appropriate enroute console locations.
18. Place all peripheral elements in temporary system test positions and connect ac, signal, and required PAMRI cables.
19. Perform overall visual inspection of the system checking for proper routing and good cabling procedures.
20. Installation team will run initial installation test to ensure proper operation of equipment prior to Hardware Site Test (HST).
21. After the ARTCC and ATCT site installation is complete, the HST will be performed in conjunction with FAA personnel (Airways Facilities (AF) and Air Traffic (AT) representatives). The HST will use FSG DIAG equipment to emulate the PAMRI Host interface. If any assembly fails at this level, it will be replaced from contractor stock.
22. After successful completing of HST testing, Site Acceptance testing will commence in conjunction with FAA and AT representatives. If any assemblies fail at this level, it will be replaced from contractor's stock.
23. Once the system has been accepted, FAA AF personnel will assume responsibility for placing all equipment not already in its permanent position and for final connection to the PAMRI link.

24. FAA personnel will be responsible for any console modifications required.

9.6.2 Remote Site Installation Procedures

The procedure for installation at the remote sites is as follows:

1. Installation team arrives at site.
2. Utilizing FSG, Inc. equipment, the installation team will inspect applicable ac power and ground sources.
3. The team will visually inspect the RCU cabinet assemblies for any signs of damage during moving operations.
4. The RCU cabinets will be placed in or near their designated final installation position. Permanent placement will sometimes be accomplished by FAA personnel after installation team leaves (for example, when FDIO equipment physically replaces FDEP equipment).
5. Installation team will run ac power from a GFE breaker panel through GFE conduit and/or cable tray to the RCU.
6. Make the connection to a GFE ground plane.
7. Power up the RCU cabinet assembly. Ensure dc voltage level is correct.
8. Run offline RCU control element internal diagnostics.
9. Run cable(s) from the RCU cabinet assembly to the modem. Connect the modems to the lines extending from the RCU.
10. In conjunction with FAA personnel, test link through the modem over the GFE phone line through the modem at the ARTCC and applicable CCU cabinet assembly.
11. All peripheral elements will be brought to the appropriate RCU cabinet assembly location.
12. Unpack elements in accordance with paragraph 9.4.
13. Visually inspect the peripheral elements for any signs of damage during moving operations.
14. Power up each peripheral element and run self-diagnostics.
15. Connect each peripheral element to its BC port in the RCU cabinet assembly and run the applicable DIAG. If any peripheral element fails at this level, it will be replaced from contractor stock.
16. Installation team will place all peripherals' permanent signal cables, routing from the RCU cabinet assembly through GFE cable trays to the appropriate IFR and Tower Cab room locations.
17. Place all peripheral elements in temporary acceptance test positions and connect ac and signal cables.
18. Perform overall visual inspection of the system checking for proper routing and good cabling procedures.
19. Installation team will run installation test to ensure proper operation of equipment prior to HST.

20. In conjunction with FAA personnel (AF and AT representatives) the team will run the FAA approved HST after all RCUs have been installed in accordance with the contract schedule. The HST will use FSG DIAG equipment to emulate the PAMRI Host interface. If any assembly fails at this level, it will be replaced from contractor stock.

21. Once the system has been accepted, FAA AF personnel will assume responsibility for placing all equipment not already in its permanent position.

22. FAA personnel will be responsible for any console modifications required.

9.7 INSTALLATION CHECKOUT

All FDIO equipment will pass the Factory Acceptance Test or Unit Testing approved by the FAA before being shipped to the installation site. At the installation site, the equipment will be tested using the HST and Site Acceptance procedures approved by the FAA. This test will demonstrate that the FDIO equipment operates correctly and within specified tolerances. Periodic maintenance procedures for the FDIO equipment will be found in section 6.0 of this document.

9.7.1 Installation, Inspection, and Pre-energizing Procedures

A checklist will be provided for the installation crew chief to verify installation procedures. The checklist will include the following items:

1. All control and peripheral elements are installed in their correct locations and are properly oriented. When FDIO equipment physically replaces FDEP equipment, FAA personnel may be required to place the equipment in its permanent position after the Acceptance Testing is completed and the FSG, Inc. installation team has left.

2. All cable assemblies and transmission lines are installed in accordance with plans and specifications. Continuity exists in all interconnections.

3. Equipment has been properly installed to allow adequate access to the equipment for maintenance.

4. Rotating devices are free from obstruction. Fans with openings into blade areas are free of packing material or other foreign materials.

5. Adequate ventilation has been provided to equipment areas which generate heat.

6. All pre-energizing servicing procedures have been accomplished as required.

9.7.2 Initial Startup and Preliminary Test

Procedures for energizing the equipment for the first time are found in section 3.0 of this document. Step-by-step procedures are provided for testing the equipment at the HST.

9.7.3 Installation Verification Test

Complete instructions for testing are provided in the Site Acceptance. These procedures include checking alarms and other sensing devices for proper operation. Necessary setup data is included for each procedure.

10.0 COMPUTER SOFTWARE

10.1 GENERAL

The software developed for the FDIO system is divided into two categories: modifications to existing Host software and the tasks, called firmware, integrated into the hardware design described in this document. The technical manuals and documents listed in table 10-1 contain the programming and design information pertinent to the FDIO firmware. The firmware resides in the microprocessors of the FDIO system. All entries in table 10-1 are described in paragraph 10.2.

10.2 CONTENT DESCRIPTION

The following subparagraphs provide brief descriptions of the firmware publications listed in table 10-1.

10.2.1 American National Standard for Advanced Data Communication Control Procedures (ADCCP)

The ADCCP standard establishes procedures to be used on synchronous communication links using ADCCP. It is intended to cover a wide range of applications and a wide range of data link configurations and is designed in terms of actions that occur on receipt of commands at secondary stations and combined stations.

10.2.2 Overall Computer Program Description (OCPD)

The OCPD identifies the functions of the overall computer firmware including descriptions of system functional capability, equipment configurations and variations, each functional area, and each version and its implementation plan.

10.2.3 Computer Program Functional Specification (CPFS)

The CPFS specifies all the functions required of the computer firmware in order to satisfy system requirements. Included are descriptions of the functions and their performance criteria, operational limitations, constraints, and other qualifying data.

10.2.4 Software Interface Control Document (SICD)

The SICD describes computer firmware interface communications between two or more interacting tasks or system components. It also provides descriptions of the interface channels, hardware operation, startup/startover, interface order and control words, and data transfers.

10.2.5 Program Design Specification (PDS)

The PDS translates the functional specifications of the FDIO system into the resultant firmware design for the system. The PDS provides a description of system organization, message logic flow, task interfaces, and firmware storage and timing requirements.

10.2.6 Software Design Data (SDD)

The SDD describes all the program information on the internal design of the FDIO firmware. The SDD contains descriptions and logic flows of each task, storage requirements and timing estimates, and program source listings.

TABLE 10-1. SOFTWARE INSTRUCTION BOOK LIST

Manual Number	Source	Title
ANSI X3.66	ANSI	American National Standard For Advanced Data Communication Control Procedures (ADCCP)
FDIO 51G1	FSG	Overall Computer Program Description (OCPD)
FDIO 51G2	FSG	Computer Program Functional Specification (CPFS)
FDIO 51G3	FSG	Software Interface Control Document (SICD)
FDIO 51G4	FSG	Program Design Specification (PDS)
FDIO 51G5	FSG	Software Design Data (SDD)
FDIO 51G6	FSG	Data Base Table Design Specification (DBTDS)
591112003	Hunter & Ready, Inc.	VRTX/86 User's Guide
121703-003	Intel	ASM86 Language Reference Manual
121737-002	Intel	MCS-51 Utilities User's Guide for 8080/8085-Based Development Systems
121776-002	Intel	Run-Time Support Manual for iAPX 86, 88 Applications
122085-002	Intel	iC86 Compiler User's Guide
143824-003	Intel	iSBC 88/45 Advanced Data Communications Processor Board Hardware Reference Manual
9800937-03	Intel	MCS-51 Macro Assembler User's Guide
ISBN 0-8359-3035-1	Intel	iAPX 86, 88, 186 and 188 User's Manual and Programmers Reference, Volume 1
00-2057-02	Zilog	Z8030/Z8530 SCC Serial Communications Controller Technical Manual

10.2.7 Data Base Table Design Specification (DBTDS)

The DBTDS includes a detailed description of each table, including its functional dimensions, usage, lock requirements, ordering, and general design considerations. The specification also includes intertable relationships, definition and layout, data descriptions, and any restrictions or limitations.

10.2.8 VRTX/86 User's Guide

This vendor publication describes the silicon software component that is integrated into FDIO as the EXEC firmware task; it defines the architecture, features, and commands used to adapt VRTX/86 to FDIO requirements.

10.2.9 ASM86 Language Reference Manual

This manual describes the assembly language for the 8086/8088 microprocessor; it assumes the reader has knowledge of the 8086/8088 microprocessor.

10.2.10 MCS-51 Utilities User's Guide for 8080/8085-Based Development Systems

This manual describes the RL51 linker and locator and the LIB51 librarian for program modules produced by MCS-51 language translators such as ASM51 and PL/M-51.

10.2.11 Run-Time Support Manual for iAPX 86, 88 Applications

This manual focuses on the run time aids that Intel offers for the iAPX 86, 88 family of processors. The documentation of these run time aids is applicable to all Intel languages.

10.2.12 iC86 Compiler User's Guide

This manual describes the C programming language compiler for the Intel iAPX 86 family of microprocessors. It is intended to support new users as well as those already familiar with the C programming language.

10.2.13 iSBC 88/45 Advanced Data Communications Processor Board Hardware Reference Manual

This manual supplies general information, preparation for use, programming information, principles of operation, and service information for the iSBC 88/45 Advanced Data Communications Processor Board.

10.2.14 MCS-51 Macro Assembler User's Guide

This manual describes how to program the MCS-51 single-chip microcomputers in assembly language. It also describes the operating instructions for the MCS-51 Macro Assembler.

10.2.15 iAPX 86, 88, 186 and 188 User's Manual and Programmers Reference

This manual describes the iAPX 86, 88, 186, and 188 family of microprocessor systems. Volume 1 is a general introduction and contains an overview of the CPU along with some design information.

10.2.16 Z8030/Z8530 SCC Serial Communications Controller Technical Manual

This manual describes the capabilities, architecture, programming, and register functions of the serial communications controller.

SECTION 10. COMPUTER SOFTWARE

10.1 GENERAL.- The software developed for the FDIO system is divided into two categories: (1) modifications to existing NAS 9020 software and (2) the tasks, called firmware, integrated into the hardware design described in this document. The technical manuals and documents listed in Table 10-1 contain the programming and design information pertinent to the FDIO firmware. The firmware resides in the microprocessors of the FDIO system. All entries in Table 10-1 are described in Paragraph 10.2.

10.2 CONTENT DESCRIPTION.- The following subparagraphs provide brief descriptions of the firmware publications listed in Table 10-1.

10.2.1 American National Standard for Advanced Data Communication Control Procedures (ADCCP).- The ADCCP standard establishes procedures to be used on synchronous communication links using ADCCP. It is intended to cover a wide range of applications and a wide range of data link configurations and is designed in terms of actions that occur on receipt of commands at secondary stations and combined stations.

10.2.2 Overall Computer Program Description (OCPD).- The OCPD identifies the functions of the overall computer firmware including descriptions of system functional capability, equipment configurations and variations, each functional area, and each version and its implementation plan.

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10.2.6 Software Design Data (SDD).- The SDD describes all the program information on the internal design of the FDIO firmware. The SDD contains descriptions and logic flows of each task, storage requirements and timing estimates, and program source listings.

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143824-003	Intel	iSBC 88/45 Advanced Data Communications Processor Board Hardware Reference Manual
9800937-03	Intel	MCS-51 Macro Assembler User's Guide
ISBN 0-8359-3035-1	Intel	iAPX 86, 88, 186 and 188 User's Manual and Programmers Reference, Volume 1
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10.2.16 Z8030/Z8530 SCC Serial Communications Controller Technical Manual.- This manual describes the capabilities, architecture, programming, and register functions of the serial communications controller.

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SECTION 11. TROUBLESHOOTING SUPPORT DATA

11.1. INTRODUCTION.- The support data in this section includes line drawings, block diagrams, blocked schematics, and other diagrams of printed circuit board layouts as well as other illustrative data describing the FDIO system. All the support data for this section is presented on B-size pages in a separate volume. The form and content of this information is intended to assist the technicians who will be maintaining and troubleshooting the system.

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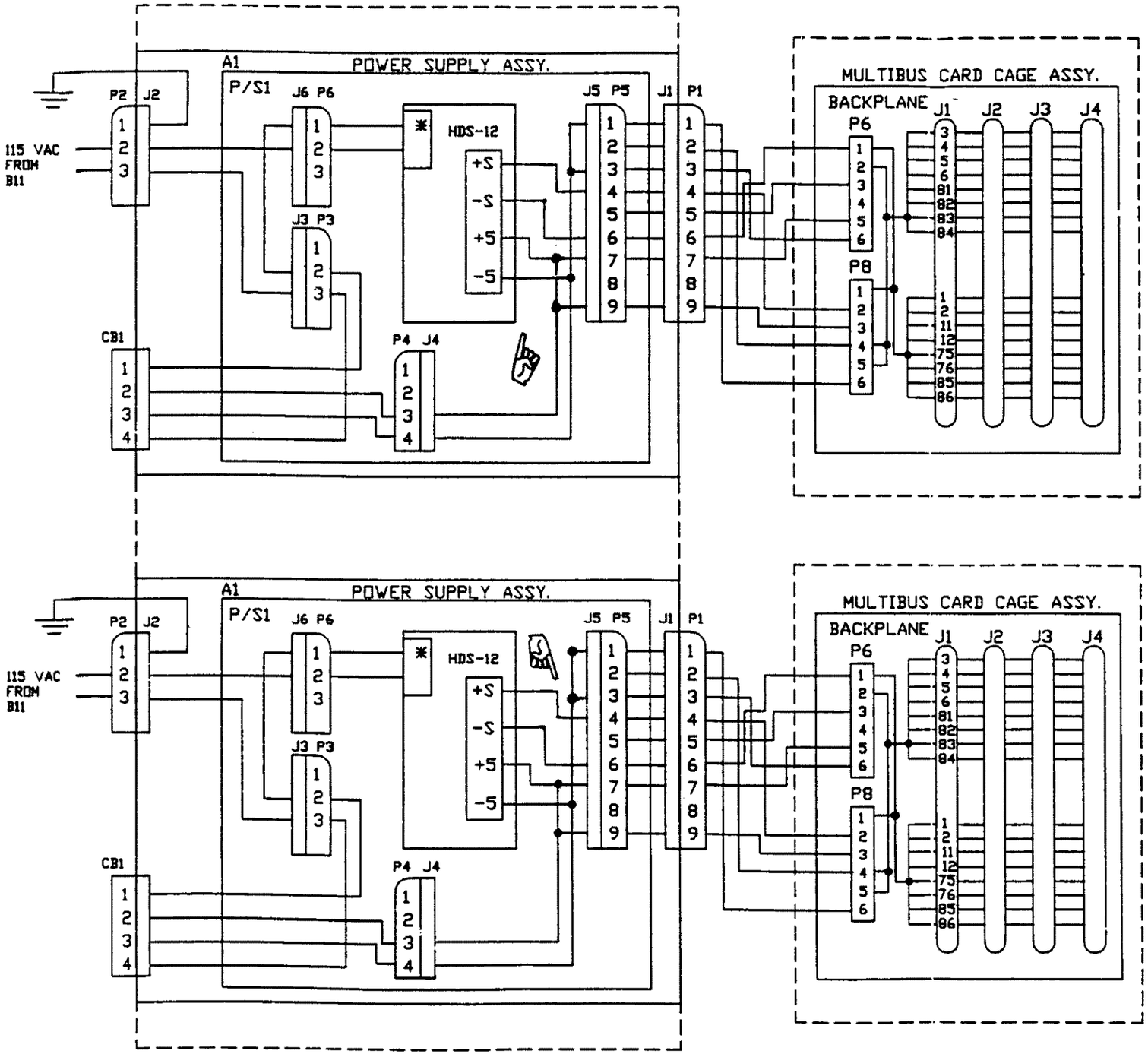
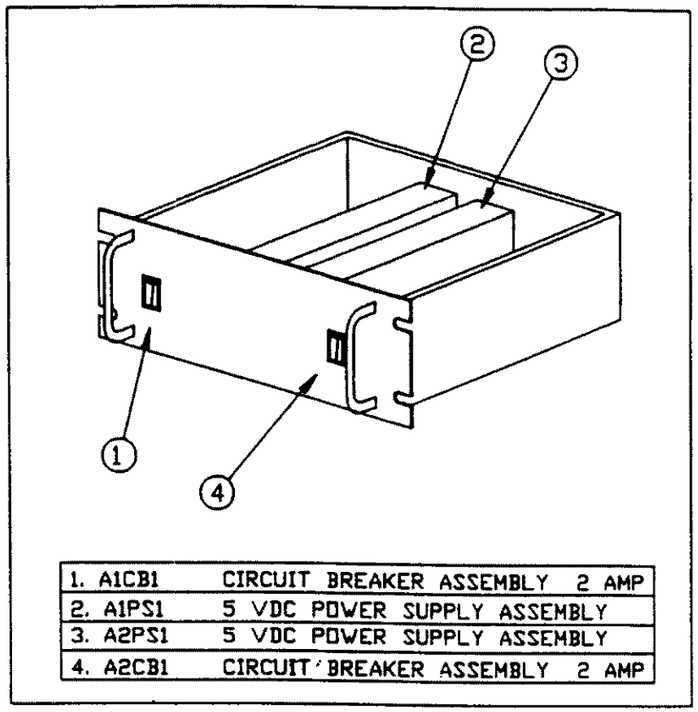
FDIO-51B





1. A1CB1	CIRCUIT BREAKER ASSEMBLY	2 AMP
2. A1PS1	5 VDC POWER SUPPLY ASSEMBLY	
3. A2PS1	5 VDC POWER SUPPLY ASSEMBLY	
4. A2CB1	CIRCUIT BREAKER ASSEMBLY	2 AMP

THE CONTROL CABINET CONFIGURATION(S) LISTED BELOW USE THE SINGLE VOLTAGE POWER SUPPLY TO SUPPLY THE MULTIBUS ASSEMBLY.

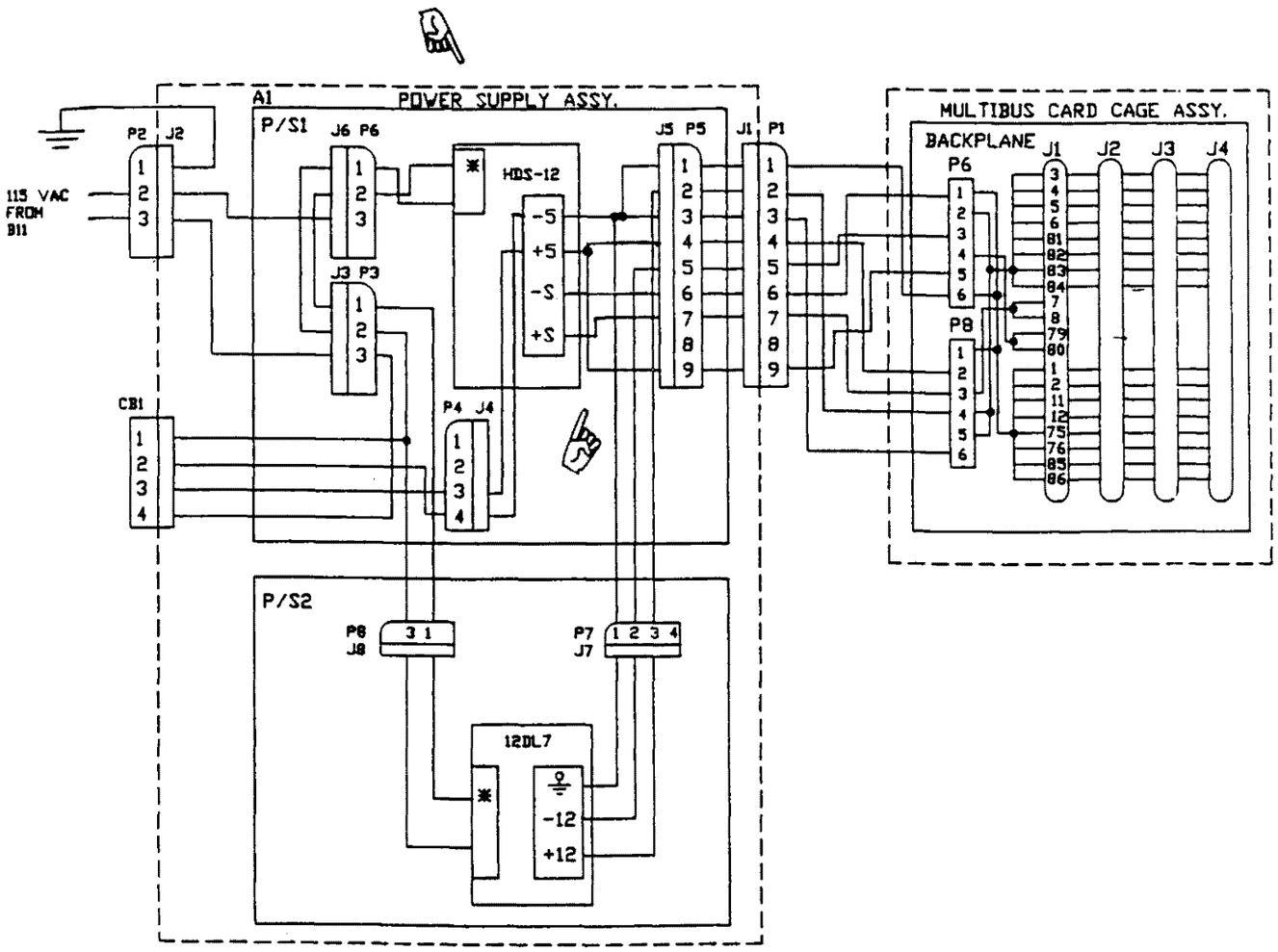
1. CCU
2. PCU
3. CCU / PCU
4. CCU / CCU
5. PCU / PCU

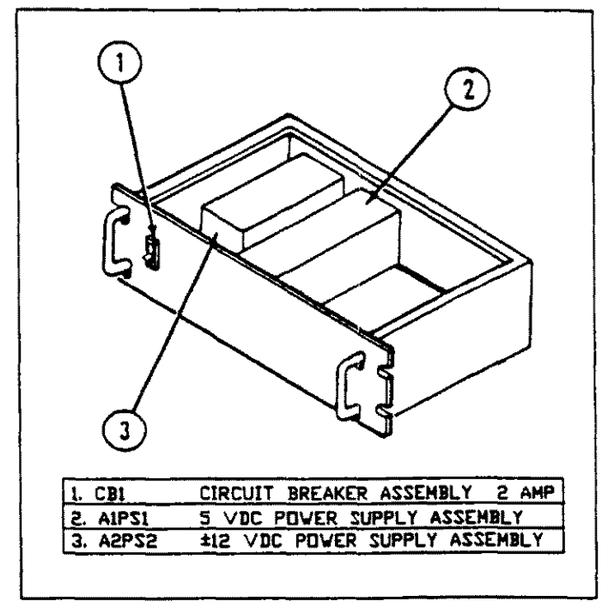
* Refer to power supply for 120 VAC terminal connections

Figure 11-16. FDIO System DC Power Distribution, Sheet 1 of 4

FDIO-51B

TI 6130.6



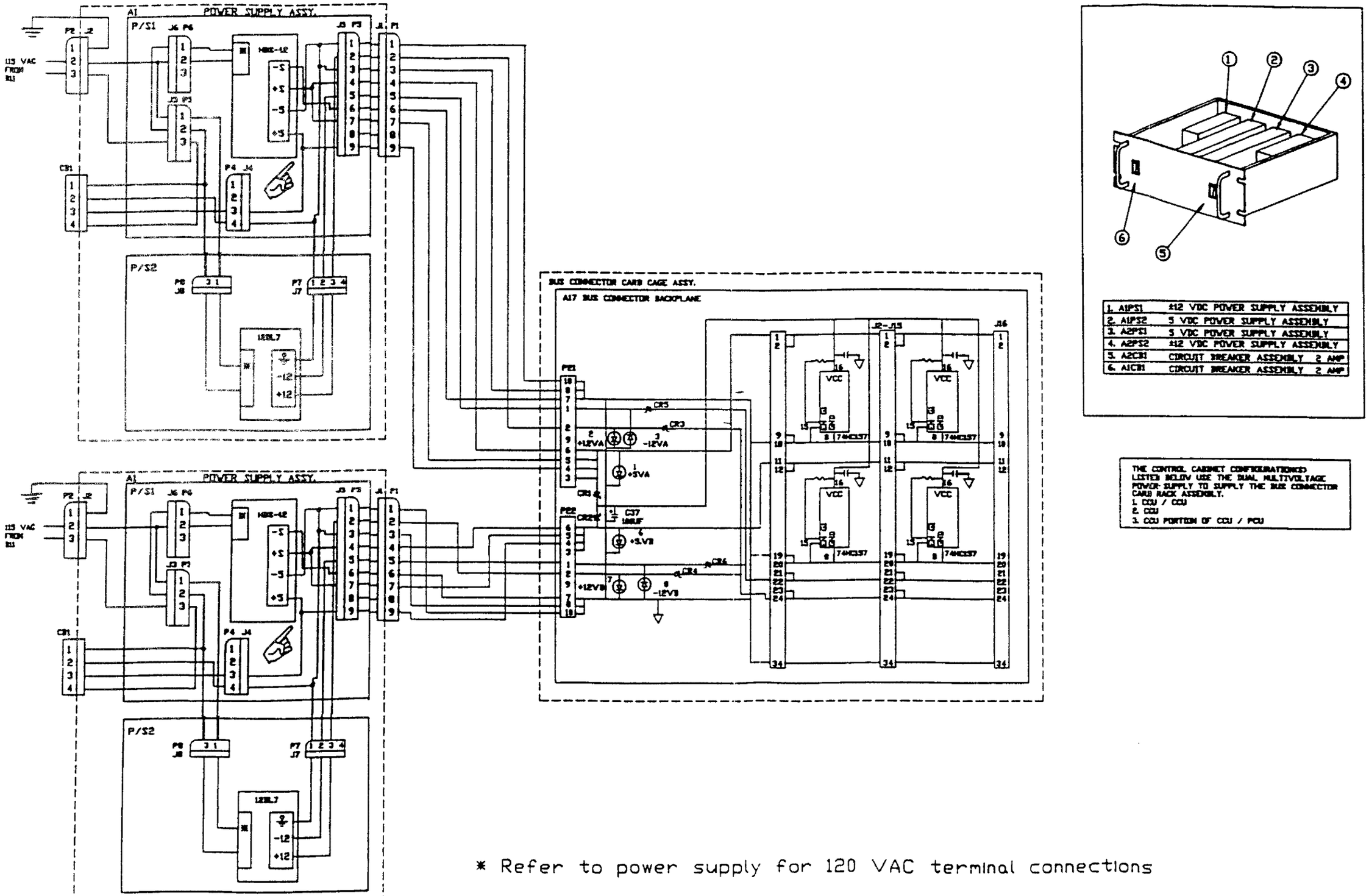


1. CB1	CIRCUIT BREAKER ASSEMBLY	2 AMP
2. A1PS1	5 VDC POWER SUPPLY ASSEMBLY	
3. A2PS2	±12 VDC POWER SUPPLY ASSEMBLY	

THE CONTROL CABINET CONFIGURATION(S) LISTED BELOW USE THE SINGLE MULTIVOLTAGE POWER SUPPLY TO SUPPLY THE MULTIBUS ASSEMBLY.
1. RCU
2. RCU EXPANDED

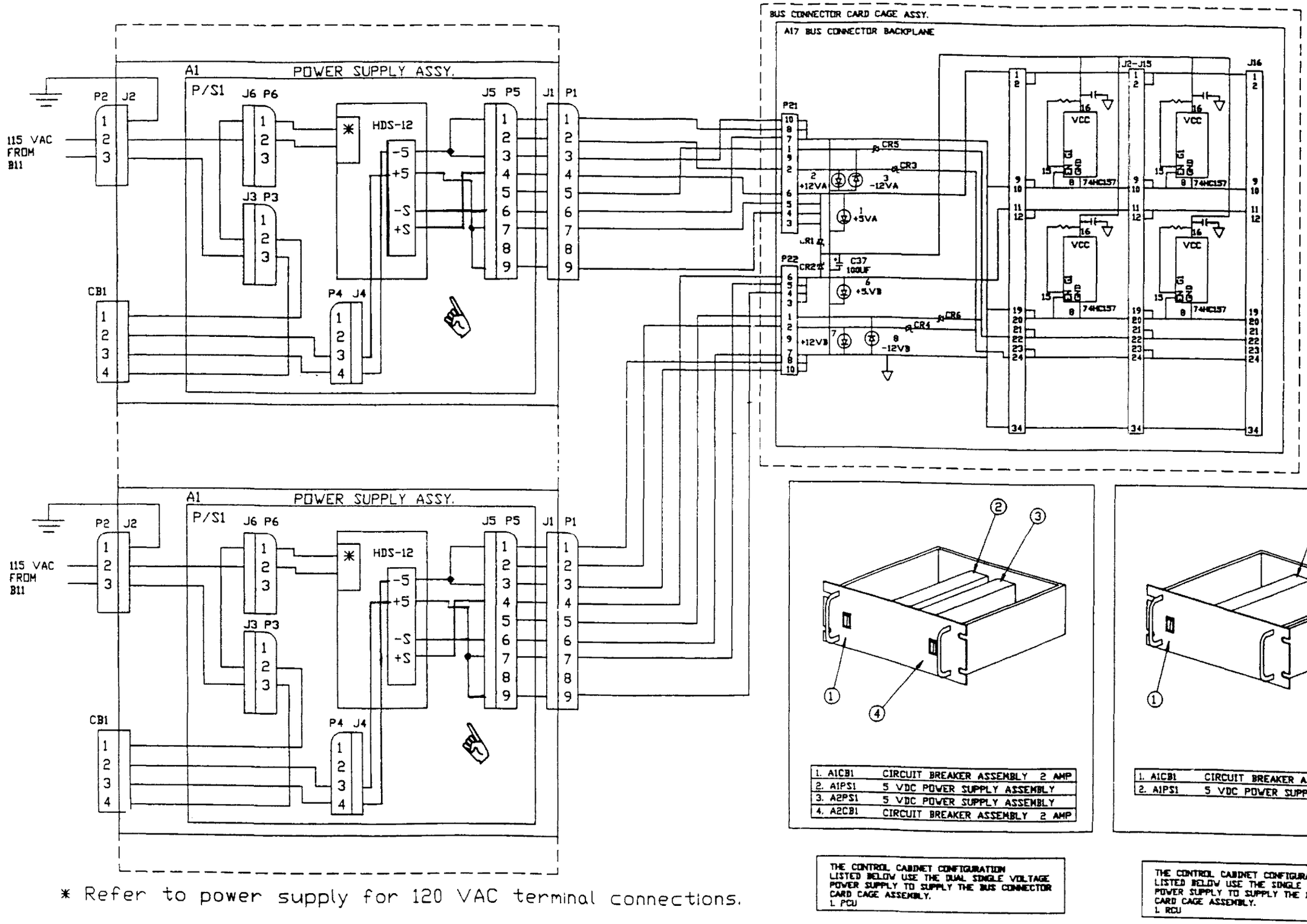
* Refer to power supply for 120 VAC terminal connections

Figure 11-16. FDIO System DC Power Distribution, Sheet 2 of 4



* Refer to power supply for 120 VAC terminal connections

Figure 11-16. FDIO System DC Power Distribution, Sheet 3 of 4



* Refer to power supply for 120 VAC terminal connections.

Figure 11-16. FDIO System DC Power Distribution, Sheet 4 of 4

DATE:
SUBJECT:

FROM:
TO:

a. Present Problems -

b. Recommended Improvements -

Signature

FACILITY IDENTIFIER & ADDRESS

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a. Present Problems -

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