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LETTER REPORT

MODE S COMPUTER PERFORMANCE MEASUREMENT SYSTEM (CPMS)

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PURPOSE.

The intent of this document is to provide a functional description of the Mode S Computer Performance Measurement System (CPMS), and to enumerate it's capabilities and uses.

INTRODUCTION.

The Mode S engineering model sensors built by Texas Instruments Incorporated (TI) include a computer subsystem having a distributive architecture consisting of 36 processors tied together through a large central or global memory by a system of data buses called tilines. All communication among processors is through the global memory. This architecture was selected because of its potential to improve total system reliability and simplify system software development.

During the period of initial hardware fabrication and software development, a software simulation package was developed by TI to study the effects of contention among the processors for access to the system data buses and global memory. This simulation package was also used to study interaction between software modules. The study showed that, due to low predicted utilization for the system data buses, contention effects would be very low and could be ignored.

Additional processors were added during final system development. An engineering analysis indicated that the added processors would only slightly increase data bus utilization and that contention effects would remain negligible. However, the software simulation package was not used to verify this.

During factory acceptance testing an attempt was made to measure data bus utilization. These measurements showed bus utilizations were much higher than predicted. Although no degradation in sensor operation was evident, a more detailed study of the Mode S sensor computer subsystem was determined necessary as an input toward procurement of field implementable sensors.

It was determined that a special piece of test equipment was necessary to accomplish this task. Although many commercial systems were available at the time, they possessed limited capabilities when used in a distributive architecture environment. The CPMS was designed and fabricated for this reason.

A test and evaluation effort using the CPMS followed. Specific performance areas investigated were: System data bus contention/utilization, global memory address space utilization, and processor utilization. A complete description of this effort, as well as an explanation of Mode S sensor probe points is contained in Report No. FAA-RD-81-12.

RELATED DOCUMENTS.

1. "Discrete Address Beacon System (DABS) Computer Performance/Test and Evaluation", FAA-RD-81-12, April 1981.

2. "Discrete Address Beacon System Functional Description", FAA-RD-80-41, April 1980.

3. "The Aircraft Reply and Interference Environment Simulator (ARIES)", FAA-RD-78-96, March 1979.

DESCRIPTION OF EQUIPMENT.

The following paragraphs are intended to provide a functional description of the CPMS.

GENERAL. Designed and built by personnel of the FAA Technical Center to collect performance data on Mode S, the CPMS consists of a Digital Equipment Corporation (DEC) model PDP 11/55 computer with peripherals, a data collection unit, and probes for connection to the Mode S sensor. A block diagram of the basic CPMS is shown in figure 1.

In general, signals providing performance data are received from the Mode S sensor via the following probes which act as buffer/line drivers to the data collection unit: (1) tiline probes, (2) azimuth probes, and (3) memory address probes. Data from these probes are sampled in the data collection unit by the tiline monitor units, control azimuth unit, and memory address monitor units, respectively. The sampled data from these units is transferred to the PDP 11/55 by the computer interface unit. The PDP 11/55 computer buffers data and writes it onto magnetic tape. The data is later reduced via data reduction software.

TILINE PROBES. - The tiline probes, named so because of their use with the Mode S sensor, are used to detect the logic level which exists at the specific signal point to which the probe is attached. They consist of high-impedance differential amplifiers which isolate the signals from the CPMS equipment, are capable of detecting pulses of less than 10 nanoseconds in duration, and act as line drivers to the data collection unit. Each tiline probe unit contains the logic necessary to monitor six independent signals.

For Mode S data bus contention testing, one tiline probe unit was installed on the motherboard of each ensemble data bus, and two units were installed on each of the global data buses. The tiline probe units were wired to connectors on the Mode S sensor's front panel. Any six tiline probe units can be connected to the data collection unit simultaneously. Signal cables are 25 feet in length.

MEMORY ADDRESS PROBES. The memory address probes are used to detect memory address data on a 16-bit memory address bus and logic signals which indicate that valid address data are available on the bus. They connect to the breakpoint panel interface connectors on the Mode S sensor's front panel, and consist of high-impedance single-ended amplifiers which act as line drivers to the data collection unit. Twelve memory address probe units are available for simultaneous connection to the data collection unit. Signal cables are 25 feet in length. Each probe and cable is an integral assembly.

AZIMUTH PROBES. The azimuth probes consist of line drivers used to buffer the azimuth change pulse (ACP) and azimuth reference pulse (ARP) signals for distribution to the data collection unit. These probes are mounted in the Aircraft Reply and Interference Environment Simulator (ARIES), and are necessary for azimuth referencing of data collected from Mode S.

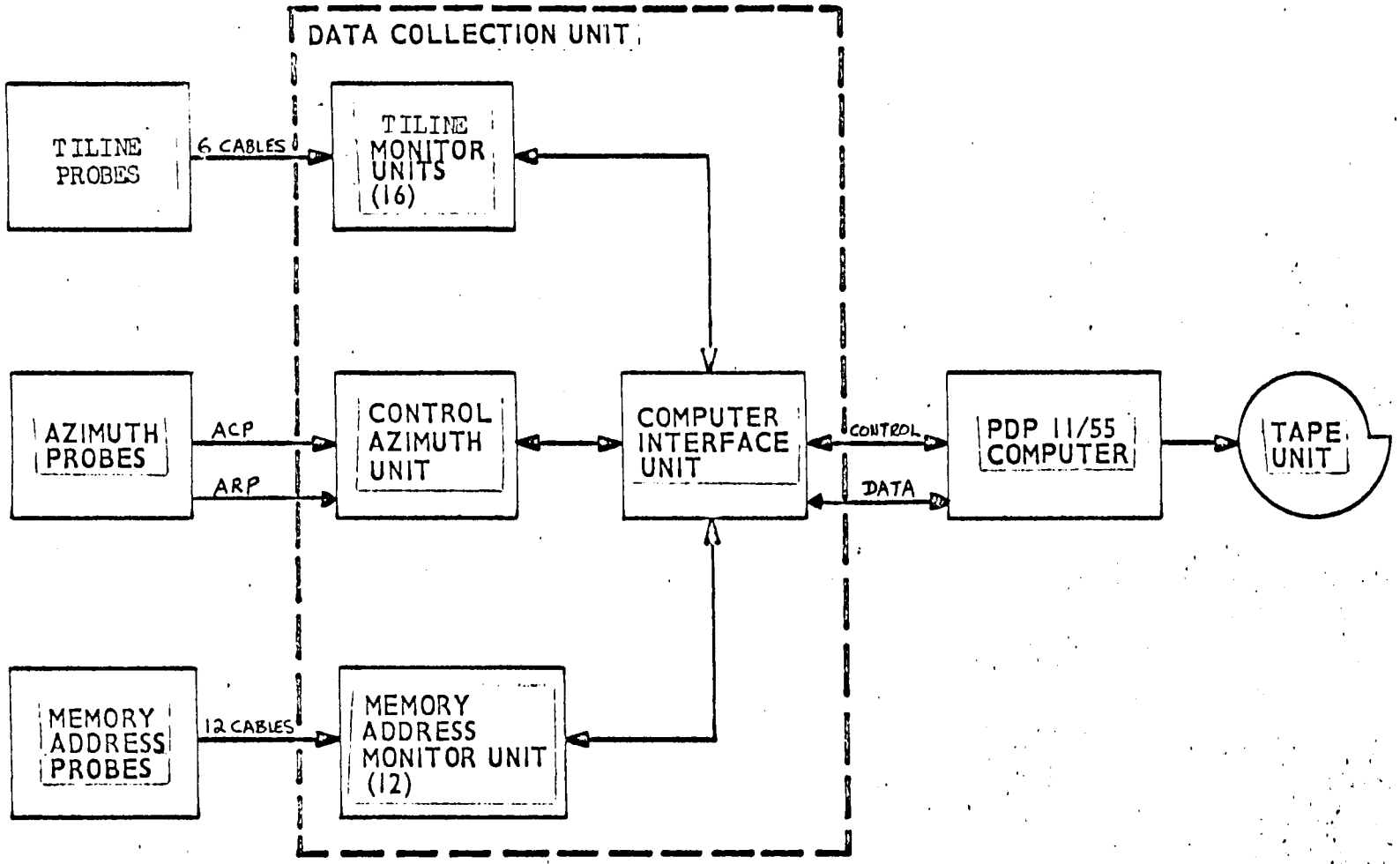


FIGURE 1. BASIC COMPUTER PERFORMANCE MEASUREMENT SYSTEM FUNCTIONAL BLOCK DIAGRAM

DATA COLLECTION UNIT. The data collection unit contains the logic necessary to monitor and process the data forwarded to it by the probe units. It consists of 16 tiline monitor units, 12 memory address monitor (MAM) units, a control/azimuth unit, and a computer interface (I/O) unit. A memory address splitter (MAS) option, and tiline patchboards are provided for use with the MAM and tiline units respectively. Also included is a hardware debugging tool known as the test system.

The unit is physically housed in a mobile 19 inch electronics rack enclosure. Present interconnection cabling lengths allow it to be located up to 50 feet from the PDP 11/55 computer.

Tiline Monitor Units. A block diagram of a typical tiline unit is shown in figure 2. Each tiline unit monitors a single signal and provides three separate measurements:

1. Iteration counts. The number of inactive to active transistions, or lead edges, that occur during a sample interval. The maximum iteration count is 65,536.

2. Elapsed time accumulated. A measure of the cumulative signal active time over the sample interval. The maximum elapsed time during a sample interval is 400 milliseconds.

3. Elapsed time sample. A measure of the duration of the first active period during a sample interval. The elapsed time sample counter is limited to 51 microseconds.

Counter clock frequency is 40 MHz., giving a resolution of 25 nanoseconds on all timing measurements.

Four special conditions are indicated and passed on as an aid in analysis of the data: (1) A signal lead edge but no trail edge, (2) Overflow on elapsed time sample, (3) Signal was active during the entire sample interval, and (4) Elapsed time accumulate counter active at sample time.

Tiline Patchboards. The signals to be monitored by each tiline unit are determined by a patchboard placed in the data collection unit. These patchboards route the signals form the six connected signal probe units to the individual tiline units. Presently there are 15 different patchboards which were wired for each combination of signals required during Mode S testing. Additional boards can be fabricated for almost any desired combination.

Memory Address Monitor (MAM) Units. Each MAM gathers data on the activity of a processor by providing information on the execution of software tasks. A typical MAM is depicted in figure 3. A MAM receives a 16-bit address, compares it to a previously stored set of addresses, and performs the following four measurements:

1. Address sample. The value of the first address detected during the sample interval.

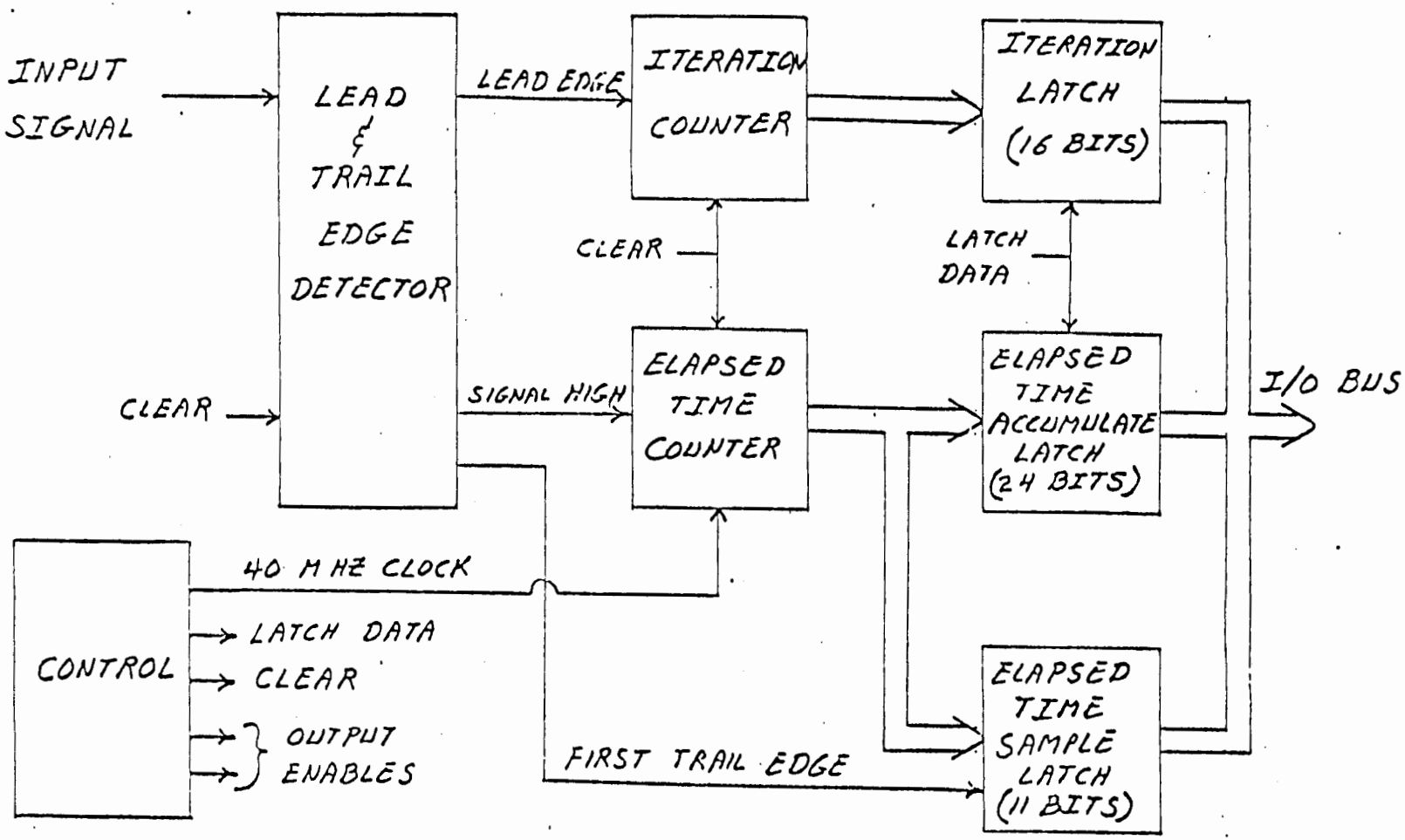


FIGURE 2. TILINE UNIT FUNCTIONAL BLOCK DIAGRAM

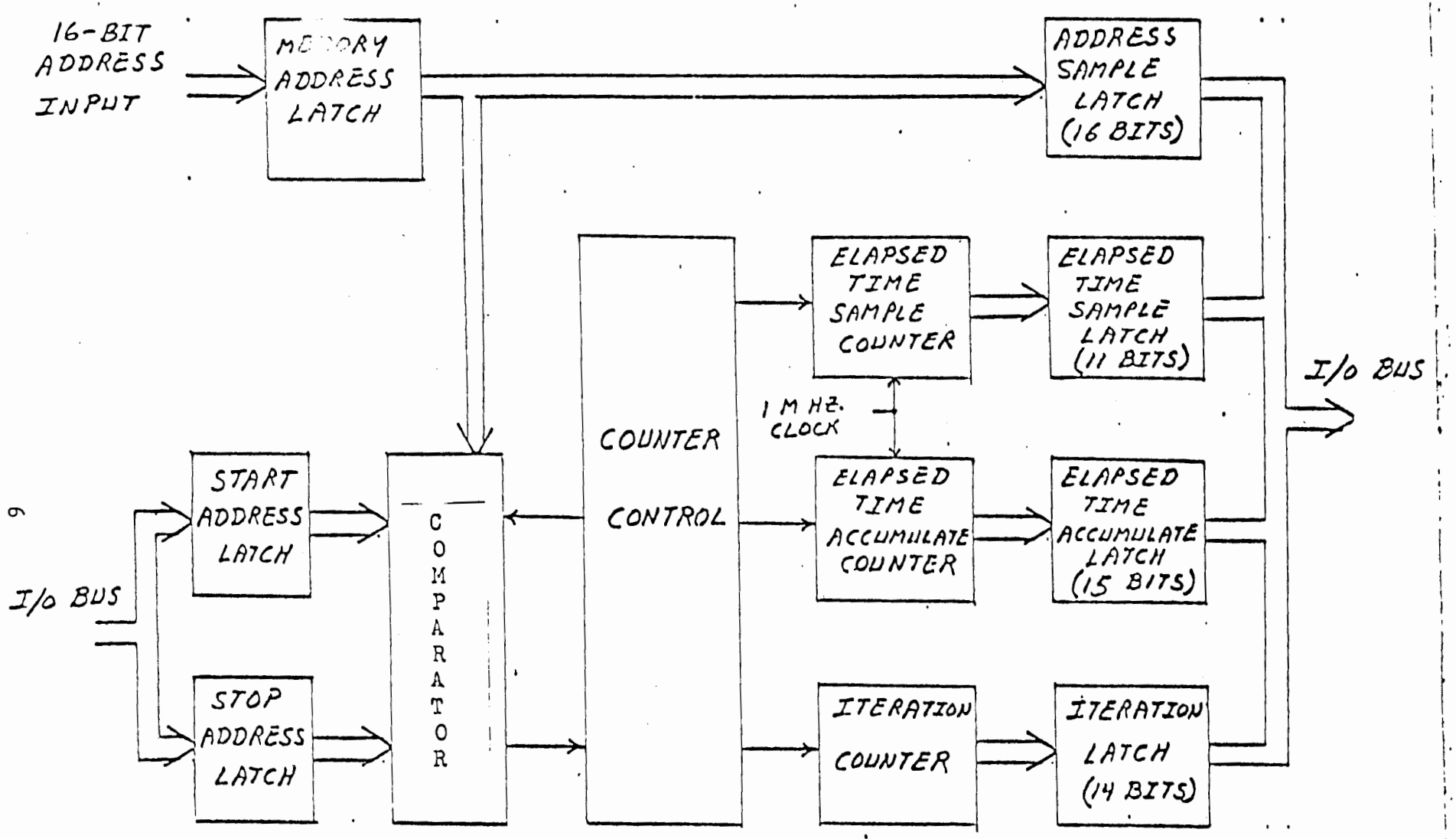


FIGURE 3. MEMORY ADDRESS MONITOR (MAM) UNIT FUNCTIONAL BLOCK DIAGRAM

2. Elapsed time sample. The time spent executing code between a start and stop address for the first occurrence of the address pair during the sample interval. The maximum elapsed time sample count is limited to 2 milliseconds.

3. Elapsed time accumulated. The time accumulated between a start and stop address pair during the sample interval. The maximum allowable time accumulated is 32 milliseconds.

4. Interation counts. The number of occurrences during the sample interval. There are three separate user selectable interation counter modes: (a) Start/stop address pairs, (b) start addresses, and (c) stop addresses.

All time measurements are made with a resolution of 1 microsecond.

Three special conditions are reported and passed along with the data for use in analysis: (1) A start address but no stop address occurred during the sample interval, (2) Overflow on elapsed time sample counter, and (3) The entire sample interval was spent between the start and stop addresses.

Memory Address Splitter (MAS). The MAS is an important option of the data collection unit. It enables a user to monitor more than one start/stop address pair per memory address probe. Without the MAS, only one memory address probe can be used per MAM unit. Also, since only one memory address probe can be connected per Mode S processor, use of the MAS allows timing of multiple software tasks within the same processor. Up to twelve different sections of code within the same processor can be monitored simultaneously. The MAS has several configurations, and can be used with multiple probes.

Control/Azimuth Unit. The control/azimuth unit controls the overall operation of the data collection unit, and monitors the ACP and ARP signals to determine the exact azimuth of the Mode S sensor. A block diagram of this unit is shown in figure 4.

Three system clocks are generated, 40 MHz., 10 MHz., and 1 MHz. for use by the tiline units, control logic, and MAM units respectively. This unit contains the logic for the generation of the system sample command which defines the length of a sample interval. This is a programmable counter that can count down via time or azimuth depending on user selection.

Azimuth gating of data transfers is also controlled here. Data can be inhibited when not between user specified start and stop azimuths. The azimuth counter is incremented on an ACP and reset on an ARP. In addition, the contents of this counter are included in every data sample so that each data set can be associated with an azimuth.

When the control/azimuth unit detects the end of a sample interval it causes the current contents of all the tiline units and MAM units to be latched into output registers. These units are then reset and a new sample interval started.

Computer Interface Unit (I/O). The system I/O is a 1 MHz., 16-bit parallel interface between the data collection unit and the PDP 11/55 computer. It actually consists of two units, one for control of the data bus, and the other for the transfer of data to and from the PDP 11/55. During system initialization this interface is used to transfer control information from the computer to the data

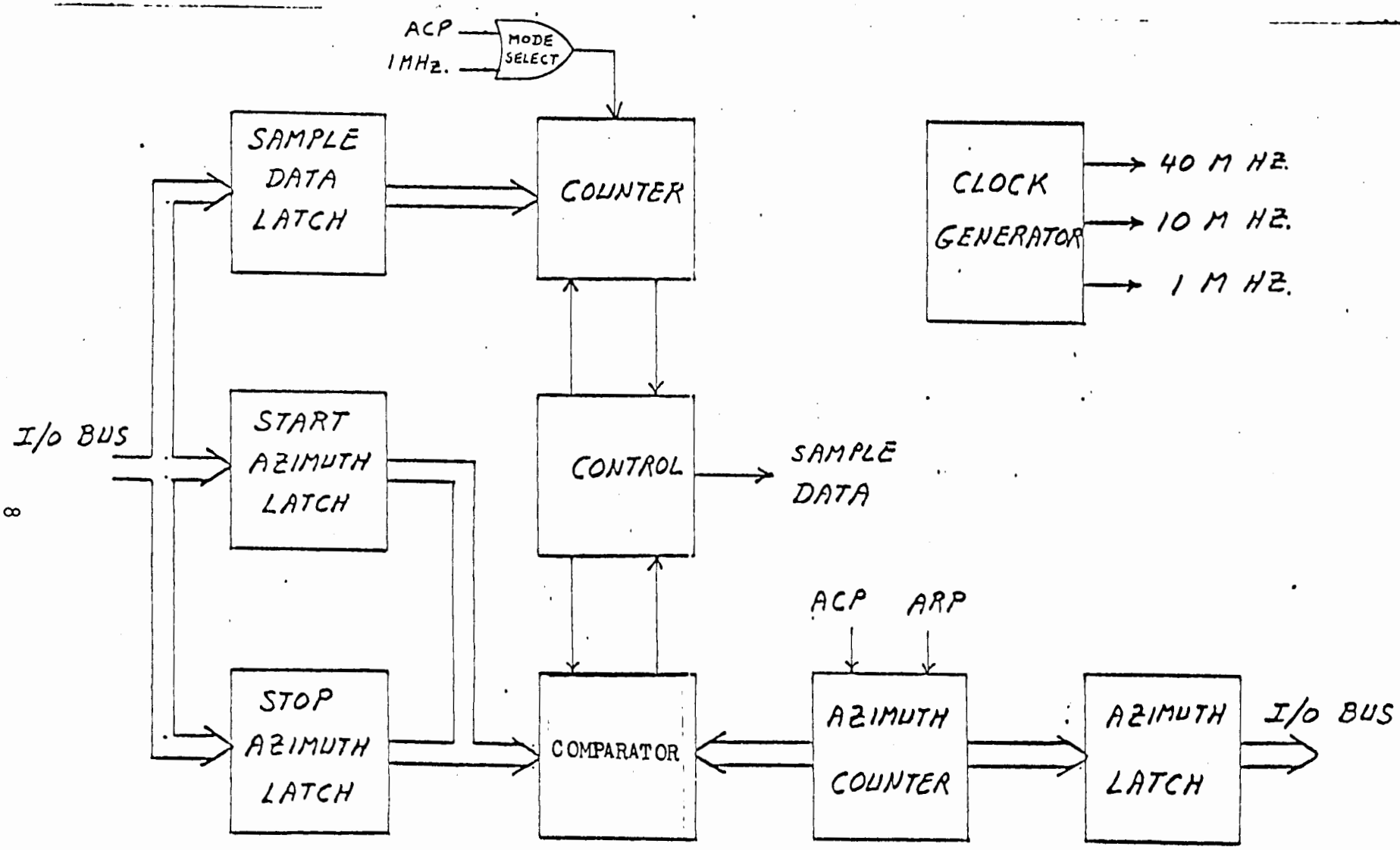


FIGURE 4. CONTROL/AZIMUTH UNIT FUNCTIONAL BLOCK DIAGRAM

collection unit. This control information specifies which of the 28 monitor units are to collect data, whether the sample interval is to be specified in time or azimuth, the length of the interval in either time or ACP's, and the azimuth window over which data is to be collected.

The I/O is notified by the control/azimuth unit each time data are latched into the output registers of the monitor units. Once in the output registers, these data are then sequentially transferred to the computer under I/O control.

Test System. The test system is a powerful hardware debugging tool that is resident in the data collection unit. It can be used for data collection by itself, since it is basically a miniature version of the main data collection unit. The test system consists of the following units:

Tiline monitor unit
Tiline simulator
Tiline probe cable tester
MAM unit
Random Address Generator (RAG)
MAM probe/cable tester
Computer simulator

1. Tiline Simulator. The tiline simulator provides known signals for use in checking the operation of a tiline unit. It is actually a programmable position pulse generator. All pulses will be a constant width as selected by a set of switches. Sixteen different pulse widths are available varying form 100 nanoseconds to 1.6 microseconds in 100 nanosecond increments. Pulse spacing information is stored in a programmable read-only memory (PROM). Single pulse trains with frequencies of 10 kHz., 80 kHz., and 200 kHz. are available via switch selection.

2. Tiline Probe Cable Tester. During normal test system operation, a jumper board forms a direct wire connection from the data output of the tiline simulator to a tiline unit. A tiline probe cable with a suspect malfunction can be checked via removal of this board and substitution of the cable in its place. The front panel of the data collection unit contains plugs for this purpose. Each of the six signal pairs used in a tiline probe cable can be checked individually via rotary switch selection on the front panel.

3. Random Address Generator (RAG). The RAG provides a pseudo-random set of address that can be input to a MAM as an aid in debugging. Of the many address loops available thru the RAG, one has been measured and documented. By loading the appropriate start/stop address pair into a MAM, the loop can be sampled, counted, and timed. The collected data can later be checked for accuracy.

4. MAM Probe/Cable Tester. Normally, a jumper board provides a one-to-one connection between the output of the RAG and the address input lines of a MAM. A MAM probe and cable can be tested via removal of this board and substitution of a MAM cable. Plugs are provided on the front panel for this purpose.

5. Computer Simulator. The computer simulator card intercepts output data from the I/O and responds with signals in the same manner as the PDP 11/55. In this way, a system check can be made without the computer. Two

switches located on the card are used to control system operation. All system data inputs such as sample interval, number and type of monitors to be enabled, etc are stored in a PROM. This card need not only be used with the test system, but can be used in conjunction with the main data collection unit if so desired.

PDP 11/55 COMPUTER. The PDP 11/55 is used to control operation of the CPMS, record the data received from the data collection unit onto magnetic tape, and perform off-line data reduction. The following peripherals are included: removable disk drive, tape drive, video display terminal, Tektronix display terminal, and Tektronix hard copy unit.

FORTRAN and assembly language are the two languages used in the programming. Four main program types exist: (1) Configuration, (2) Real time data collection, (3) Data reduction, and (4) Diagnostic.

Configuration Program. This program requires user interaction via keyboard to establish a configuration file on disk for use by the real time program. It first requests a filename, and searches for this file on disk. If the file is not found, one is created. Next, several options are listed on the display. These options include enabling or disabling tiline units and MAM's, definition of an azimuth window and sample interval, print file, and close file. There is also a help function which list the various functions available. Additional functions are incorporated to assist a user. One places an identification message in a created file, while another calculates the system utilization ratio. This ratio indicates system throughput so that the amount of data collected does not exceed system capability. It also allows the user to maximize his data collection close to 100% of system capability.

Real Time Data Collection Program. The real time data collection program is run during testing to control the system. It's first task is to acquire the desired configuration file from disk and send the configuration to the data collection unit. The program prompts the user for run identification and date, and outputs the system configuration to tape. Once the system is set up for processing, the program continues by buffering data, outputing data to tape, and updating a real time display.

The real time display is updated each scan and is an aid in identifying problems during a test. This prevents the collection of invalid data due to improper initial conditions. Data for all 16 tiline and 12 MAM units are displayed showing the percentage of time a signal was active during the scan, and between start and stop addresses respectively. Also, the number of signal or address iterations, hardware errors and overflows, and tape errors and overflows are displayed.

Data Reduction. The present data reduction package runs on the PDP 11/55 or on a PDP 11/45 computer. Both plot and data summarization programs are available. The plot programs are designed for use with a Tektronix display terminal and hard copy unit. Each program allows the following where technically feasible: (1) Definition of data to be analyzed by scan interval, (2) Azimuth filtering, (3) Interactive plotting with user defined abscissa and ordinate limits, and (4) Plots of the minimum, maximum, and the mean observed element.

Seven programs are currently available, performing reduction in the following areas:

Tape Configuration
Signal time and count distribution
Address frequency distributions
Data summarization
MAM counts/times
Processor loading versus azimuth
Processor loading versus scan number

1. Tape Configuration. This program provides a printout of the system configuration used during the data run. This is a copy of the file defined in the configuration routine. Figure 5 is a sample printout showing the file name, identification message, azimuth window, sample interval rate, all tilines disabled, 11 MAM's enabled with an interation mode of 1 for start/stop address pairs, and sample address pairs.

2. Signal Time and Count Distributions. These are histograms of the percentage of signals sampled versus signal duration, or occurrence. The x- and y-axis values are used definable to program limits.

The numbers on the x-axis should be multiplied by 25 nanoseconds to derive the correct time units in the Mode S tiline time sample distribution depicted figure 6.

3. Address Frequency Distributions. Figure 7 is a histogram of global memory addresses accessed by a Mode S processor. Each axis is user definable, with the x-axis in hexadecimal. These plots were used in the study of global memory address space utilization in Mode S.

4. Data Summarization. These summaries are applicable to tiline and MAM units. Data is provided for a selected scan interval, and may be filtered in azimuth. The following is included in each printout: (1) Probe number, (2) The mean time percentage and standard deviation, (3) The mean count of occurences and standard deviation, (4) Minimum and maximum times, (5) Minimum and maximum counts, (6) The number of elapsed time sample underflows and overflows, and (7) The total number of samples taken. The printout shown in figure 8 lists sample data for 10 MAM units.

5. MAM Counts/Times. This is a printout of raw data for MAM's on a per scan basis, where the number of scans dumped is user selectable. The following information is listed for each monitor: (1) The number of samples taken, (2) The total time in microseconds spent between start and stop addresses, and (3) The total number of iterations.

6. Processor Loading Versus Azimuth. Figure 9 depicts the percentage of processor utilization versus azimuth. Each axis is user definable to program limits. These plots were used to study Mode S processor loading in relation to air traffic density.

7. Processor Loading Versus Scan Number. In figure 10, the percentage of processor utilization versus scan number is plotted. The x- and y-axes are user definable. Up to 400 scans of data can be incorporated in one plot. This program

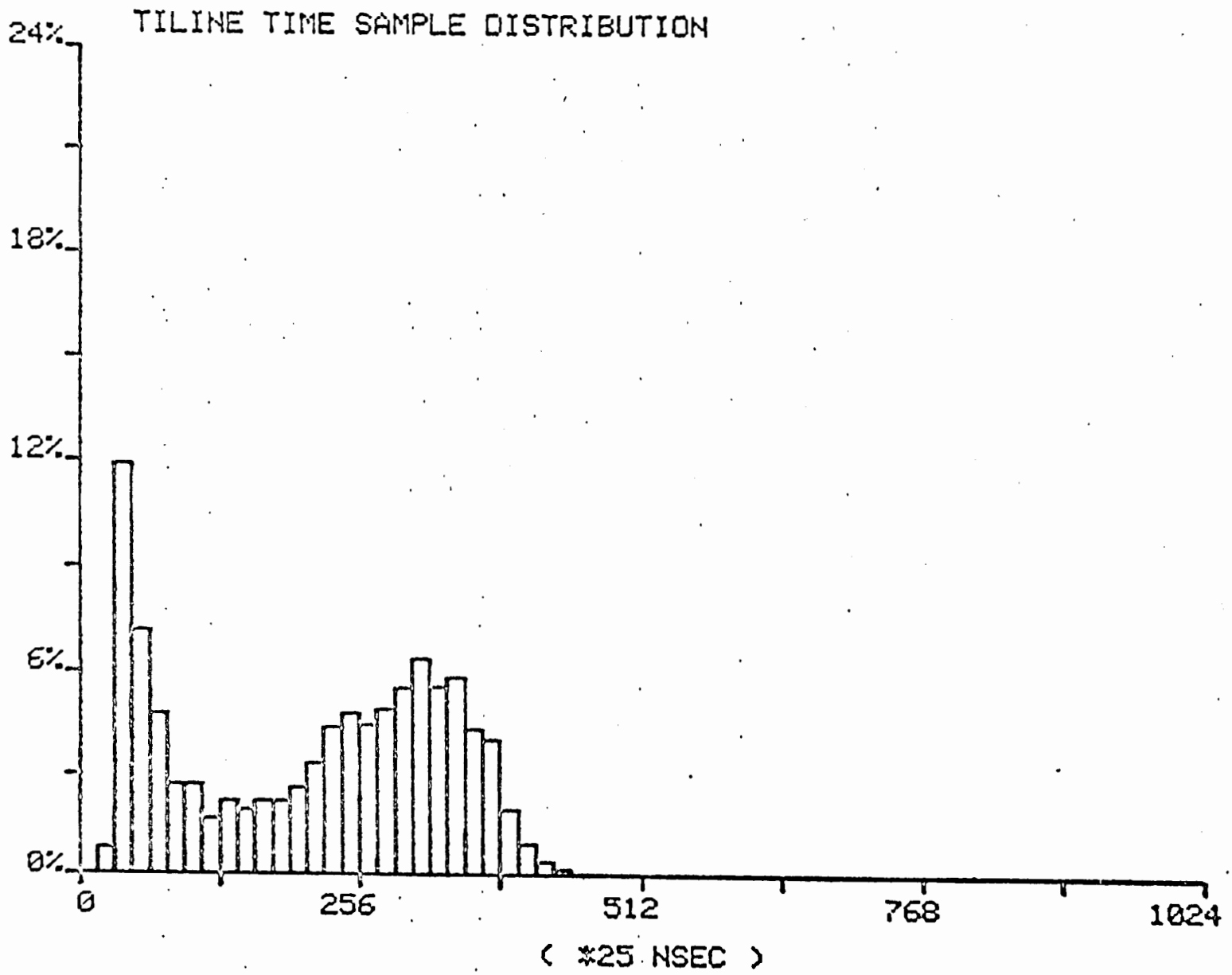
PEP1

THIS IS WHERE THE CONFIGURATION IDENTIFICATION WOULD BE

THIS IS WHERE THE RUN IDENTIFICATION WOULD BE
AZMUITH WINDOW IN DEGREES 270- 358
RATE IN CYCLES - 100

TIE LINES	ADDRESS LINES	START	STOP	AIC MODE
0 - DISABLED	0 - ENABLED	2010	205C	1
1 - DISABLED	1 - ENABLED	2062	2102	1
2 - DISABLED	2 - ENABLED	21BE	220E	1
3 - DISABLED	3 - ENABLED	0B60	0B64	1
4 - DISABLED	4 - ENABLED	0B28	0BA6	1
5 - DISABLED	5 - ENABLED	0BA6	0C40	1
6 - DISABLED	6 - ENABLED	0DF2	0E08	1
7 - DISABLED	7 - ENABLED	0F2E	0E52	1
8 - DISABLED	8 - ENABLED	14D8	155A	1
9 - DISABLED	9 - ENABLED	0CD4	057E	1
10 - DISABLED	10 - ENABLED	0F3E	102E	1
11 - DISABLED	11 - DISABLED			
12 - DISABLED				
13 - DISABLED				
14 - DISABLED				
15 - DISABLED				

FIGURE 5. TAPE CONFIGURATION PRINTOUT



SIGNAL DURATION

FIGURE 6. MODE S TILINE TIME SAMPLE DISTRIBUTION

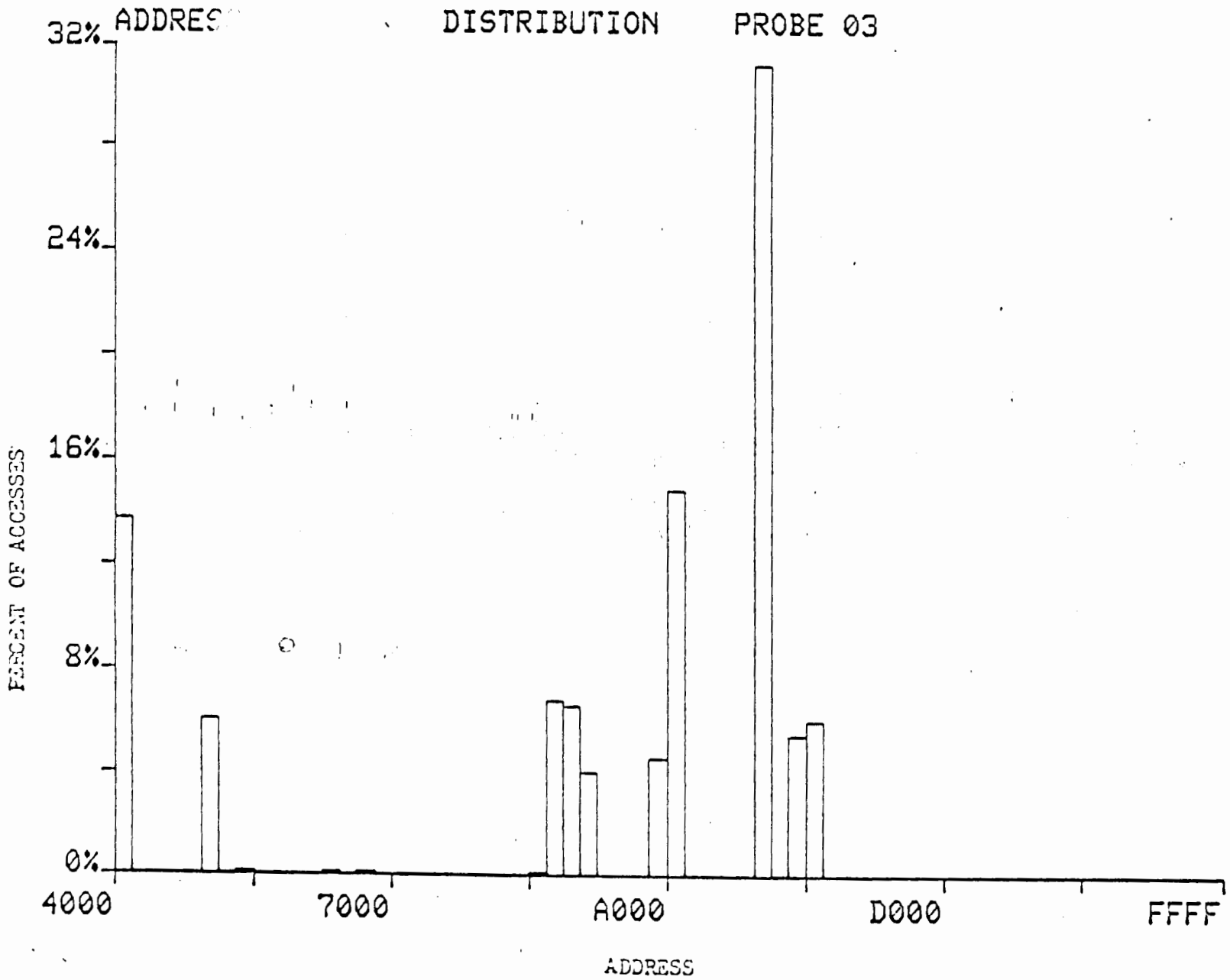


FIGURE 7. ADDRESS FREQUENCY DISTRIBUTION

THIS IS WHERE THE RUN IDENTIFICATION WOULD BE

THIS IS WHERE THE CONFIGURATION IDENTIFICATION WOULD BE

SKIP 0 SCANS - DUMP 5 SCANS AZIMUTH 270-359

PROBE	MEAN TIME (PERCENT)	S. D.	MEAN COUNT (PER SCAN)	S. D.	MINT (RAW COUNTS)	MAXT	MINC	MAXC	ETS OF	ETS UF
A 0	0.14	0.00	148.6	0.9	9	21	0	3	0.0	1.2
A 1	96.34	0.48	7.0	0.7	50	1262	0	3	0.7	95.3
A 3	1.34	0.28	148.4	0.9	72	1521	0	3	0.0	1.4
A 4	7.28	0.01	5860.2	29.2	12	220	18	54	0.0	0.0
A 5	42.37	0.05	5859.6	29.1	69	250	18	54	0.0	0.0
A 6	7.24	0.03	5869.8	29.1	12	25	21	55	0.0	0.0
A 7	62.69	0.16	158.2	1.1	852	1071	1	5	96.7	0.0
A 8	17.08	10.63	16.0	1.6	66	2025	0	4	0.5	93.4
A 9	87.88	0.36	148.6	0.9	148	174	0	4	92.1	3.1
A10	0.31	0.03	10.4	0.9	202	483	0	4	0.0	94.5

579. SAMPLES

FIGURE 8. DATA SUMMARIZATION PRINTOUT

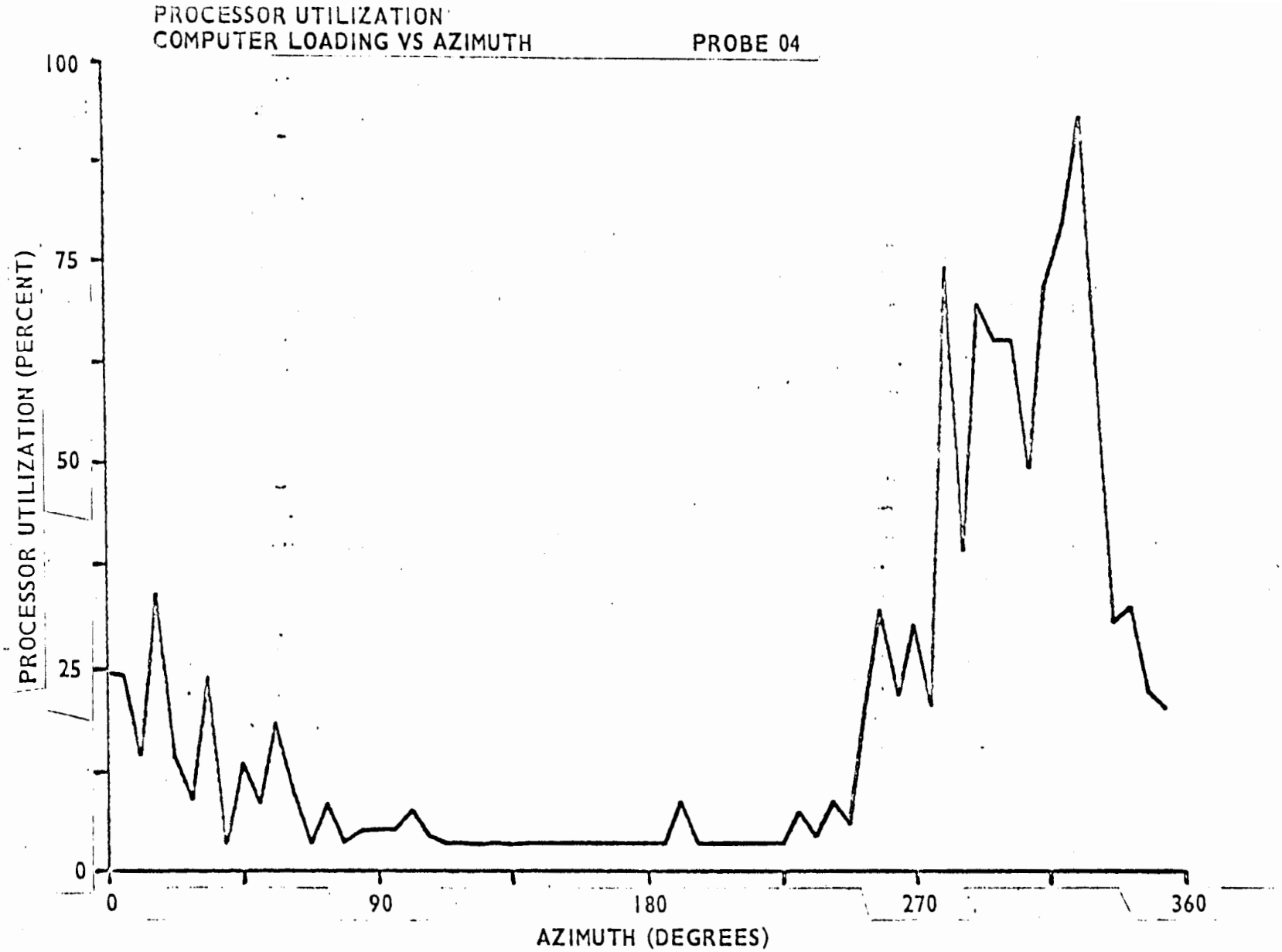


FIGURE 9. PROCESSOR UTILIZATION VERSUS AZIMUTH

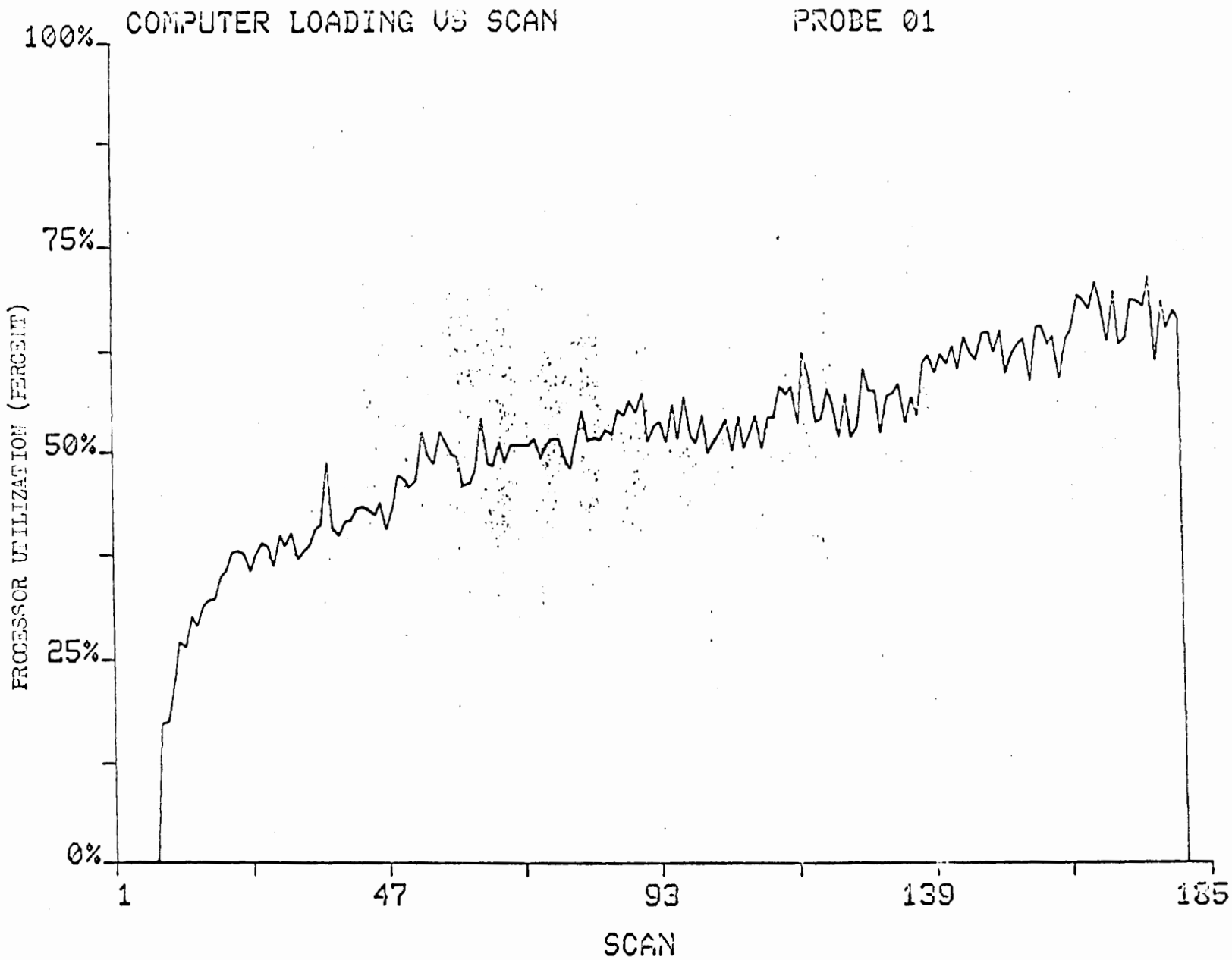


FIGURE 10. PROCESSOR UTILIZATION VERSUS SCAN NUMBER

is of great value when the input load varies as a function of scan number, and aids in determining which loading conditions cause a processor to saturate.

Diagnostic routines. The diagnostic routines are used for testing of the interface between the PDP 11/55 and the data collection unit.

SYSTEM SAMPLE INTERVAL LIMITATIONS. The real time data collection program uses a multiple buffering input technique and the hardware has a First-In-First-Out (FIFO) output buffering element. A system utilization ratio is calculated in the configuration routine to caution a user of possible system misuse. The permissible sample interval size, or sample rate, is a function of the number of monitors used. Table 1 is a representative list of the number of monitors versus the maximum allowable sample rate.

TABLE 1. NUMBER OF MONITORS VS. SAMPLE RATE

No. of Monitors	Maximum Allowable Sample Rate (Hz.)
28	138
26	148
24	160
22	174
20	190
18	210
16	235
14	266
12	307
10	363

SYSTEM UTILIZATION.

The CPMS was used to measure the performance characteristics of the Mode S sensor's computer subsystem distributive architecture. The specific performance areas investigated were: System data bus contention/utilization, global memory address space utilization, and processor utilization. All tests were conducted with a fixed Mode S software package being excercised under simulated traffic scenario inputs generated by the ARIES.

Delays experienced on global memory accesses due to contention between processors and the utilization of the data buses as a function of system loading were measured during data bus contention/utilization testing. Tiline probes tiline patchboards, tiline monitor units, and azimuth probes were used in this effort. Figure 6 depicts the access delays for one particular Mode S processor on an ensemble data bus.

The intent of the global memory address space utilization testing was to determine what portion of a 24,576 word address space reserved for global memory accesses was actually being utilized by each Mode S processor. These data were used to study the potential impact of expanding the current 8,192 word processor local memory to 12,288 words or greater. Figure 7 is an example of one Mode S processor's global address map showing unused portions of memory. Memory address probes, MAM units, and azimuth probes were utilized in these tests.

Processor utilization testing consisted of measuring the percentage of time during which each processor was actively processing data. The Mode S sensor software executes continuously by looping through each of the subtasks checking global memory it finds data to be processed. Each subtask was studied

and broken down into sequences of code which reflected the presence of real work. A code sequence to be measured was identified in the CPMS as a start/stop address pair. Figure 9 depicts the percent of processor utilization versus azimuth for one particular Mode S processor. Memory address probes, MAM units, azimuth probes, and the MAS option were used for this testing. A more complete description of the test and evaluation effort using the CPMS is contained in Report No. FAA-RD-81-12.

The CPMS can be used further as an aid in determining the efficiency of newly developed software, in determining the effectiveness of software enhancements, and anywhere a high resolution digital counting and timing device is needed.

SUMMARY.

The CPMS was originally designed to measure the performance characteristics of the computer subsystem distributive architecture within the Mode S engineering model sensors built by TI. In general, the CPMS consists of a DEC model PDP 11/55 computer with peripherals, a data collection unit, and probes for connection to the Mode S sensor. Processor signals of interest and memory address data can be monitored to gather information on the execution of software tasks. In addition, an integral test system is included to aid in isolating hardware faults. The collected data can be reduced off-line via a data reduction package which runs on a PDP 11/55 or on a PDP 11/45 computer. A Mode S test and evaluaiton effort was conducted using the CPMS, which proved to be a versatile tool for collection of numerous types of system parameters.