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Advanced Automation Program HOST Computer System Acquisition Phase Acceptance Test Report for Contract No. DTFA01-85-C-00030

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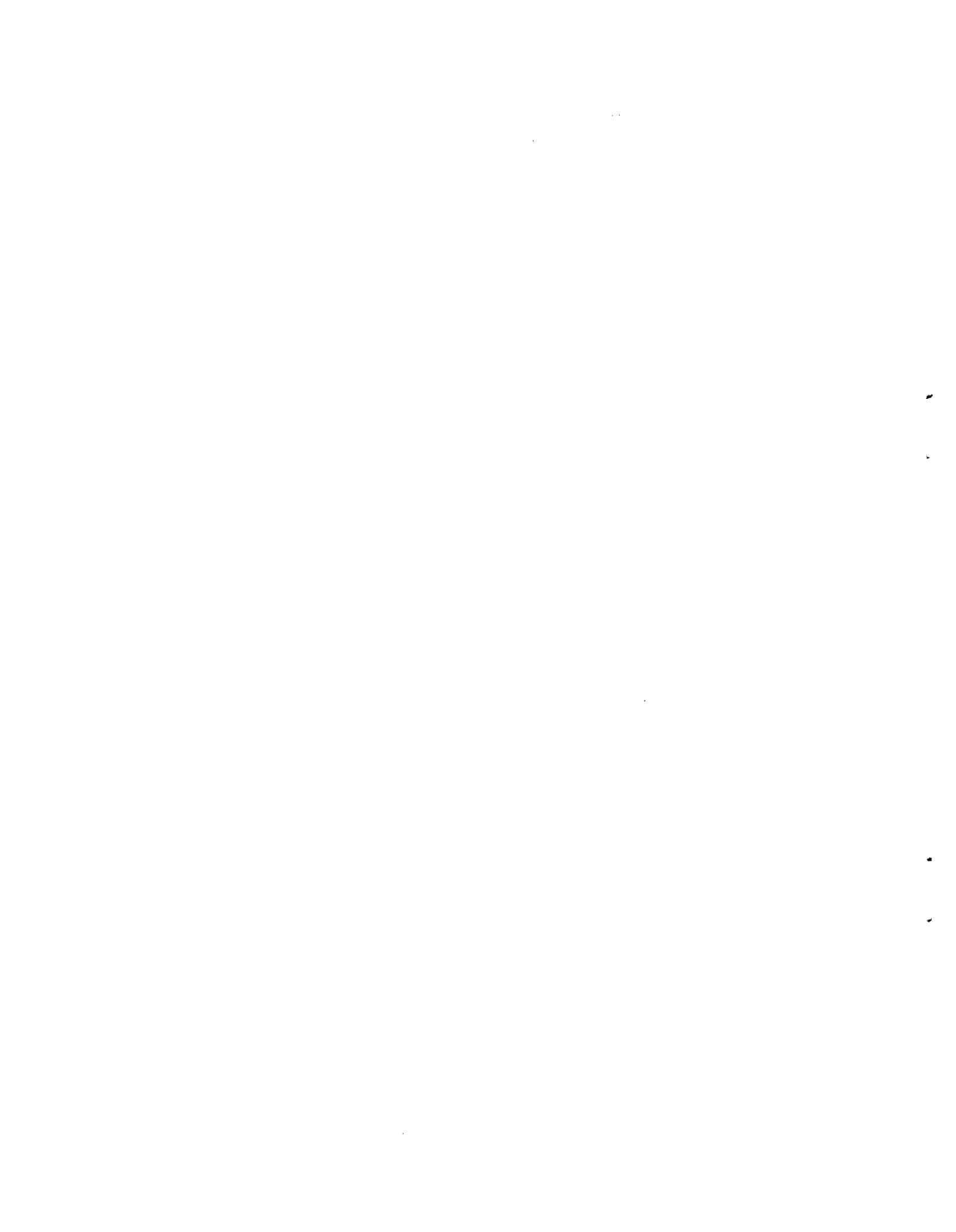
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16. Abstract <p>This report summarizes the results of the Acceptance testing conducted during the Host Computer Acquisition Phase (AP) performed by IBM under contract number DTFA-01-85-C-00030. These tests were conducted at the Federal Aviation Administration (FAA) Technical Center beginning on September 17, 1985 and ending with FAA system acceptance on November 21, 1986. The Government lead in the Host acquisition acceptance testing was ACT-130, the Advanced Automation Branch located at the Technical Center. The tests were described in the Engineering Requirements of the Host AP Contract and were partitioned into three series: the Hardware/Systems tests, the Support Software tests, and the Operational Software tests. All tests were conducted by an IBM test team and witnessed by FAA and FAA support contractor personnel. This report describes the test objectives, the detailed analysis methods, and the results obtained during the AP testing.</p>			
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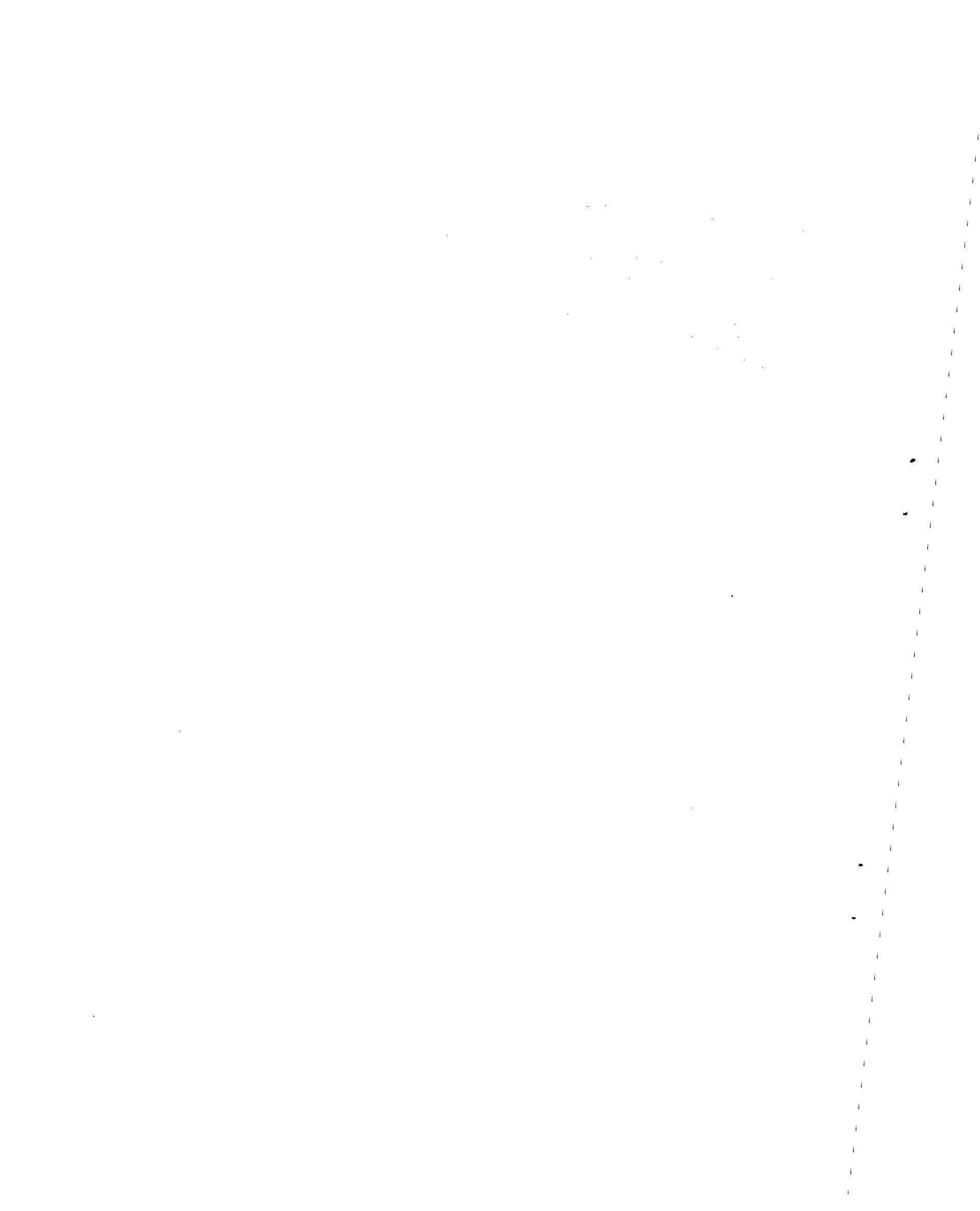


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EXECUTIVE SUMMARY

This report documents the Federal Aviation Administration's (FAA's) Acceptance testing conducted at the FAA Technical Center, Atlantic City International Airport, NJ, during the Acquisition Phase (AP) of the HOST Computer System (HCS) procurement. The contract for this procurement was awarded to IBM under contract number DTFA01-85-C-00030.

Acceptance testing addressed in this document was only part of the total HCS test program conducted at the Technical Center. Additional HCS test programs included Failure Mode Testing (FMT), Site Simulation Testing, and Reliability, Maintainability and Availability (RMA) analysis; all of which contributed to the final Technical Center acceptance decision. This decision was necessary to begin installation of the HCS at the 20 Air Route Traffic Control Centers (ARTCC), the first being the Seattle, Washington Center.

Procurement of the HCS is the initial step of the Advanced Automation Program to upgrade the Air Traffic Control (ATC) systems to meet the needs of the projected Air Traffic load of the 1990's. The HCS program provides modern off-the-shelf equipment to replace the mid-sixties vintage 9020 Computer Systems at all 20 ARTCC's. Three systems were used for testing at the FAA Technical Center. The System Support Facility (SSF) System, the Central Support and Software Development (CS/SD) System, and a Reliability, Maintainability, Availability (RMA) System. The RMA System is the 20th system and was advanced delivered to the Technical Center.

The lead on all HCS Technical Center testing was the Advanced Automation Branch, ACT-130. ACT-130 in cooperation with all concerned FAA HCS development and maintenance organizations; i.e. ATR, ALG, and APM established an "Integrated Test Team" to monitor and evaluate the total test program at the Technical Center. In addition to permanently assigned FAA and support contractors (MITRE, RCA, SEI, and RMS) personnel, at least 219 FAA regional personnel from all 20 ARTCCs contributed to the HCS testing. Test team members evaluated IBM produced test plans and procedures in accordance with FAA prepared review guides, witnessed both dry and formal test runs, and performed test data analysis both jointly with IBM and independently. Internal test reports were prepared documenting results as determined by the FAA personnel. These reports contributed to the main body of this document.

The strategy employed in the HCS contract requirements was to duplicate the entire current 9020 NAS ATC systems with no loss of capability. This included all support, maintenance, and NAS operational system software. This approach also allowed a major portion of test results verification to be accomplished by a comparison of HCS data to identical 9020 test data. In excess of 450

reels of magnetic tape containing NAS systems source code, scenarios, and test comparison data were prepared and delivered to IBM for conversion. In addition, 30,000 pages of supporting documentation were delivered to the contractor to update as necessary to document the operation and maintenance of the HCS.

Formal testing commenced September 17, 1985 and concluded at the FAA Technical Center on November 21, 1986. During this period, 79 formal tests were completed including 12 Regression Tests. Prior to each formal test conduct, contractor dry runs were monitored, system data captured, and final decisions made as to test readiness.

Hardware tests were repeated for each of three systems installed; SSF, RMA, and CS/SD. All NAS operational software tests and the majority of the support software tests were conducted on the SSF system, the facility most closely resembling an ARTCC configuration. The FAA directed Site Simulation and FMT were accomplished on the RMA system.

FAA test teams worked closely with IBM on each of the formal tests beginning with receipt of the preliminary delivered test plans and procedures. Technical Interchange Meetings (TIMs) were held frequently to ensure that proper environments, interfaces, and procedural actions, were taken and that designated requirements were verified.

All problems uncovered during Testing were documented in Problem Trouble Reports (PTR). Daily FAA/Contractor PTR review meetings were held to determine the impact of each problem and to categorize its criticality. All problems that impacted mission performance were considered the most critical and were corrected and verified before system acceptance at the FAA Technical Center.

The HCS was stressed extensively while interfacing with the FAA equipment found at the operational facilities and its capability of replacing the 9020 System was conclusively demonstrated. By simulating the airspace of 6 ARTCC's, confidence was established that the system was adaptable to the varied environments of the 20 ARTCCs located throughout the Continental United States. The ease at which HCS implementation are proceeding are the direct results of the extensive testing conducted at the Technical Center.

In summary, the Host test effort at the FAA Technical Center was very extensive and highly successful. At the time of this writing, six En Route sites are fully operational with the new Host system. This can be attributed to the testing performed at the FAA Technical Center.

This report covers the details of the Acceptance Testing. Details of the Site Simulation and Failure Mode tests are covered in separate documents. To assist a non-technical reader, each test section of this report contains a general language overview of the test purpose and its results.

1 INTRODUCTION

1.1 BACKGROUND

The HOST AP is the extension of the HOST Design Competition Phase (DCP) in which competing contractors demonstrated their ability to provide modern off-the-shelf instruction compatible computer hardware replacements for the FAAs En Route Air Traffic Control (ATC) Central Computer Complex (CCC) systems, and to convert the associated software for use in the new HCS's. The current 9020 systems, in use at 20 En Route Centers, were developed in the 1960's to process radar and flight data, enabling air traffic controllers to maintain safe separation standards, and to manage the flow of aircraft in the air space between airports.

The continuing growth of air traffic since the 9020s were installed has put a heavy burden on the system, and this growth is projected to continue to increase through the 1990's to the year 2000. Software enhancements under development that would provide a level of automation, efficiency, and additional safety could not be implemented due to limitations in the processing capabilities of the 9020s. Further, the cost and availability of spare parts for these aging systems are an increasing problem affecting the reliability of the 9020 system.

The HCS replacement program is being implemented in two phases: (1) a Design Competition Phase, and (2) an Acquisition Phase in which software was converted, tested at the FAA Technical Center, and installed at En Route Centers.

The DCP indicated that the rehosting of the current ATC operational software to an off-the-shelf state of the art computer system was a viable solution to solve immediate problems for the FAA. The DCP was conducted between IBM Corporation and Sperry Corporation from September 1983 thru July 1985. Both companies submitted proposals following the competition and IBM was selected to produce the production units.

The AP represented the production phase in which the system to be delivered to the 20 En Route Centers was developed and demonstrated. This report details the results of testing conducted at the FAA Technical Center prior to implementing the HCS at the 20 En Route Centers.

1.2 SCOPE

This report addresses the formal acceptance test program conducted by IBM and witnessed by the FAA and its support contractors beginning on September 17, 1985, and ending with FAA Technical Center acceptance on November 21, 1986.

The acceptance test program consisted of three essentially independent test phases:

- Phase 1: Hardware/System Tests
- Phase 2: Nonoperational Software Tests
- Phase 3: Operational Software Tests

Phase 1 consisted of seven test areas to demonstrate Engineering Requirements related to manufacturing design practices and standards, system installation, and system interfaces.

Phase 2 consisted of 11 test areas demonstrating Engineering Requirements relative to converted or replaced support and maintenance software and associated monitors and operating systems.

Phase 3 consisted of eight test areas demonstrating Engineering Requirements associated with the rehosted NAS Operational Software including the NAS Monitor, Applications, and COMPOOL.

All tests were conducted at the FAA Technical Center. Many of the 26 test areas were repeated, as deemed necessary by the government, to demonstrate proper functional operation.

1.3 TEST GUIDELINES

All tests were conducted in accordance with the Engineering Requirement, section 4.0, Test Requirements. Test descriptions contained in this report are excerpts from the specific test requirements contained in that section of the HOST contract where applicable. Tests were conducted using the following guidelines.

All test plans, procedures, and scenarios were submitted by the contractor and approved by the government prior to test conduct. Pretest briefings were conducted by the contractor and attended by the FAA and its support contractor personnel. Changes and deviations from approved test plans, procedures and scenarios were discussed and approved by the government.

IBM test dry runs were observed by the FAA test leaders or their representatives in order to provide familiarity with test procedures, expected results, and to assess the readiness of the system and software for formal tests. Early in the test program, the need for a method of rigid control and identification of software Build levels became obvious. In particular, a method was needed to ensure that a software baseline established upon the successful completion of the dry runs would be maintained through the formal tests.

Procedures were developed to capture the baseline software used at the last successful dry run for each test area and restored this software into the HCS at the start of formal testing. This process was called bonding.

Prior to the start of formal testing, the FAA QRO and/or FAA test leaders verified and documented the System Hardware Configuration and Software Version being used including Simulation and Data Reduction.

During test conduct, all variations in observed expected results, as documented in test procedures, were recorded as anomalies. As a result of anomalies, the FAA and the contractor conducted a brief on-the-spot analysis to determine the impact on the test. In cases where the impact was deemed minor, the test was continued. In cases where the impact was considered major, the test was aborted and rescheduled. All hard copy data produced during the tests was made accessible to the FAA within 24 hours.

Post-test briefings addressed all pertinent aspects of hardware, software and test documentation and included as a minimum the following topics:

- a. Preliminary analysis of test responses and results.
- b. Anomalies encountered and their impact on test results.
- c. Planned and unplanned deviations and changes to test procedures.
- d. Test logs.

Extensive data analysis was conducted by the FAA and its support contractors primarily by comparing the outputs of the hosted system to government furnished special test cases of similar software run on the 9020 system. Differences between the 9020 and HOST outputs were considered anomalies. These anomalies were investigated and those determined to be a problem were entered into the INFO Problem Management system for resolution.

The contractor provided Quick Look test reports for each test, summarizing the important test results and briefly highlighting any discrepancies noted during test conduct including their significance. These reports were reviewed by the FAA and its support contractor test leaders and were found to be in conformance with witness logs and government findings.

The final test reports provided by the contractor identified and evaluated discrepancies between expected and actual results encountered during test conduct and as a result of post-test analysis. All anomalies were documented. The FAA and its support contractor test leaders reviewed the format, content, and completeness of these reports prior to the FAA's approval.

1.4 HOST COMPUTER SYSTEM GENERAL DESCRIPTION

The HCS, which replaces the IBM 9020 A and D based CCC of the En Route system, consists of both hardware and software functions divided into a primary and a support subsystem.

A primary processor subsystem and a support processor subsystem comprise the two similar and distinct portions of the HCS. The primary processor subsystem performs the ATC operational software tasks while meeting the response time and workload requirements specified. The support processor subsystem performs multiple support tasks concurrently under the Virtual Machine Control Program (VMCP). These tasks include a hot standby NAS ready to take over operational processing in case of primary subsystem failure, a test NAS used to baseline new versions, support software and maintenance software. The software breakdown is shown in Figure 1, HOST Computer System Software Architecture.

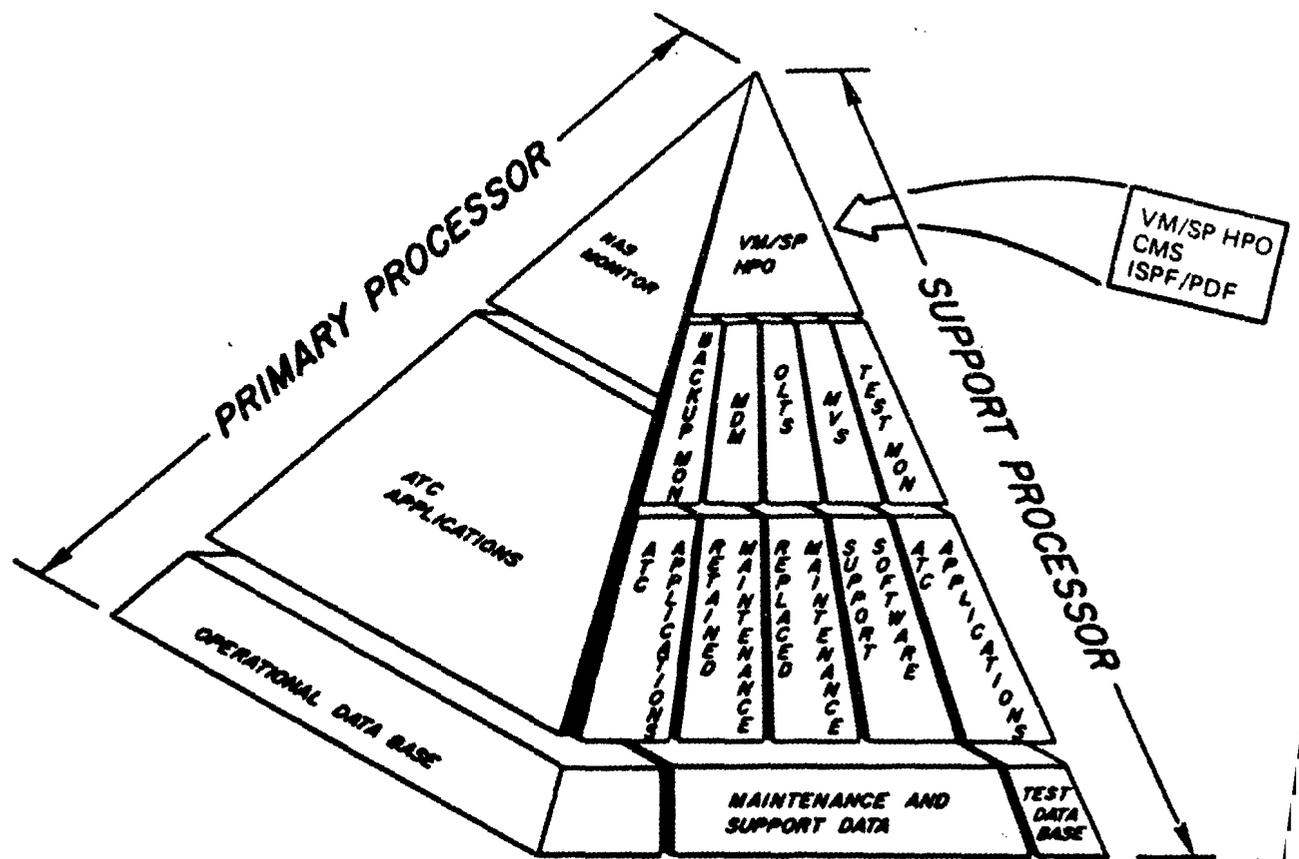


FIGURE 1. HOST COMPUTER SYSTEM SOFTWARE ARCHITECTURE

The HCS hardware replaces the 9020 era equipment with current technology-based equipment and incorporates fully redundant hardware units and subsystem and unit interfaces. The HCS is comprised of the following major hardware subsystems:

- a. Processor Subsystem (two each) - The central data processing function is performed by the processor subsystem which is comprised of the central processing unit (CPU), memory and input/output (I/O) channels.
- b. Peripheral Subsystem (one each) - The operator machine interface function is facilitated by the peripheral subsystem which is comprised of keyboard video display terminals (KVDTs), console printers (KPRs), high speed printers (HSPs), magnetic tape equipment, and controllers.
- c. System Control and Maintenance Subsystem (SCMS) (two each) - The system control and maintenance function is performed by means of the system control and maintenance support processor. This is a processor with interfaces to the processor subsystem and, via communication link, to a central support facility.
- d. Direct Access Storage (DAS) Subsystem (one each) - The on-line storage function is performed by the DAS subsystem which is comprised of disk controllers and disk drives.

The components of the En Route System hardware that will be retained include the display channels, computer display channel (CDC) or display channel complex (DCC), and the peripheral adapter module (PAM) and its adapters. The interface between the HCS and the display channel is provided through a switch management system. The PAM is accessed by the HCS through the utilization of a configuration control register (CCR) translator to ensure signal level compatibility and an I/O channel for data transfer to the PAM. During the transition period from 9020 to HCS, a transition switch will permit either the 9020 or HCS to communicate to the display channel and PAMs as shown in Figure 2, En Route Facility Transition Switch Function.

The HCS software consists of the existing NAS programs which are modified/converted as required to operate with the new processor subsystem and new contractor-provided software including a Virtual Machine Control Program (VMCP). These programs will be used to provide the operational, support, and maintenance software requirements of the HCS. The HCS operational software utilizes the present NAS operational software consisting of the monitor, applications and COMMON POOL (COMPOOL) converted to run in the HCS.

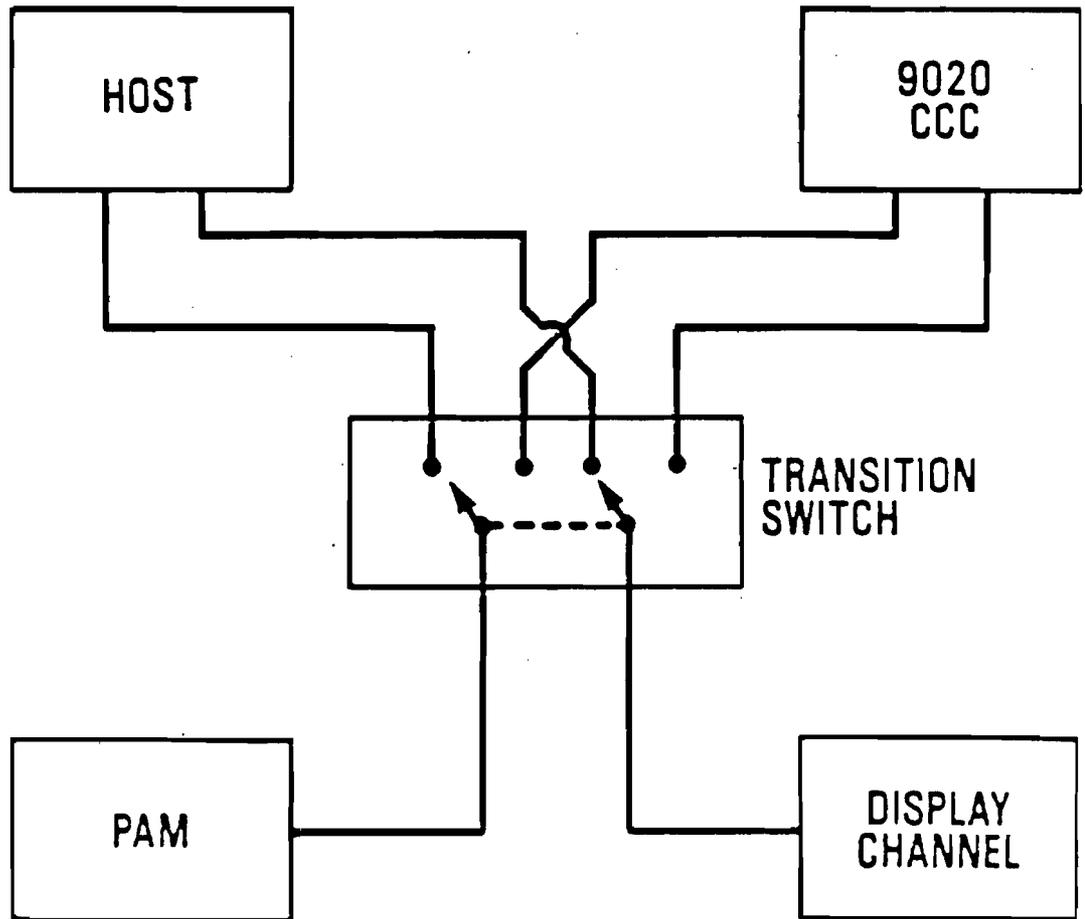


FIGURE 2. EN ROUTE FACILITY TRANSITION SWITCH FUNCTION

The HCS support software has the capabilities to modify, build, test, and verify all of the HCS software and is usable with the HCS operational software. The current support software with the modifications or additions necessary for the new features or new equipment constitute the HCS support software.

The HCS maintenance software provides the hardware diagnostics for all HCS hardware elements and peripheral devices and includes the current NAS maintenance software with modifications and additions, as necessary, for the new equipment and interfaces. The maintenance software can be site-adapted to reflect the HOST site's unique equipment configuration.

1.5 HCS DETAILED HARDWARE CONFIGURATION

The acceptance series of tests was conducted at the FAA Technical Center using the System Support Facility (SSF), Central Support/Software Development (CS/SD) and Reliability, Maintainability, Availability (RMA) systems for the Hardware/System tests and the SSF system for the Nonoperational Software tests and the Operational Software tests. The SSF and CS/SD are the systems that will be used as the FAA Technical Center support facility. Figure 3, HOST Computer System Block Diagram, shows the layout of the hardware units.

The model numbers and components utilized in the HCS are:

Processor Subsystem

- 3083-BX1 Improved Processor 16 MB
- 3087-001 Coolant Distribution Unit
- 3089-001 Power Distribution Unit

System Control and Maintenance Subsystem (shown as part of Processor Subsystem)

- 3082-X16 Improved Processor Controller

Peripheral Subsystem

Tape Equipment

- 3420-005 Magnetic Tape Unit
- 3480-A22 Cartridge Tape Control Unit
- 3480-B22 Cartridge Tape Unit
- 3803-002 Tape Control

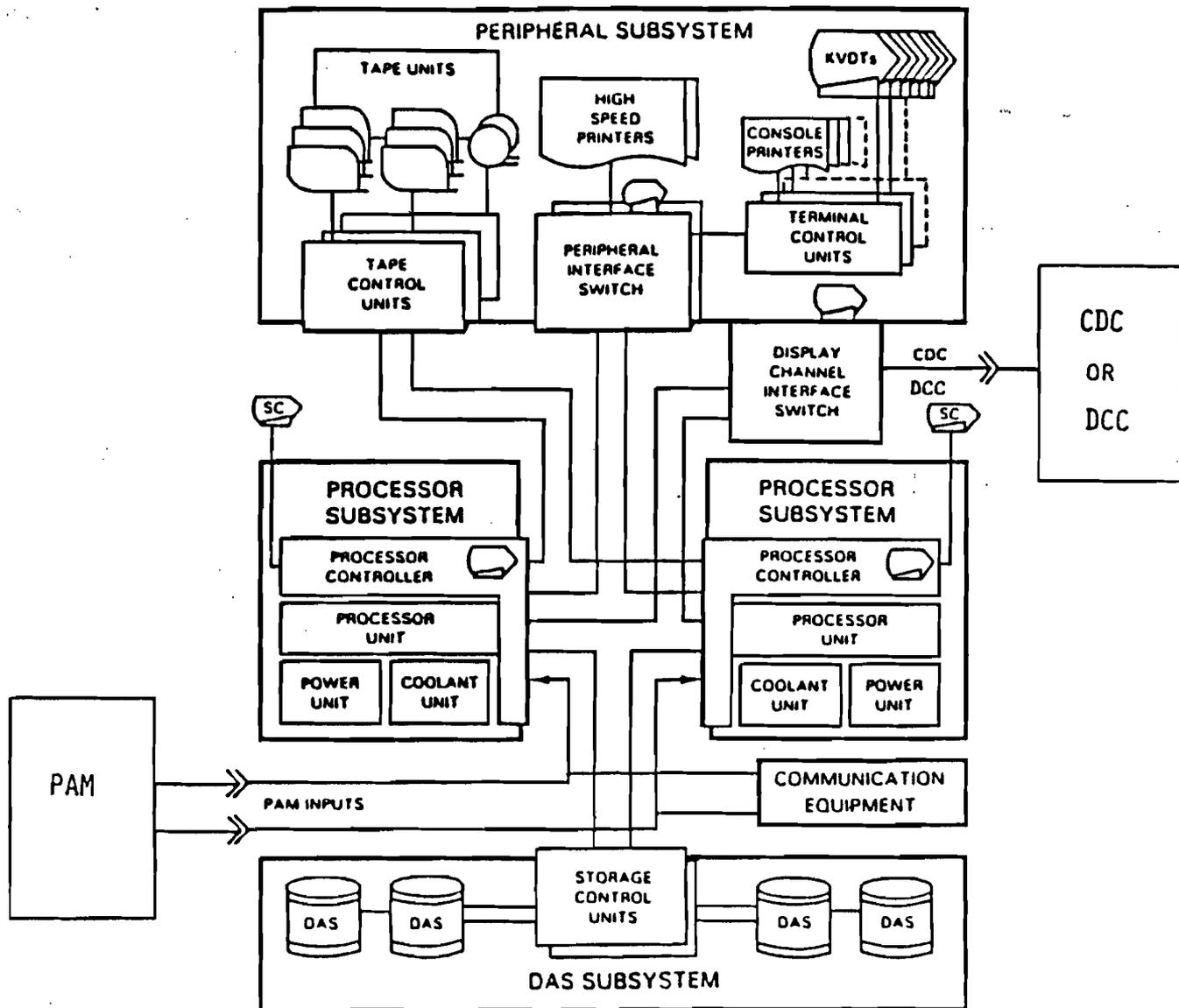


FIGURE 3. HOST COMPUTER SYSTEM BLOCK DIAGRAM

Printer Equipment

4248-001 Printer

KVDT and Console Printer Equipment

3274-D41 Terminal Control Unit
3180-110 Keyboard Video Display Terminal
3278-A02 Display Console
3268-C02 Console Printer

Communication Equipment

3725-002 Communication Controller
3727-700 Communication Console
3864-002 4800/2400 BPS Switched Modem

Direct Access Storage Subsystem

3380-AD4 Direct Access Storage
3380-BD4 Direct Access Storage
3880-003 Storage Control

Switch Management Equipment

3274-D41 Terminal Control Unit
3180-110 Keyboard Video Display Unit
3814-A01 Switching Management System

Transition Equipment

3180-110 Keyboard Video Display Unit
3814-A01 Switching Management System
3814-B01 Switching Management System

Other Equipment

4805-B03 CCR Signal Translator
4805-B04 CCR Signal Translator
4805-A04 CCR Signal Translator

2 HARDWARE/SYSTEM TESTS

Hardware/System Tests consisted of 7 tests areas:

Performance
Element

Subsystem
System
Electronic Interface
System Interface
Host/9020 Transition

The Engineering Requirement for the HOST Computer System specified that Fabrication Inspection and Design Qualification tests would be performed on all noncommercially available hardware units. As the HOST System consists only of commercially available hardware units, these tests were not conducted. The remaining hardware unit test, Performance, was conducted on the RMA System, a system totally representative of a field installation.

System tests consisted of installation and checkout tests (Element tests, Hardware Subsystem tests, and Hardware System tests) to demonstrate that the newly installed HCS was operating and ready to begin interactive testing with the government furnished PAMs and Display Channel Equipment. Table 1 shows test conduct dates for Hardware/System Tests.

TABLE 1. HARDWARE/SYSTEM TESTS

TEST NAME	SSF (1985)		RMA (1985-1986)		CS/SD (1985-1986)	
	FORMAL TESTS	RETESTS	FORMAL TESTS	RETESTS	FORMAL TESTS	RETESTS
PERFORMANCE	N/A	N/A	8 NOV 4 APR	N/A	N/A	N/A
ELEMENT	18 SEP 19 SEP	N/A	31 OCT	N/A	18 DEC	N/A
SUBSYSTEM	23 SEP 24 SEP	N/A	1 NOV 3 NOV	N/A	18 DEC	N/A
SYSTEM	23 SEP 24 SEP	1 OCT	4 NOV	6 NOV	19 DEC	7 JAN 10 JAN 19 FEB 15 JUL
ESI	18 SEP 19 SEP	29 OCT	14 NOV	N/A	19 DEC	N/A
SYSTEM INTERFACE	18 SEP 20 SEP 23 SEP 24 SEP	N/A	1 NOV 5 NOV 6 NOV 7 NOV	N/A	17 DEC 6 JAN 7 JAN	N/A
HOST/9020 TRANSITION	24 SEP	N/A	5 DEC	N/A	N/A	N/A

The sections which follow provide details on the Hardware/System tests.

2.1 PERFORMANCE TESTS

2.1.1 Overview

The purpose of Performance testing was to verify each configuration item type's ability to meet the specified characteristics of the engineering requirements. Performance testing as applied to the Host configuration included such items as: printer speeds, print clarity, and character strings validity of the printers, data transfer rates of the tape units, visual clarity and character strings validity of the terminals, fault isolation capabilities of the control processor, disk storage capacities and data transfer rates, and cable length requirements. The environment in which the Performance testing occurred required the processor interface to generate data and, in selected test cases to execute data transfer rate algorithms.

All Performance tests were held on November 8, 1985, with the exception of a special test to verify character requirements for the terminal displays and the terminal console printers. The special test was held on April 4, 1986. All engineering requirements pertaining to Performance tests were verified on these two dates.

2.1.2 Test Description

Performance tests verified that the HCS hardware units performed in accordance with the requirements specified in sections 3.7.1.2.1 through 3.7.1.2.3 of the Engineering Requirement.

These provisions establish the performance characteristics for the Primary and Support Processor Subsystems, the Direct Access Storage Subsystem (DASD), KVDT, console printers, line printers, magnetic tape equipment, and the SCMS processors.

DASD error detection and retry requirements verification were deferred to Reconfiguration testing. Processor million instructions per second (MIPS) rate requirement verification was deferred to the Capacity and Response Time tests.

Seventy engineering requirements were verified as a result of the Performance tests.

2.1.3 Success Criteria/Analysis Method

Error free analysis of all the hardcopy output, visual observations, stop watch timings, and test drivers determined a successful Performance test. Analysis methods were:

- a. Stop watches for timing on-line and console printer speeds.

- b. Printer outputs from Performance test software to verify character set train, printer quality, alignment, and carriage control characters.
- c. Visual observation of terminal display requirements.
- d. Action queue entry data from the maintenance position to verify error retention analysis.
- e. Listings from console printers for alignment and quality printing requirements.
- f. Test drivers run under Multiple Virtual Storage (MVS) to verify DASD and magnetic tape data rates.

2.1.4 Test Conduct/Results

2.1.4.1 Reliability, Maintainability, Availability (RMA) System

Test conduct was held November 8, 1985, at 0900 hours. The Performance test was conducted in an orderly manner. Pretest audits were performed for all devices under test. The only modification to the already system tested RMA system configuration was 1000-foot cables to the KVDT and console printer under test replacing the standard cables.

All MVS supported testing started in the morning performed as described in the pretest briefing. Stop-watches were provided for the printer speed tests. DASD speed tests were software timed. The morning session was completed per schedule with no major anomalies.

The afternoon session consisted of processor error data retention and retry, element characteristics (KVDT, console printer, HSP printer), and configuration items to be verified by Performance testing. The afternoon session was concluded without major anomalies.

A special test to verify requirements for the NAS-MD-311 IOT character set and EBCDIC on the KVDTs and console printers occurred on April 4, 1986, to complete the Performance testing.

Analysis of all the hardcopy output, visual observations, and stop watch timing determined the results to be successful for the Performance testing. All Engineering Requirements allocated to the Performance test were verified.

2.2 ELEMENT TESTS

2.2.1 Overview

Element testing verified the capability of each individual configuration item to be powered on and execute self-contained diagnostics to assure readiness for system interface. Element testing required that all delivered items: processors, switches, and peripherals be individually tested to assure interface readiness.

Element tests were held on September 18-19, 1985, on the System Support Facility (SSF) System, on October 31, 1985, on the Reliability, Maintainability, Availability (RMA) System; and on December 18, 1985, on the Central Support/Software Development (CS/SD) System. All engineering requirements pertaining to Element tests were verified on these dates.

2.2.2 Test Description

The individual hardware elements (processors, peripherals, DAS) were tested according to the Contractor's normal installation procedures.

2.2.3 Success Criteria/Analysis Method

Each test of an element was a subset of the contractor's installation checkout procedures and contained the particular results that were expected. Successful completion of each set of checkout procedures constituted a successful test. On-line Test System (OLTS) was utilized to verify correct operation of processor, DAS, and tape elements. All other elements were tested with internal microdiagnostics.

2.2.4 Test Conduct/Results

2.2.4.1 System Support Facility (SSF) System

The SSF System Element tests were conducted on September 18 and 19, 1985. After three failed attempts to load the OLTS from tape, it was discovered that the 3274 controller for the maintenance console was not on-line. The tape loaded once the controller was commanded on-line. To expedite testing, the procedure sequence was modified to allow all elements requiring OLTS testing to be conducted sequentially. This deviation had no significant impact to the test. The as-run procedure was updated for the CS/SD and RMA systems test conduct.

All steps of the SSF System Element test were conducted successfully.

2.2.4.2 Reliability, Maintainability, Availability (RMA) System

The RMA System Element tests were conducted on October 31, 1985. All steps of the updated procedures were completed. OLTS and each element's internal microdiagnostics were used to verify all requirements. There was no 3864 modem installed on the RMA system.

The FAA waived testing this element since it was successfully tested on the SSF system. Additionally, the FAA agreed that the power off/power on procedure did not have to be repeated when testing the secondary 3083 processor.

All steps of the RMA System Element test were conducted successfully.

2.2.4.3 Central Support/Software Development (CS/SD) System

The CS/SD System Element tests were conducted on December 18, 1985. Again, the 3864 modem test and the secondary 3083 processor power off/power on procedure were waived by the FAA.

All steps of the Element test conducted on the CS/SD system were successful. All Engineering Requirements allocated to the Element test were verified.

2.3 HARDWARE SUBSYSTEM TESTS

2.3.1 Overview

Hardware subsystem testing verified each element of the subsystem was functional as a group and independently interfaced with the Host processor. This test was accomplished with diagnostics operating in the Host processor which, in addition to verifying the interface, also performs remote checkout of each configuration item in the subsystem. Subsystems tested were: processors, disk storage, magnetic tapes, communications, visual displays, and medium speed printers. Cluster controllers and programmable switches were tested as an integral part of the peripheral subsystems interface. The High Speed printer was essential to all subsystem tests as the output device for the diagnostics.

Hardware Subsystem tests were held on September 23-24 and October 1, 1985, on the SSF System, on November 1 and 5, 1985, on the RMA System, and on December 18, 1985, on the CS/SD System. All hardware subsystems performed correctly and interfaced properly with the Host processor.

2.3.2 Test Description

Diagnostic tests were run between each processor subsystem and the DAS subsystem and the peripheral subsystems to verify the correct performance and interface of each subsystem. Tests were performed to demonstrate that the DAS subsystem meets the performance requirements specified in section 3.7.1.2.2 of the Engineering Requirement. This provision establishes DAS characteristics such as configuration, transfer rate, interfaces to processor subsystem, and access mechanisms.

Hardware subsystem tests were used to verify that the subsystem equipment meets the environmental requirements specified in section 3.2.5 of the Engineering Requirement. This provision establishes

climatic service conditions such as temperature and humidity, electrical service conditions, and air cleanliness standards.

2.3.3 Success Criteria/Analysis Method

OLTS diagnostics running under the On-line Test Stand-alone Executive Program (OLTSEP) exercised each subsystem. The completion of each test and any errors encountered were displayed on a KVDT. Error-free results as observed at the KVDT were the expected success criteria.

2.3.4 Test Conduct/Results

2.3.4.1 System Support Facility (SSF) System

The Hardware Subsystem test was conducted on the A1 processor subsystems of the SSF system on September 23, 1985, and on the A2 processor subsystems on September 24, 1985. All steps of the government approved test procedure were successfully performed except for the 3725 Communication Controllers tests. The 3725 was successfully tested on October 1, 1985, when the system was free of VM users and each channel path could be tested.

Analysis of all test results verified the correct performance of the SSF hardware subsystems and the interfacing of each subsystem.

2.3.4.2 Reliability, Maintainability, Availability (RMA) System

The Hardware Subsystem test was conducted on the A5 processor subsystems of the RMA system on November 1, 1985, and on the A6 processor subsystems on November 5, 1985. The 3725 Communications Controller testing was not performed on November 1, 1985, because the proper address for the RMA system was not on the OLTS tape. A new tape was created and the test was run on November 5, 1985.

A "critical failure" indicated by the processor during the loading of OLTS on November 1, 1985, was determined to be an operator entry error. A cartridge tape drive failure was attributed to a defective cartridge tape.

Analysis of the test results verified the correct performance of the RMA hardware subsystems and the interfacing of each subsystem.

2.3.4.3 Central Support/Software Development (CS/SD) System

The Hardware Subsystem test was conducted on both the A3 and A4 processor subsystems on December 18, 1985. Since the CS/SD system has three additional DASD units and one additional communication controller, an approved procedure was implemented to test the additional elements. The procedure equated addresses of these units not recognized by the OLTS tape to known addresses.

Analysis of all test results verified the correct performance of the CS/SD hardware subsystems and the interfacing of each subsystem.

2.4 HARDWARE SYSTEM TESTS

2.4.1 Overview

Hardware systems testing is the ultimate level for the Host hardware testing with all procured equipment concurrently operational via an IBM system exerciser program, New System Test (NST). This test further verifies all cluster controllers and programmable switches and connections are operational and are correctly interfaced by Logical Device Number (LDN). Correct address verification an integral part of the NAS adaptations, is essential for subsequent operational tests.

Hardware System tests on the SSF System began September 23 and were completed with an FAA requested retest on October 1, 1985. The tests were begun on the RMA System on November 4, 1985, and completed with an FAA requested retest on November 6, 1985. The CS/SD System test was begun on December 19, 1985, but could not be completed until a cluster controller was correctly interfacing to the terminal console printers. A hardware modification resolved these problems successfully. All subsystems were verified as being properly integrated into a functional system on each final test.

2.4.2 Test Description

Hardware System tests were conducted with the complete complement of HOST hardware equipment. A diagnostic test was run which verifies that the functional subsystems (processor, DAS, and peripheral) are integrated into a functional system. This diagnostic test exercised all possible I/O channel paths and exercised all units in the system concurrently.

2.4.3 Success Criteria/Analysis Method

New System Test-2 (NST) release 4.4 diagnostic tests were run on each processor connected to a complete complement of HOST hardware equipment. The number of times each of the routines ran and any errors encountered were displayed at a KVDT. Error-free results as observed at the KVDT were the success criteria.

2.4.4 Test Conduct/Results

2.4.4.1 System Support Facility (SSF) System

The NST diagnostic used to accomplish the System test is a nondeliverable installation/checkout tool used principally for new installation checkout. It is a cumbersome diagnostic to proceduralize due to its excessive checks on all possible configurations based on all ranges of addresses whether or not used. Due to user complexities, numerous procedural deviations occurred relative to the use of NST. Also, NST is extremely demanding in exactness relative to the configuration hookups. This resulted in considerable number of anomalies that were quickly resolved, but required restarting NST for

each occurrence. As a result, the System test required considerable more time than anticipated, but did accomplish the desired results.

Testing began on September 23, 1985, and did not complete until October 1, 1985. The post-test briefing occurred September 25 at which time it was determined that the System test was not complete to the satisfaction of the FAA. To alleviate set-up problems for the System test, a configuration checklist was added to the procedure used for retest October 1, 1985, which concluded the SSF System tests.

All elements and the I/O channels were successfully tested without errors. Analysis of the test results verified that the HCS functioned as a system and no additional retests were required.

2.4.4.2 Reliability, Maintainability, Availability (RMA) System

The Hardware System test was conducted on the A5 processor and the A6 processor on November 4, 1985. Numerous anomalies attributed to incorrect set-up procedures were observed. Deviations to work around the set-up problems resulted in other anomalies. All anomalies were resolved except during the A5 processor testing; all printout to the high speed printer was lost. The test diagnostic NST had terminated printer output after receiving a band check report. The FAA test team deemed it necessary to rerun the entire test of the A5 processor on November 6, 1985. The test was rerun successfully with no configuration or set-up problems. However, an unexpected interrupt was reported from address 0264 (a device which does not exist). A problem report was written, but was closed on December 12, 1985, when the interrupt could not be recreated.

Analysis of the test results verified that the test was successful.

2.4.4.3 Central Support/Software Development (CS/SD) System

Hardware System testing was performed using NST diagnostic program to exercise all I/O interfaces in each processor of the CS/SD system. Testing performed on December 19, 1985, was unsuccessful due to errors on tape drives (0A91, 0A92) and DASD (UA0827). Investigation revealed that these devices were still executing NST from a previous test run and were unavailable for the test run that failed. Retest was scheduled for January 7, 1986, at which time various printers (connected to the same controller) were inadvertently dropping from "Ready" status. A second retest was scheduled for January 10, 1986.

Prior to retesting on January 10, 1986, IBM informed the FAA test team that the problem (HIPR 640) opened concerning the printers dropping "Ready" during testing had not been resolved.

Testing continued without anomalies. However, the printer problem (HIPR 640) remained an open issue and had to be resolved prior to final acceptance of the CS/SD system hardware.

A defective interface board was discovered in a KVDT of the CS/SD system. This board was considered to be the cause of the printers

dropping "Ready". A test was scheduled on February 19, 1986, to verify the solution. The test was run three times and failed each test run.

Although this problem was only observed on the CS/SD system, it was determined that the problem was caused by the design of the 3724 Cluster Controller. A hardware modification was applied to all Cluster Controllers and the verification of the solution was successfully conducted on July 15, 1986.

2.5 ELECTROMAGNETIC AND ELECTROSTATIC TESTS

2.5.1 Overview

Electromagnetic and Electrostatic testing is critical to the Host configuration to assure proper grounding of all equipments, whether the equipment is directly tested or associated through interconnection cabling. The criticality of this testing is further amplified at the ARTCC's where a system is operational 24 hours a day, 7 days a week. To assure there is no interference to the 9020 CCC System while field testing of the HCS, electrostatic testing of the Host is accomplished prior to transition switch hook-up with the 9020 CCC system despite having separate ground connections. To accomplish this test, an Electronic Discharge Simulator instrumentation is required. 7000 Volts are discharged in an operational environment while all Host equipment is exercised utilizing the installation/checkout program, NST. 12000 volts are discharged in a non-operational environment with all equipment connected.

The Electromagnetic and Electrostatic tests on the SSF System were held on September 18-19, 1985, with a retest on October 29, 1985. The RMA System was tested on November 14, 1985. The CS/SD System test began December 19, 1985, with a retest on December 20. All final tests were run successfully without any reported errors or incidents.

2.5.2 Test Description

Tests were performed which provide the validation of the HOST Computer System/Subsystem Electrostatic Interference (ESI) and Electromagnetic Compatibility/Electromagnetic Interference (EMC/EMI) performance requirements as specified in section 3.3.2 of the Engineering Requirement. This provision establishes characteristics such as compatibility and equipment degradation.

ESI testing was performed on the following elements:

- 3083 Processor
- 3082 Processor Controller
- 3480 Cartridge Tape Unit

3420 Magnetic Tape Unit
3380 Direct Access Storage Device
3880 Storage Control Unit
3814 Switching Management System

2.5.3 Success Criteria/Analysis Method

Selected units were injected with electrostatic interference. Diagnostics were run prior, during, and after each voltage injection. Error-free results, as observed at the maintenance printer while listing the Action Queue entries, were the success criteria for the processors, and NST error indicators for the peripherals.

2.5.4 Test Conduct/Results

2.5.4.1 System Support Facility (SSF) System

The Electrostatic Interference test was conducted on September 18, 1985, (A1 processor) and September 19, 1985, (A2 processor). Errors were observed when the 3380 DAS unit of the A1 processor was injected with electrostatic interference. HIPR No. 31, DAS ESI failure, was opened. All other units successfully met the ESI engineering requirements.

The DAS unit was eliminated from testing on the A2 processor until a solution to the problem was found. All other units of the A2 processor were tested successfully.

IBM discovered that the manufacturer's recommended procedure for attaching a ground strap between the EDS-200 Electrostatic Discharge Simulator and the unit under test was not followed.

On October 29, 1985, the complete test was successfully run using the ground strap. HIPR No. 31 was closed and no further retests were required.

2.5.4.2 Reliability, Maintainability, Availability (RMA) System

The RMA System Electrostatic tests were conducted on November 14, 1985. Electrostatic voltage testing was confined to the processor, controller, and DAS ground in both the operational (7KV) and nonoperational (12KV) modes. The DASD was included in this test due to problems occurring on the previously tested SSF system.

Each unit was successfully tested with no reported errors.

2.5.4.3 Central Support/Software Development (CS/SD) System

The CS/SD System Electrostatic tests started on December 19, 1985. Steps were added to the approved test procedure to load VM on the

secondary processor and have VM running while electrostatic discharges were applied to the primary processor. During the test run a "System Reset" was observed on the high speed printer. The test was suspended and HIPR 582 was written against the test. Investigation revealed that the "System Reset" was a normal condition. The message was present during prior tests of the SSF and RMA systems but was not noticed by test personnel.

The complete test was rerun successfully on December 20, 1985, without incident.

2.6 SYSTEM INTERFACE TESTS

2.6.1 Overview

The initial Government Furnished Equipment (GFE) and Host Interface testing occurs via the System Interface test. This testing occurred in three distinct phases; (1) Signal Level Testing, (2) 9020 CCC/GFE interface via the transition switch testing, and (3) Host/GFE interface testing. Signal Level testing consisted of utilizing instrumentation for measuring the signal level voltage of each individual line within all interfacing Host Channels. 9020 CCC/GFE interface testing consist of generating comparison data prior to recabling and interface verification by comparison following recabling. Host/GFE interface testing was accomplished using a series of Maintenance Diagnostics Monitor (MDM), Perhipheral Adapter Module (PAM) and Display Channel diagnostic routines. Comparison data generated in the 9020 was used to verify proper Host/GFE interface.

System Interface tests began on the SSF System on September 18, 1985, and were completed on October 2, 1985. The RMA system tests began November 5, 1985, and were completed on November 11, 1985. CS/SD System testing began December 17, 1985, and was completed on January 7, 1986. All tests were completed satisfactorily.

2.6.2 Test Description

Proper interface of the HCS equipment to the government furnished equipment (GFE) was demonstrated by meeting the performance requirements stated below. The HCS equipment tested included the HOST transition switch and interfaces as follows:

- 9020A to GFE through transition switch
- 9020D to GFE through transition switch
- HOST to PAMs
- HOST to CDC
- HOST to DCC
- Electronic Compatibility
 - Display Data Channel Interface
 - PAM Data Channel Interface
 - Configuration Control Register Interface
 - Configuration Control Register/PAM Data Interface

The test consisted of the following steps:

- a. An initial demonstration of the Electronic Compatibility between the transition switch and the GFE prior to actual connection of the switch to any government equipment.
- b. The 9020/PAM Maintenance test DCC51 run error free through the switch.
- c. The 9020/CDC Maintenance test D71C1 and D71C2 run error free through the switch.
- d. The 9020/DCC Maintenance test D71D1 run error free through the switch.
- e. The hosted PAM Maintenance test DCC51 run error free.
- f. The hosted SCOPE D70C3 Maintenance test run error free.
- g. The hosted CDC Maintenance tests D71C1 and D71C2 run error free.
- h. The hosted DCC Maintenance - Functional test D71D1 run error free.

2.6.3 Success Criteria/Analysis Method

The expected success criteria for the electronic compatibility segment of the interface test was the observation of the active signal level between 2.25 and 6.0 volts and the inactive level between 0 and 0.15 volts on the Configuration Control Register Signal Translators and the Data Channel Interfaces. A contractor furnished Interface Path Analysis Tester (IPAT) and an oscilloscope were used to verify these levels. The expected success criteria for the communication segment of the interface test was the error free execution of 9020/GFE and HCS maintenance programs.

2.6.4 Test Conduct/Results

2.6.4.1 System Support Facility (SSF) System

The electronic compatibility segment of the System Interface test was conducted on September 24, 1985. The IPAT and an oscilloscope verified that all signal levels were within the specifications for the display channels.

The PAM Data Channel Interface test was conducted successfully. The IPAT and oscilloscope were interfaced to the BUS lines on channel 0 of the A2 processor controller. All levels were measured and found to be within the specifications tolerances.

The Configuration Control Register test was conducted successfully. All IPAT settings of the test procedure were measured and matched expected results.

The Configuration Control Register/PAM Data Interface test was conducted successfully. The active and inactive levels of the SCON data bits, the select pulses, and the simulated PAM element checks were all within the specifications.

During the Compatibility test conduct, four deviations to the approved test procedures were performed. All deviations were due to incorrect test steps or test configurations and had no impact on testing. There was a delay in the initiation of the testing because the test conductor interfaced the wrong processor controller channel at the 3814 switch. The FAA recommended that all cable markings in the system be improved. The communications segment of the System Interface test was verified by executing diagnostic programs on the HCS under the Maintenance Diagnostic Monitor (MDM) in a Virtual Machine (VM) environment. The diagnostic programs were converted GFE programs to execute on the HCS during the DCP of the HOST Contract. The programs were not deliverable items at the system test time and as such had many outstanding problem reports. These known problems had no effect on the verification of the HCS's capability to communicate with the GFE display systems and PAMs.

The communications segment of the System Interface test was conducted from September 18 to October 2, 1985, in five test sessions. During the test sessions, eight known problems written against the diagnostic programs were observed, seven deviations were made due to incorrect procedures, three problems related to the GFE were observed and one new problem report was written against D71C1-routine 22.

Summary of Test Conduct

Key: HCSA1 = HOST A1 Processor

HCSA2 = HOST A2 Processor

September 18, 1985

DA051 - 9020D/Channel to Channel Adapter was completed.

DD8A0 - 9020D/Configuration Control Register was completed.

DCC51 - 9020D/PAM Adapter was completed.

D71D1 - 9020D/DCCMNT Routines 1,2,3,4,5,6, and 15 were completed.

D70C3 - 9020D/SCOPE2 - Not run at request of FAA.

D71D1 - HCSA2/DDMNT Routines 1,2,3,4,5,6, and 15 were completed.

DCC51 - HCSA2/PAM Adapter was completed.

September 20, 1985

- D71C1 - HCSA1/CDCMNT Routines 3,14,15,21,22,23,18, and 17 were completed.
- D71C2 - HCSA1/IOC Routines 1,2,3, and 4 were completed.
- DCC51 - HCSA1/PAM Adapter PAMs 1,2, and 3 were completed.
- D74C1 - HCSA2/QARS was completed.
- D70C3 - HCSA2/SCOPE2 was completed.
- D71C1 - HCSA2/CDCMNT Routines 3,14,16,17,18,21,22, and 23 were completed.

September 23, 1985

- D71D1 - HCSA1/DCCMNT Routines 2,3,6,7,14, and 15 were completed.
- D70C3 - HCSA1/SCOPE was completed.
- D74C1 - HCSA1/QARS was completed.

September 24, 1985

- D71C1 - HCSA2/CDCMNT Routines 17,18,21,22, and 23 were completed.
- D71C2 - HCSA2/IOC Routines 1,2,3, and 4 were completed.
- D70C3 - HCSA2/SCOPE2 was completed.

October 2, 1985

- OLTS - Channel to Channel Adapter was completed.

2.6.4.2 Reliability, Maintainability, Availability (RMA) System

The electronic compatibility segment of the System test was conducted on November 11, 1985. To expedite testing, each individual test was run on one processor, then the other processor, then proceeding to the next test.

During the Display Channel Interface test (channel 5 of Processor Controller A5) the "Operational Out" signal failed. The redundant 3814 matrix switch was configured and the test completed with no problems. All other tests ran successfully.

To conclude the test, the Display Channel Interface test was rerun after a defective printed circuit card had been replaced in the failed 3814 matrix switch. The test was completed successfully.

The communications segment of the Systems Interface test was conducted November 5 through 7, 1985. During the test runs ten known diagnostic program problems were observed, seven deviations were made due to incorrect procedures, one GFE problem was observed, and one problem report was written against D74C1 (QARS) diagnostic program.

Summary of Test Conduct

November 5, 1985

- D70C3 - 9020/SCOPE2 was completed.
- D71D1 - 9020/DCCMNT Routines 14 and 15 were completed.
- DD8A0 - HCSA5/Configuration Control Register was completed.
- DCC51 - HCSA5/PAM was completed.
- D71D1 - HCSA5/DCCMNT routines 1,2,3,6,7,14, and 15 were completed.
- D70C3 - HCSA6/SCOPE2 was completed.
- D71D1 - HCSA6/DCCMNT Routines 1,2,3,6,7,14, and 15 were completed.
- D74C1 - HCSA6/QARS was completed.

November 6, 1985

- DD8A0 - HCSA5/Configuration Control Register was completed.
- DCC51 - HCSA5/PAM was completed.
- D71C1 - HCSA5/CDCMNT Routines 3,14,16,17,21,22, and 23 were completed.
- D71C2 - HCSA5/IOC Routines 1,2,3, and 4 were completed.
- D70C3 - HCSA6/SCOPE2 was completed.
- D71C1 - HCSA6/CDCMNT Routines 3,14,16,17,21, and 23 were completed.
- D71C2 - HCSA6/IOC Routines 1,2,3, and 4 were completed.
- D74C1 - HCSA6/QARS were completed.

November 7, 1985

- OLTS - HCSA5, HCSA6 and 9020 E1/E2 Channel to Channel Adapter Test was completed.

2.6.4.3 Central Support/Software Development (CS/SD) System

The electronic compatibility segment of the System Interface test was conducted on December 17, 1985. All steps of the approved test procedure were performed. All output matched the expected results.

The communication segment of the System Interface test was conducted on January 6 and 7, 1986. CDCMNT, DCCMNT, and OLTS diagnostic programs were not run because the display channels are not connected to the CS/SD system. During the test runs, known diagnostic program problems identical to the problems that were reported during the SSF and RMA system test runs were observed. A SCON problem was experienced on January 6, 1986, while attempting to run D70C3 on the HCSA4 processor. The problem was isolated to an improper cabling for the A4 processor in the SCON unit. After correcting the cabling, the test was rerun successfully on January 7, 1986.

Summary of Test Conduct

January 6, 1986

- D74C1 - 9020A/QARS was completed.
- D70C3 - 9020A/SCOPE2 PAMs 2 and 3 devices were completed.
- DD8A0 - HCSA3/Configuration Control Register was completed.
- DCC51 - HCSA3/PAM was completed.
- D70C3 - HCSA3/SCOPE2 was completed.
- D74C1 - HCSA3/QARS was completed.
- D74C1 - HCSA4/QARS was completed.

January 7, 1986

- D70C3 - 9020D/SCOPE2 PAMs 2 and 3 devices were completed.
- D74C1 - 9020D/QARS was completed.
- D70C3 - HCSA3/SCOPE2 PAMs 2 and 3 devices were completed.
- D74C1 - HCSA3/QARS was completed.
- DD8A0 - HCSA4/Configuration Control Register was completed.
- DCC51 - HCSA4/PAM was completed.
- D70C3 - HCSA4/SCOPE2 was completed.
- D74C1 - HCSA4/QARS was completed.

Note: SCOPE2 tests where devices for PAMs 2 and 3 only were tested, PAM 1 was not tested due to a GFE problem.

2.7 HOST/9020 TRANSITION TEST

2.7.1 Overview

The principal requirement verified by this test was the ability of the ARTCC NAS system to be switched between the Host and the 9020, and vice versa, within 30 seconds and the subsequent success of either being operational via the switches. This test was exercised from control terminals remotely located from the 3814 switches in the vicinity of the SMCC.

The initial Host/9020 Transition test was made on the SSF System on September 24, 1985. However, the transition time exceeded the Engineering Requirement of 30 seconds which required a logic change in the 3814 transition switch. A successful retest was later held on the RMA system.

2.7.2 Test Description

Tests were performed to verify that the PAM and Display Channel equipment can be manually switched from the HCS to the 9020 system in less than 30 seconds, and that the PAM and Display Channel equipment can be manually switched from the 9020 system to the HCS in less than 30 seconds.

2.7.3 Success Criteria/Analysis Method

The HCS/9020 Transition test was considered successful when it was verified that switching the PAMs, SCON, and Display Channel interfaces from the HCS to the 9020 CCC and from the 9020 CCC to the HCS completes within the required time limit. Each switchover is allowed up to 30 seconds to complete. The CS/SD system has no transition switch and, as such, was not tested.

2.7.4 Test Conduct/Results

2.7.4.1 System Support Facility (SSF) System

The SSF System Transition Switch test was conducted on September 24, 1985. The test consisted of bringing up the Baseline 500 program on the appropriate system (9020 or HOST) and selecting the configuration at the transition switch KVDTs. Switching time was measured with a stop watch from the time the "ENTER" button was depressed, until the display screen responded with "OPERATION ENDED.EX". The test was executed using the individual 3814 KVDTs for PAMs, SCON, and Display Channel interfaces. Two test runs were conducted: HOST to 9020 transition and 9020 to HOST transition. After each run the Baseline 500 was executed to verify that the transition had been achieved.

HOST to 9020

	<u>Stop Watch No. 1</u>	<u>Stop Watch No. 2</u>
Displays	31.57 Seconds	31.58 Seconds
PAMs	36.77 Seconds	36.82 Seconds
SCON	33.72 Seconds	33.57 Seconds

9020 to HOST

	<u>Stop Watch No. 1</u>	<u>Stop Watch No. 2</u>
Displays	32.64 Seconds	32.14 Seconds
PAMs	33.61 Seconds	33.62 Seconds
SCON	27.72 Seconds	27.81 Seconds

The systems switched successfully but, the transition times were not within the Engineering Requirements specification of 30 seconds. It was determined at post-test that reconfiguration of the 4x4 switch matrices was necessary to meet the 30 second requirement. As a result, the test was deferred to the RMA facility testing, the next scheduled installation event. A single set of transition switches was furnished to the Technical Center for test purposes.

2.7.4.2 Reliability Maintainability Availability (RMA) System

This test varied from the test performed on the SSF system in that one 4x12 matrix was used in the transition switch configuration instead of the three 4x4 matrices used on the SSF. This change was not a physical change but a logical change. The use of one matrix reduced the transition times dramatically.

HOST to 9020

The execute command was entered sequentially on the three KVDTs with one stop watch per console recording the time.

<u>Displays</u>	<u>PAMs</u>	<u>SCON</u>
11.89 Seconds	12.94 Seconds	12.68 Seconds

9020 to HOST

All three consoles were clocked separately by three observers.

<u>Displays</u>	<u>PAMs</u>	<u>SCON</u>
8.20 Seconds	8.24 Seconds	12.68 Seconds

8.14 Seconds	8.21 Seconds	12.46 Seconds
Operator Error	8.64 Seconds	12.56 Seconds

One operator entered execute consecutively on the three consoles. Time was clocked by three observers from execute on the first console to operation complete on the third console.

<u>Stop Watch No. 1</u>	<u>Stop Watch No. 2</u>	<u>Stop Watch No. 3</u>
14.45	14.41	14.41

Transition Switch testing was thereby concluded on the RMA system with all engineering requirements verified. There was no requirement to re-hook up the switches to the CS/SD system since it would not use the full complement of GFE equipment, i.e. the display channels.

3 NONOPERATIONAL SOFTWARE TESTS

The HOST Nonoperational Software Test series consisted of 11 test areas:

- VMCP
- MDM
- MVS
- System Build Support Software
- System Utility Software
- HOST Computer System Diagnostics
- Maintenance Software
- Support Software
- Modified Commercially Available Software
- SCMS
- Security

Many of the test areas addressed numerous software programs that were run over the course of many months beginning in December 1985, and continuing through November 1986. Tests were repeated as deemed necessary by the government until satisfactory performance was achieved. Table 2 shows Test Conduct dates for Nonoperational Software Tests.

TABLE 2. NONOPERATIONAL SOFTWARE TESTS

TEST NAME	FORMAL RUNS (1985-1986)	RETESTS/ DEFERRED TESTS (1986)	REGRESSION/ VERIFICATION TESTS (1986)
VIRTUAL MACHINE CONTROL PROGRAM (VMCP)	3 MAR	1 JUL	N/A
MAINTENANCE DIAGNOSTIC MONITOR (MDM)	6 MAR	AS PART OF MAINTENANCE SOFTWARE TESTING	5 NOV
MULTIPLE VIRTUAL SYSTEM (MVS)	19 DEC	N/A	N/A
SYSTEM BUILD	27 MAR 8 APR	15 JUL	10 SEP 5 NOV
SYSTEM UTILITIES	11,12 DEC	9 JAN	20, 21 FEB
HCS DIAGNOSTICS	13 DEC 16 DEC	14 MAR	N/A
MAINTENANCE SOFTWARE	14-28 MAR	16-18 JUL 26 SEP - 14 NOV	N/A
SUPPORT SOFTWARE	1,2 APR 21 JUL	8 SEP 17 OCT 11 NOV	N/A
MODIFIED COMMERCIAL SOFTWARE	28 FEB	20 JUN	N/A
SYSTEM CONTROL AND MAINTENANCE SUPPORT	20 MAR	28 MAY 26 JUN 11 JUL	N/A
SECURITY	24 FEB	N/A	N/A

In addition to the verification of Engineering Requirements allocated to these areas, one Engineering Change Request (ECR), No. 13, was demonstrated which provided change bars to ACES listings reported under the Build Test.

The sections which follow provide details on each of the nonoperational software test areas.

3.1 VIRTUAL MACHINE CONTROL PROGRAM (VMCP) TESTS

3.1.1 Overview

A variety of support system monitors each with its own set of applications programs were required to be run concurrently under a common Support System Monitor simultaneously with a NAS standby ready to assume operations should the Primary System fail. IBM chose their Virtual Machine/System Product (VM/SP) to perform this function. This test verified that all rehosted NAS monitors and newly procured monitors would operate in the Support Processor concurrently including the NAS Operational Monitor in the test mode.

The VMCP test was held on March 3, 1986, with a rerun on July, 1 1986. The final test satisfactorily demonstrated that VMCP executed the NAS operational monitor, the NAS operational system in a test mode, and various other NAS monitors on the support processor while the operational NAS program was executing in the primary processor.

3.1.2 Test Description

The VMCP was tested for correct operation by executing multiple monitors correctly and concurrently on the support processor, with the hosted NAS operational software running on the primary processor.

The following was run concurrently on the support processor under VMCP:

- a. NAS Operational system (CDC Version) in Test Mode-Baseline Test 500.
- b. NAS Operational system (DCC Version) in Test Mode-Baseline Test 500.
- c. OS/MVS - COMPOOL Edit
- d. NAS Operational Monitor
- e. Hosted MDM - PAM Diagnostic Test (DCC51)
- f. Conversational Monitor System (CMS)
- g. Remote Spooling Communication System (RSCS)

h. System Monitor Analysis Real Time (SMART)

i. OLTS

3.1.3 Success Criteria/Analysis Method

The results of both Baseline 500 tests, Data Analysis and Reduction Tool (DART), COMPOOL Edit, and PAM Diagnostic test were compared to government furnished results for the test of these programs run on the 9020 system. Any non-comparisons between HCS data and 9020 computer data and other discrepancies were fully explained and documented. The specific explanation and proof provided was approved by the government prior to having the test considered satisfactory.

3.1.4 Test Conduct/Results

The Formal VMCP test was conducted on March 3, 1986, using government approved red-lined procedures. A planned deviation to the procedures was approved at the pretest briefing, deferring the demonstration of the DART program requirement since DART was not yet ready. A second COMPOOL Edit was run in place of DART. VMCP version 4.0 was used. Thirteen anomalies occurred during the test. Three were due to configuration errors, nine were due to editorial problems with procedures and one due to the failure of the PAM diagnostic program, DCC51, executing in one of the Virtual Machines under MDM. These anomalies were not considered significant and had little effect on the test results.

Only three of the seven reports expected to be generated by the SMART program were produced. The remaining four reports were accidentally lost prior to printing. As a result, data analysis could not be fully completed.

Although a preliminary analysis indicated that the VMCP test was successful in demonstrating the operation of multiple virtual machines, a retest was needed to demonstrate the DART processing requirement and to obtain the missing SMART reports.

The complete VMCP test was rerun on July 1, 1986, using government approved red-lined test procedures. NAS version HR10.21CB was executed on the primary processor, and version 4.0 of VMCP was used on the support processor.

All steps of the test procedure were executed successfully. All SMART reports were printed when requested and the DART job ran successfully. An improved version of the PAM diagnostic, DCC51, executed successfully.

Post-test analysis revealed that the DART processing was successful and produced the expected outputs.

The SMART reports contained CPU utilization percentages as expected. No anomalies were encountered and the test was considered a successful

demonstration of VMCP's ability to manage the resources of the HOST Computer System without interfering with the on-line NAS operations.

3.2 SUPPORT/MAINTENANCE MONITOR TESTS

3.2.1 Overview

In-depth testing of the Multiprocessing Diagnostic Monitor (MDM) and the Multiple Virtual Storage (MVS) operating system were required due to the changed environment in which they were required to operate under VMCP. Each were originally built to operate independently and required extensive modification to operate in the Host Support System environment. Many of the NAS support programs that had previously operated under a variety of monitors were now required to run under MVS. MDM was required to operate in either of two modes; multiprogramming or sequential.

The MDM tests were held on March 6, 1986. Portions of the MDM sequential test requirement pertaining to the CDC interface were initially unsuccessful. An FAA required retest of MDM in the sequential mode was successfully included during a portion of the Maintenance Software tests that were held between March 24 and November 11, 1986. A successful final regression test of MDM in the concurrent mode was held on November 5, 1986. These tests verified the capability of MDM to correctly perform selected hardware diagnostic programs. On December 19, 1985, MVS was successfully tested with no significant problems occurring. This test verified the ability of MVS to execute multiple jobs concurrently.

3.2.2 Maintenance Diagnostic Monitor

3.2.2.1 Test Description

The MDM was tested in the multiprogramming and sequential modes. The tests performed included the following:

a. Multiprogramming Mode

1. Load the MDM Monitor
2. Enter the applicable messages specified in section 2.1 of the Maintenance Monitor Manual, FAA-2000.
3. Select a representative subset (at least 10) of the Test and Maintenance Programs from section 20.4.1 MDM Maintenance Software section of the Engineering Requirement Appendix B, NAS Software Description, and run them concurrently.

b. Sequential Mode

1. Load the MDM Monitor
2. Enter all applicable messages specified in section 2.1 of the Maintenance Monitor Manual, FAA-2000.
3. Select a representative subset (at least 10) of the Test and Maintenance Programs from section 20.4.1 of Engineering Requirement Appendix B, NAS Software Description, and run them sequentially.

3.2.2.2 Success Criteria/Analysis Method

Tests were considered complete and satisfactory when data analysis verified that each function performed successfully. Moreover, the test was run again as deemed necessary by the government to demonstrate proper functional operation.

3.2.2.3 Test Conduct/Results

The pretest briefing for the MDM test was held on March 5, 1986. No major issues were raised. Red-lines to the final test plan and test procedure were approved.

The test was conducted on March 6, 1986. Ten maintenance programs were run sequentially and ten programs were run concurrently. All programs ran with no problems in concurrent mode.

Four anomalies were recorded when the programs were run sequentially. Three were due to operator errors and were insignificant. The fourth anomaly was related to the failure of MDM to properly run the CDCMNT Program D71C1. An HIPR No. 1106, was written against CDCMNT. The system was reset and the CDCMNT procedures repeated without incident.

Post-test analysis indicated that the CDCMNT program performed correctly however, MDM did not function correctly on the first sequential run. The problem report against CDCMNT was updated to reflect the MDM failure rather than the CDCMNT failure.

In view of these findings, the test was not considered a satisfactory demonstration of the MDM sequential requirement, in particular with respect to the CDC interface. Regression testing of MDM with D71C1, CDCMNT would be required if the solution to HIPR No. 1106, also documented as INFO problem No. 1568, required changes to the MDM program and its interface to the CDC system.

On May 19, 1986, INFO problem No.1568 was resolved by IBM. MDM contained several errors related to I/O interrupt handling and the CDC dual channel operation.

The retesting of MDM in the sequential mode with CDCMNT was accomplished by the performance of the Maintenance Software tests. Details are contained in section 3.6 of this report.

A Formal Regression test was performed on November 5, 1986, to verify that the changes to MDM did not affect the concurrent mode of operation. Five programs were selected and run concurrently. No anomalies were reported and the MDM test was considered successful and complete.

3.2.3 MVS

3.2.3.1 Test Description

MVS testing included the following:

- a. Select and run a representative subset (at least ten) of the functions described in section 20.3 NAS Support Software of Engineering Requirement Appendix B, NAS Software Description.
- b. Select and run a representative subset (at least five) of the programs described in section 20.4.2 OS Maintenance Support Software of Engineering Requirement Appendix B, NAS Software Description.

3.2.3.2 Success Criteria/Analysis Method

The particular result expected was for the ten NAS initiators to be activated concurrently and execute the ten NAS support programs. Following the successful completion of the support programs, five of the MVS initiators were to be activated concurrently and execute the five radar data and analysis programs.

3.2.3.3 Test Conduct/Results

The formal test of MVS was conducted on December 19, 1985. The pretest briefing was uneventful and no changes or deviations to government approved test plans or test procedures were anticipated.

During the test conduct, minor corrections were required to the procedures. These corrections were editorial and had no effect on the test results. Two anomalies occurred, one relating to printer paper feed and the other due to the inadvertent deleting of a source module to be assembled. The job was resubmitted and ran correctly.

Post-test data analysis uncovered one invalid MVS condition code of 7128 during the execution of one radar data analysis program, BCST. This problem was considered insignificant and a GFE related error. All anomalies were attributed to procedural deviations due to dry run oversights and problems with data management of test software and procedures.

All engineering requirements for MVS were met during the test. No anomalies or deviations were considered significant and the test was successful.

3.3 SYSTEM BUILD SUPPORT SOFTWARE TESTS

3.3.1 Overview

The system build process encompasses utility and report producing tools which prepare the data, perform the build, and finally produce the necessary reports to validate results and furnish accountability and control for changes. Modifications of all types; adds, deletes, and replacements were tested to ensure no loss of capability. In addition the data file security controls required of formal and final system build processes was demonstrated. The final steps within the procedure was to verify the system build could be initialized and perform operationally.

A series of System Build Support Software tests were held beginning March 26, 1986. The use of a non-rehosted patch tool (ZAP) resulted in test completion being delayed until April 8, 1986. An FAA required retest was held on July 15, 1986, with a final successful test held on September 10, 1986. An Engineering Change required a demonstration which was successfully held on November 5, 1986. This series of tests verified that the Host Computer System could successfully build an operational NAS system.

3.3.2 Test Description

The system Build process was tested using the appropriate tools and programs of the NAS to generate a complete and operational NAS. The system was built under the MVS operating system, in the VMCP environment, utilizing the support processor of the HOST Computer System. Each of the following system Build steps were performed to completion. The system Build was performed in both the create mode and the update mode.

- a. The COMPOOL edit function tested the following inputs:
 1. COMPOOL item(s) added, deleted, and updated in an existing table.
 2. New COMPOOL table(s) added.
 3. Old COMPOOL table(s) deleted.
 4. System parameters added, deleted, and modified.

- b. The library edit function tested the following inputs:
 - 1. A new library module added.
 - 2. Source changes added to an existing module.
 - 3. A library procedure descriptor table change added.

- c. The NAS operational source Build tested the following inputs:
 - 1. A new NAS module added.
 - 2. Source changes to an existing module.

- d. The ACES/Adaptation Build tested the following inputs:
 - 1. New and modified record dataset(s) added/deleted.
 - 2. Updates to Table Data Build (TDB) programs.
 - 3. Updates to the order of TDB execution.
 - 4. New adaptation data added/deleted.

- e. The NAS disk Build tested the following inputs:
 - 1. A new COMPOOL.
 - 2. New library and NAS modules object added.
 - 3. Old library and NAS modules object deleted.
 - 4. Source change(s) object to update existing modules.
 - 5. New ACES output tape.
 - 6. Different systems configuration, CDC, and DCC.
 - 7. Changes to storage allocations.

The tested software included; ACES, ACEUTE, CEST, OBJEDT, COMPOOL Analyzer, LIBRARY Analyzer, UNTE, DISKCNVT, NASLKED, NASXREF, and UNTESIZE. The software was tested both functionally and within a procedure which generated a software system that would load on the HCS. Procedural changes have been initiated into the HOST System Build identified as the Automated System Build (ASB) replacing the 9020 methods for configuration control of the NAS software. This procedure was demonstrated within the Build test by "DRAWDOWN" of module sources from a release file to a development file, modified,

and "PROMOTED" back into the release level file. The Build software was then run sequentially as required by ASB, including implementation of national patches, to create the final loadable system.

3.3.3 Success Criteria/Analysis Method

The software functional testing portion of the Build test was compared to identical 9020 runs. This was in accordance to criteria established by the FAA prior to the delivery of comparison GFE data which exercised a selected set of program functional capabilities. As required by the established FAA criteria, ACES consisted of seven runs, ACEUTE required seven runs, CEST two functional runs, one OBJEDT run, and six UNTE Build runs.

Further success criteria was specified within the Quality Assurance, section 4.0 of the contract Engineering Requirements. The success criteria specifies that updates be performed on the NAS module sources, COMPOOL, library sources, and adaptations source prior to Building a system to Initial Program Load (IPL).

The successful completion of the system Build process resulted in the generation of a NAS disk ready for IPL. The NAS operational program built in this section was used for the NAS Operational Software Test requirements described in this report.

3.3.4 Test Conduct/Results

At the pretest briefing held on March 24, 1986, problems that were uncovered during dry run tests were discussed. Red-lined test procedures were distributed and the formal test was rescheduled from March 25 to March 26 to allow satisfactory resolution of the above problems.

The test conduct for formal test commenced March 26 and was completed April 8, 1986. Conduct took considerably longer than anticipated due principally to the bonding procedure. Two days were completely lost due to problems occurring while restoring the system to the pre-dry run status. Successful bonding occurred March 27 to allow testing to commence.

Overall, test conduct went relatively well despite additional red lines required throughout the procedure. The use of ZAP, a patch tool which had not been rehosted, was red-lined into the procedure. This tool was disallowed causing a portion of the procedure to be rerun. A quick fix by returning to OBJEDT with the patches failed.

Following extensive research by IBM, the system was restored and bonded back to the beginning of March 31 to complete the test on April 8, 1986. Additional red lines were required due to the removal of ZAP. The test completed successfully with the system loading satisfactorily and executing for approximately 15 minutes.

A substantial number of deviations resulted from the System Build test. The deviations were adequately presented at the post-test briefing. Due to the excessive number of red lines, the procedure was republished as Revision 1 following the test. Thirty-seven deviations were presented at the post-test briefing. These were reviewed in detail at that time. Eight outstanding problems affected the testing. Two new INFO problems were written, one against the COMPOOL Analyzer and one against VMCP.

At the post-test briefing it was agreed that the test was incomplete and further testing was required. A retest was scheduled once all outstanding problems were resolved and in order to produce a system to be used in operational software testing. Five ACEUTE runs were deferred due to an outstanding problem report.

The retest occurred on July 15, 1986. The purpose of this test session was to complete the System Build requirements verification. Verification of solutions to problem reports generated during the initial test conduct were included as part of this test. These were, OBJECT EDIT retest, COMPOOL Analyzer retest, four against ACES, and retest of the drawdown/promotion process due to a problem against VM. Also, an ACES update run was made to demonstrate change bar usage (ECR No. 13), a design change capability, and a NAS DUMP/Restore to/from tape demonstration.

Test conduct was accomplished as planned in a single session on July 15, 1986. However, data analysis produced four additional problem reports preventing the completion of this test.

Another anomaly with the procedure occurred. A deferred ACEUTE run required comparing two COMPOOLS and identifying differences. However, identical COMPOOLS were used rendering the run useless.

A post-analysis meeting held with IBM on July 24, 1986, resulted in agreement that a problem verification session would be required to complete the Build test requirements. The verification test was run on September 10, 1986. The four outstanding problem resolutions were successfully demonstrated. The COMPOOL mismatch was successfully demonstrated when comparing two adaptation sets generated from different COMPOOL's. No problems occurred during this test and the System Build test was considered successfully complete.

As a demonstration of ECR No. 13, IBM successfully demonstrated the ACES change bars on November 5, 1986, by first running an ACES CREATE and then running an ACES UPDATE that used a control file containing changes to be made to the output.

3.4 SYSTEM UTILITY SOFTWARE TESTS

3.4.1 Overview

This test furnished assurance that the re-Hosted utility programs such as; compilers, assemblers, editors, analysers, etc. essential to the system build and generation of support systems performed as required

on the Host Support System. This was an in-depth test of the utilities as opposed to the system build process which exercised the utility programs sequentially within a system in a positive manner.

Initial tests of System Utility Software were held December 11-12, 1985, Excessive execution times for two analyzer programs resulted in an FAA required retest which was held on January 9, 1986. The FAA required a rerun of all tests because VMCP was updated after the January 9 test. A successful final test was held February 21, 1986. These tests verified that the system utility software, comprised of various program compilers, assemblers, editors, and analyzers, functioned properly.

3.4.2 Test Description

Tests were performed to verify the functional capabilities of the hosted software listed in section 20.3.1 Utility Software of Engineering Requirement Appendix B, NAS Software Description. The testing was conducted in the HCS VMCP environment operated under OS/MVS in the support processor. Seven programs were tested.

3.4.3 Success Criteria/Analysis Method

Tests were considered complete and satisfactory when data analysis verified that each function performed successfully.

3.4.4 Test Conduct/Results

The Utility Software tests were conducted on December 11 and 12, 1985. All tests ran to successful conclusions; however, the running time for both the Library Analyzer and COMPOOL Analyzer were excessive (3 hours, 20 minutes and 1 hour, 20 minutes, respectively). The expected run times were approximately 15 to 30 minutes.

Both programs ran to completion. However, the test was not considered successful due to excessive run time and loss of test data.

Modified Library Analyzer and COMPOOL Analyzer programs were successfully rerun on January 9, 1986. Test run times were satisfactory and all test data were produced.

Following the January 9, 1986, tests VMCP was updated. It was deemed necessary by the FAA to rerun all of the programs with the new VMCP in order to insure no degradation.

A dry run was scheduled for February 20, 1986, with the formal test on February 21, 1986. During the dry run the following utilities were exercised:

CMPEDT
JOVIAL COMPILER
BALASM
LIBEDT
OSXREF

LIBRARY ANALYZER
COMPOOL ANALYZER

Since no anomalies were observed during any of the runs, the FAA decided to use the listings and data produced during the dry runs as formal data and only run the CMPEDT and the JOVIAL programs during the formal test. Both programs took longer to complete than expected. This was due to the excessive number of users (87) on the system at the time of the test.

On February 21, 1986, CMPEDT and JOVIAL programs were run successfully within the expected time ranges. Minor anomalies were found during the data analysis. They had no impact on the test results and the utility software test was considered successfully completed.

3.5 HOST COMPUTER SYSTEM DIAGNOSTIC TESTS

3.5.1 Overview

Diagnostic testing performed within this test related strictly to the test and maintenance of the procured hardware; the Host computer system, Direct Access storage system, switching system, and peripherals. In addition to testing the diagnostics capabilities to isolate problems, it was specified that this type of maintenance be performed without interference to the ATC operational system.

Host Computer Diagnostic testing was held on December 13 and 16, 1985. Additional testing was held on January 9, 1986 with a final successful test held on March 14, 1986. This series of hardware diagnostic tests verified the ability of the Host Computer System to correctly identify various HCS hardware failures.

3.5.2 Test Description

HOST Computer System Diagnostic tests were performed on the HOST Processor subsystem, the SCMS Processor subsystem, the Direct Access Storage subsystem, and the Peripheral subsystem. The diagnostic test included a series of Contractor induced hardware failures that were detected and isolated by the diagnostic software. All diagnostics operated under or concurrent with VMCP.

3.5.3 Success Criteria/Analysis Method

The tests were considered complete and satisfactory when all Contractor induced hardware failures were detected and isolated.

3.5.4 Test Conduct/Results

The initial HCS Diagnostics tests were conducted on December 13 and 16, 1985. These tests verified the capability of the HCS diagnostics to isolate faults to the field replaceable units. Twelve test cases were exercised with manually induced equipment failures inserted in seven types of HCS elements to be detected and isolated.

NAS was run on the primary processor. NST and the OLTSEP were used to detect the induced failures and isolate the defective units in the support system. Unit microdiagnostics were used to isolate the failures to the replaceable item.

Four of the 12 test cases proceeded without incident and were successful. The remaining eight test cases encountered various anomalies related to procedures, human errors, and the on-line NAS. These anomalies were not considered significant to this test and the diagnostics isolated failures as expected.

Additional testing was scheduled for January 9, 1986, but had to be rescheduled due to operational errors in the conduct of the test. The testing was conducted on March 14, 1986, in order to verify that diagnostics could be performed concurrent with other operations on the support system. For this test, NAS was again made operational in the primary processor.

The NAS standby system and the OLTS were run under VMCP on the support processor. Six of the original 12 test case microdiagnostics were run without manually induced errors. Minor anomalies occurred, but the testing was considered successful with no apparent interference with VMCP, NAS, NAS standby, or other VM users.

3.6 MAINTENANCE SOFTWARE TESTS

3.6.1 Overview

The Maintenance software referred to in this test relates to the re-Hosted diagnostics that had been used over the years to maintain associated systems; i.e., Peripheral Adapter Modules, and Display suites which the Host Computer services. Previously, the Monitor which controls the operations of these maintenance programs had been tested and verified. This test furnished the in-depth test of each individual program operating within that environment.

Due to the magnitude of the Maintenance Software, testing was conducted in three sessions; on March 24 - 28, July 16 - 18, and September 26 - November 11, 1986. All final tests successfully verified the proper execution of those maintenance software programs which are used for the analysis of operational system integrity, system performance, verification of the radar system, and the correct operation of the various peripheral devices which are used by the NAS operational program.

3.6.2 Test Description

The Maintenance Software listed in Engineering Requirement Appendix B, NAS Software Description, section 20.4 was tested to verify that it performs in accordance with its respective design specification document and users manual.

3.6.3 Success Criteria/Analysis Method

The tests were considered complete and satisfactory when data analysis verified that each function performed successfully in accordance with identical 9020 comparison data. Real-time observation of KVDT and GFE laboratory equipment was supplemented by the post-test analysis. The tests were repeated as deemed necessary by the government, until proper functional operation was demonstrated. Specific success criteria included:

- a. Correct system responses to all inputs as shown in the government approved test procedures.
- b. Correct on-line outputs and PVD presentation for the Display Channel test and maintenance programs in accordance with the user's manual and 9020 comparison data.
- c. Correct on-line outputs and hardcopy printouts for the Radar Data Analysis programs and the FDEP, FSP, MSP, and TTY test and maintenance program.
- d. Correct on-line outputs and SMMC display presentations for the SMMC test and maintenance programs.
- e. Correct on-line outputs and computer readout display (CRD) for NRKM and Display Channel test and maintenance programs.
- f. Correct rejection/error response to induced error inputs for verification of selected error condition detection by test and maintenance programs.
- g. Absence of error condition/indication during the normal execution and termination of Radar Data Analysis and test and maintenance programs.

3.6.4 Test Conduct/Results

The Maintenance Software test was conducted in three parts. Seventy-eight programs were tested in 251 sections (test cases).

Part I was conducted from March 24 to March 28, 1986, and encompassed 52 programs and 132 sections. Of these, 44 programs and 130 sections were considered successful with minor deviations or anomalies. The remaining eight programs and two sections failed requiring retesting. Induced errors were run successfully on 13 of the programs.

Part II which was conducted from July 16 to 18, 1986, and demonstrated 33 programs and 117 sections. Included were 25 programs and 115 sections which were deferred from Part I and the eight programs and two sections which failed during Part I. Thirty programs and 114 sections were considered successful with minor deviations or

anomalies. The remaining three programs and three sections failed and required retesting. Induced errors were run successfully on two of the programs.

Part III was conducted from September 26 to November 11, 1986, and demonstrated one deferred program with four sections, and the three programs and three sections that failed in Part II. All were successful.

Table 3, Maintenance Software Test Cases, shows the number of programs and test cases successfully demonstrated in Parts I, II, and III.

Upon the successful completion of Part III, all maintenance software requirements were satisfied for the HCS.

TABLE 3. MAINTENANCE SOFTWARE TEST CASES

	PASSED		FAILED		DEFERRED	
	Programs	Sections	Programs	Sections	Programs	Sections
Part I	44	130	8	2	26	119
Part II	30	114	3	3	1	4
Part III	4	7	0	0	0	0
Total	78	251				

3.7 SUPPORT SOFTWARE TESTS

3.7.1 Overview

Support software testing consisted of testing of the various re-Hosted programs that are required to perform Data Reduction and Analysis, Simulation, generate special reports, etc. The monitors required to control this set of programs had been previously tested; however, the purpose of this test was to furnish in-depth evaluation of the individual programs or subsets to produce desired results.

Tests of Support Software were held on April 1-2 and July 21, 1986. FAA required retests of programs that failed initial tests were held on September 8, October 17, and November 11, 1986. These tests successfully verified the correct functional capability of 25 various support and data reduction programs that are used in the development and maintenance of NAS software.

3.7.2 Test Description

Most of the NAS Support Software listed in Engineering Requirement Appendix B, NAS Software Description, sections 20.3.2, 20.3.3, and 20.3.4 were tested to verify that it performs in accordance with its respective design specification document. Some of the support software was satisfactorily demonstrated in the Build test and was not repeated here.

Programs tested during the Build test:

ACEUTE	CEST
DISKCNVT	UNTESIZE
NASLKED	OBJEDT
NASXREF	UNTE

The Response Time Tool (RTT) and List were not converted to run on the HCS and no testing was needed. OAMP was substituted for ADR and successfully tested. Figure 4 lists the programs tested.

3.7.3 Success Criteria/Analysis Method

The tests were considered complete and satisfactory when data analysis verified that each function performed successfully. Post-test analysis of HSP outputs supplemented real-time observation of KVDT messages. User's manuals and 9020 data were used for comparison to HCS outputs.

3.7.4 Test Conduct/Results

Twenty-five software programs were exercised using 69 test cases between April 1 and November 11, 1986. The initial formal tests were conducted in April and July 1986. Thirteen programs (8-0(29 test cases), were successfully demonstrated on the first attempt on April 1 and 2 using the March 18, 1986, software release. On July 21, 1986, six additional programs (23 test cases), were completed using the July

9, 1986, software release. This completed the initial formal test runs. Six programs remained to be completed, having failed the initial attempts.

Retesting began on September 8 using the August 29, 1986, software release. Two programs were successfully tested using three test cases. The remaining four programs were demonstrated on October 17 and November 11 using 14 test cases. Figure 4 shows the relationship among programs, test cases, and test dates.

Upon completion of the test on November 11, 1986, the overall results indicated that the support software had met requirements.

PROGRAMS	FORMAL TESTS		RETESTS		
	1, 2 APR	21 JUL	8 SEP	17 OCT	11 NOV
ADPP	7				
BLKTME	2				
DLOG	3				
GMPP	2				
MAPXFER	1				
METAPHRASE	1				
OAMP	1				
PUNCHGEO	3				
SIM	1				
SDBG	1				
SDR	1				
UBSF	3				
VPP	1				
DARCMAP		1			
DART		5		6	1
EDRA		1			
GENASYS	1	1			
NASCOR				1	
NTAP		3			
REDUC	1	5		1	
REMON			1		
STDG		3			
TARP		3		5	
ULR			2		
SSP		1			

FIGURE 4. TEST CASES USED WITH SUPPORT SOFTWARE

3.8 MODIFIED COMMERCIALLY AVAILABLE SOFTWARE TESTS

3.8.1 Overview

The unique environment in which the Commercial off-the-shelf software is required to operate in the Host Support system with the ATC operational system working standby, required considerable modification. This was principally to the VMCP software. The purpose of this test was to in-depth test those areas of the modified software where changes were identified. Previously, the NAS support system monitors acquired complete control of peripherals and were dedicated within a mainframe. In the Host Support environment, several monitors were run simultaneously, each responding to peripheral assignment and space allocation controlled by the high level VMCP system.

VMCP was tested on February 28, 1986. Because of a user error, the FAA required a retest which was held on June 20, 1986. These tests verified that all capabilities of VMCP performed satisfactorily.

3.8.2 Test Description

All modified commercially available software was tested to verify its performance in meeting all the unaffected published capabilities. Additionally, tests were performed to ensure the new capabilities resulting from the modifications performed satisfactorily. The modules within VMCP that were modified are: DMKTOD, DMKHUC, DMKFAA (new), DMKCLK, DMKEXT, DMKCCW, DMKQUM, DMKVCN.

3.8.3 Success Criteria/Analysis Method

Tests were deemed successful when analysis of test output verified the functions of the modules tested performed as defined in the user's manual.

3.8.4 Test Conduct/Results

The test was conducted on February 28, 1986, using VMCP as it is the only modified commercially available software delivered with the HCS. The test was run on the SSF with NAS version 10.11 on the primary processor and VM 4.0 High Performance Option 4.0, OS/MVS and MDM release level 10.4 on the support processor.

Red-lined procedures were distributed at the pretest briefing. Eight modules within VMCP were exercised using four test cases. Minor deviations from test procedures during the test had no impact on test results. A minor anomaly involving the removal of a wire from the incorrect processor had no impact on test results.

Post-test analysis of data produced during the four test cases indicated that the test was run successfully. One anomaly was identified during data analysis which proved to be a user error and was demonstrated successfully in a retest conducted on June 20, 1986. This completed the requirement for modified commercially available software.

3.9 SYSTEM CONTROL AND MAINTENANCE SUPPORT (SCMS) TESTS

3.9.1 Overview

Continuous awareness of the operational state of the Host system and its main components is essential to the FAA maintenance personnel. Testing of the capabilities to continuously monitor the health of the system, furnish indicators for troubled areas, and furnish a means for repair is the main purpose of this test. The means for problem isolation and repair was not limited to the facility but included communications for remote diagnostics as well. A major concern for this test was the environment in which maintenance would occur. This required the ATC operational system to run in the primary computer simultaneously with the Support system processing with no impact to ATC.

SCMS tests were successfully held on March 20, May 28, and June 26, 1986. These tests verified that SCMS provides the Host Computer System with the ability to diagnose and log all subsystem failures, report status of subsystem elements, report system resource utilization information, and communicate with the Central Support Facility.

3.9.2 Test Description

The SCMS was tested to demonstrate its ability to perform the following functions:

- a. Diagnosis of processor subsystem failures
- b. Provide processor subsystem elements status (Operational, Redundant, Test, or Inactive).
- c. Provide log out error data for all processor subsystem failures.
- d. Continuously monitor and provide system resource utilization information. These resources include, but are not limited to, the processors, I/O channels, main memory, peripherals, and program elements (NAS Applications, NAS Operational Monitor) per section 3.7 of the Engineering Requirements.
- e. Telecommunications with the Central Support Facility.

The configuration for the test included both the primary and support processor. The NAS operational software was executing in the primary processor in native mode with the Baseline 500 test scenario input from tape. On-line system resource utilization information was displayed on the console KVDT and printed on the console printer every minute. Resource Monitoring (REMON) data and High Resolution Timer (HRT) data were output to tape for post-test reduction and analysis.

The support processor ran a COMPOOL edit under MVS/OS, NAS test mode under VM, and executed the NAS operational monitor in standby mode throughout the test conduct. SMART and VM MAP were invoked for on-line and off-line resource utilization reports for the support processor.

The CS/SD HOST system was used as the Central Support Facility to verify the transfer of large volumes of data and the interaction with data bases.

En Route ARTCC to another En Route ARTCC communications were provided by a personal computer/modem to the SCMS of the CS/SD system.

HOST to standard Bell 212 interface was verified using a personal computer/modem to the 1200 BPS asynchronous dial-up facilities of the SSF system.

The IBM Support Center, Poughkeepsie, N.Y., was used as the Central Support Facility to verify the diagnostic functions of the SCMS.

3.9.3 Success Criteria/Analysis Method

The on-line resource monitoring capabilities of the primary processor were demonstrated by running NAS native and turning on the utilization reports for on-line analysis. REMON and HRT recordings were used as input to REMONR and SURP, respectively, for the off-line analysis reports. NAS native was monitored continuously at the system console, the high speed printer, and the console printer throughout the test conduct. All printer output was certified by IBM QA and used to verify that there were no interferences between NAS native and the SCMS test and that the NAS functions were not degraded during the resource monitoring.

SMART and VM MAP provided the resource monitoring for the support processor and were generated on-line and printed for off-line analysis. The COMPOOL Edit, NAS standby and NAS test mode tasks were continuously monitored at the support KVDTs. Hard copy output was analyzed at the conclusion of the run to verify proper execution of the support tasks.

Observation of the SCMS KVDT during the remote diagnostic test was the method used to verify the diagnosis of processor subsystem failures. The capability to provide log out error data for all processor subsystem failures was analyzed and verified by printing the AQEID file prior to and after an induced error. All files transferred during the communication tests were printed for off-line analysis.

Success Criteria:

- a. Correct system responses to all inputs as shown in the government approved test procedures.

- b. Correct on-line outputs, REMON and HRT tapes, and PVD presentations of the NAS operational software running in the primary processor relative to an identical 9020 Baseline 500 scenario run.
- c. REMON and HRT data analysis in accordance with identical 9020 Baseline 500 scenario.
- d. Resource monitoring recording and reporting relative to capabilities existing in the current 9020 and in accordance with NAS-MD-318.
- e. SMART and VMMAP data analysis in accordance with their appropriate user's manual.
- f. Support processor COMPOOL Edit task data analysis in accordance with NASP 9215-8, User's Manual: COMPOOL Edit program.
- g. Correct on-line outputs of the support processor NAS test mode task executed under VM.

3.9.4 Test Conduct/Results

The initial formal System Control and Maintenance Support Test, was conducted on the SSF system at the FAA Technical Center on March 20, 1986. All steps of the government approved test procedures were run; however, the test procedures did not contain tests to verify the ARTCC to ARTCC diagnostic support, the Bell 212A compatibility, and the off-line SMART reports for the support processor resource monitoring requirements.

The primary and support processors on-line resource utilization reports were continually observed. The state of processor subsystem elements was continuously monitored. A 6000 line ASCII character file was transferred from the CS/SD system to the SSF system via the 4800 BPS interface. An HP 1640B data analyzer was used to check the line protocol. An error was induced on the support processor's memory; communications were established between the FAA Technical Center SSF SCMS and the IBM Support Center in Poughkeepsie, N.Y., and the error was diagnosed correctly by the support center. The AQEID file was printed prior and after the error was induced to verify the log out error data requirement.

Two major anomalies were encountered. First, the REMON tapes generated during the test contained no data. The REMON tape reduction was required to verify primary processor resource utilization and, as such, was scheduled for retest. Second, a cold start was performed prior to initializing the system for the afternoon session. The cold start caused the VMMAP spool file to be lost. VMMAP recordings were restarted and reduced at the end of the run with no impact.

All of the on-line resource monitoring requirements for the primary and support processor were demonstrated successfully. The requirement to diagnose processor subsystem failures was verified. Log out error data retention was demonstrated. Requirements relating to remote access capabilities were demonstrated successfully.

Using a government approved revised test procedure, IBM successfully demonstrated the ARTCC to another ARTCC communications requirement on May 28, 1986. A communication link between a personal computer/modem to the SCMS subsystem of the CS/SD was established. Remote diagnostic support, transfer of files, and interaction with the data bases and diagnostic functions were tested. The CS/SD system was running the normal software development tasks and INFO management programs during the test conduct. No anomalies were observed. The ARTCC to ARTCC communications was considered successful.

Using a government approved revised test procedure, verification of the Bell 212A requirement was completed successfully on June 26, 1986, without anomalies. Communications were established between a personal computer connected to a standard Bell 212A modem and the CS/SD system. Files were successfully uploaded and downloaded from the personal computer to the HCS. The use of a valid USERID and password verified the security requirement. The CS/SD system was running the normal software development tasks and INFO management programs during the test conduct.

The reduced REMON data produced the program element and storage utilization reports for the primary processor off-line resource monitoring requirements. No anomalies were observed.

All Engineering Requirements allocated to the SCMS test were verified.

3.10 SECURITY TEST

3.10.1 Overview

Security testing was required of both the Primary and Support Systems. Primary system security consisted of ensuring there was no interference on the primary processor from the Support system in acquiring access to operational resources. Support system security consisted of logon protection, password protection, security maintenance, file protection, and direct access storage read/write protection.

Security tests were held on February 28, 1986. These tests verified the security capabilities of the Host Computer System.

3.10.2 Test Description

Security testing consisted of a series of demonstrations which verified the requirements of Engineering Requirement section 3.2.6.

This included password protection, communications protection, and direct access storage read/write protection for both users and between processors.

Security requirements verification was accomplished in a HOST NAS ARTCC environment with the NAS running in the primary processor and HOST standby in the support processor simultaneously with user virtual machines.

3.10.3 Success Criteria/Analysis Method

The success criteria was principally accomplished by observation at the terminal while exercising the procedural steps. The security directory for maintenance and usage of passwords in gaining access to the system, gaining access to PASSTHRU the communications operations module, disk read/write protection, and support processor access to a NAS disk (by label name) was accomplished in a single run. Special runs were made to demonstrate NAS disk reserve protection by device number and accessibility protection to the SCMS disk.

3.10.4 Test Conduct/Results

The pretest briefing held on February 24, 1986, concluded with a discussion of red lines to the formal test procedure.

The test was scheduled for February 24, 1986. Problems with the bonding procedure delayed the start of testing. Once started, testing proceeded with a considerable number of deviations from the final test procedure which were red-lined and submitted just prior to test. Testing progressed satisfactorily with the exception of keeping the standby side running. Several retries were required before eventual success. Two problem reports were written during the test, one related to the compare program used to verify the bonding process and one related to the standby NAS disk problems. Neither problem affected security and the test was considered successful with all seven Engineering Requirements allocated to this test verified.

4 OPERATIONAL SOFTWARE TESTS

The Operational Software Test series consisted of eight test areas with a minimum of one run on each of the display channels, CDC and DCC:

Monitor	Failure/Recovery
Functional	Live Radar
Capacity and Response Time	On-Line Certification
Reconfiguration	Acceptance

Table 4 shows Test Conduct dates for Operational Software Tests.

TABLE 4. OPERATIONAL SOFTWARE TESTS

TEST NAME	FORMAL RUNS (1986)	RETESTS (1986)	REGRESSION TESTS (1986)	PTR VERIFICATION (1986)
MONITOR	4 SEP	6, 21 OCT	4, 5, 20 NOV	N/A
FUNCTIONAL	26,27 AUG 16,17 OCT	N/A	18 DEC	N/A
CAPACITY AND RESPONSE TIME	12 SEP TO 10 OCT *	N/A	7 NOV 25 NOV	N/A
RECONFIGURATION	7 OCT 8 OCT	N/A	4 NOV 5 NOV 11 NOV	N/A
FAILURE RECOVERY	20, 21 OCT	N/A	4, 8, 13 NOV	18,20 NOV
LIVE RADAR	15, 17 SEP	N/A	N/A	N/A
ON-LINE CERTIFICATION	23, 30 SEP	10 OCT	N/A	N/A
FAA TECHNICAL CENTER SYSTEM ACCEPTANCE	27, 28 OCT	N/A	8, 10 NOV	N/A

* 24 TEST RUNS

Additional requirements were imposed on the Capacity and Response Time test area which resulted in 24 formal runs of this test with five different scenarios.

The FAA and FAA Support Contractors witnessed the formal test conduct of each of these areas upon completion of internal IBM dry runs.

Throughout the Operational Software Test series, various versions of NAS operational software were used. Each version had a unique identifier for that software baseline. The identifier used in the following example indicates that this is the 32nd iteration of Build 10 software to be used for the CDC system containing source patch level B.

EXAMPLE:

```
10.32  0  C  B
      |  |  |  |
      A  B  C  D
```

KEY:

- A = Build number iteration (10.31 or 10.32)
- B = Not applicable, used for RMA system
- C = C for CDC or D for DCC
- D = Level of source patches (A, B, C or D)

The software baselines used for this test series included four revisions to the NAS Operational Software version 10.31. The FAA established a change review team to determine the impact of these software changes (patches) on the results of previous testing and to determine the need to repeat previous tests when:

- a. The changes had an impact on prior test results.
- b. The impact of the changes on prior test results could not be determined without repeating the test.

In addition to the initial formal test runs and retests due to patches, a comprehensive Regression Test series was planned when all solutions to problems found during formal tests and retests were implemented in a new NAS Build, version 10.32. This Regression Test series consisted of a full re-execution of six of the original eight formal test areas with one or both display channels. Four new functions were tested during the Regression Test Series as follows:

<u>ECR</u>	<u>Function</u>	<u>Test</u>
012	Continuous KVDT alarm	Reconfiguration
019	Inactive status definition on KCNF	Reconfiguration

020	Mandatory switchover	Failure/Recovery
021	Startup/Startover for emergency patch	Failure/Recovery

Finally, fixes to problems remaining at the end of the Regression series were verified on version 10.32D. Table 5 shows the number of source patches for each of the version 10 Software releases.

The sections which follow provide details of Formal Testing, Retesting, Regression Testing, and Problem Verification Testing, as applicable to each test area.

TABLE 5. NUMBER OF SOURCE PATCHES BY BUILD

BUILD LEVEL	10.31				10.32			
	A	B	C	D	A	B	C	D
PATCHES	30	10	43	6	101	16	9	2

4.1 NAS OPERATIONAL MONITOR-TESTS

4.1.1 Overview

The most crucial portion of the Acceptance testing was the testing of the NAS Operational Monitor. This monitor controls the total environment, handles all inputs and outputs, performs health checks, and distributes data to the functional programs. The majority of new code developed for the rehosting effort was for the monitor. The new equipment and stringent requirements for redundancy of all NAS equipments including the central processor itself, was the primary cause of this new code. Time constraints for startovers and switchovers were not to exceed 10 seconds. Also, the system was being re-Hosted from a multi-processing environment to a single processor. The HCS Monitor simulation scenario was a complete re-write of the 9020 scenario since only a minimal amount of comparison data was generated by the monitor test. Although the scenario for this test was entirely new, which would not allow validation by comparison, knowledgeable FAA personnel generated it to ensure an in-depth test.

The NAS Operational Monitor test was held on September 4, 1986. Various minor problems were documented but no major problems occurred. The FAA required a retest, held on October 6 and 21, 1986, because of source changes to the monitor. Regression tests to demonstrate solutions to problems and to test added functions, were held on November 4, 5, and 20, 1986. These tests verified that the NAS Operational Monitor gave correct system responses to all inputs used, successful startovers and switchovers within 10 seconds, correct online and display outputs of the NAS operational software, and that all new and changed monitor functions performed correctly.

4.1.2 Test Description

The M-100 Baseline Test (which was modified by the Contractor to include new and/or changed functions required for the HCS) was used to verify that the HCS processes the NAS Operational Monitor logic functions as specified in Appendix F of the Engineering Requirement. This test was performed while the NAS operational software was executing in the primary processor in the native mode and a hot NAS standby was residing in the support processor. Two tests were conducted: one test with the HCS connected to the CDC and the other test with the HCS connected to the DCC.

4.1.3 Success Criteria/Analysis Method

The on-line test analysis conducted during each test run consisted of a visual inspection of PVDs, the console and line printers, and the status KVDTs. The on-line analysis verified that the HCS responded correctly to the scenario input and that the startover and switchover operations were completed within the required time specification. After each test run, an in-depth analysis of the data collected was performed by the FAA test team. The data included test witness logs, on-line hard copy output, and recorded data reduction.

Success criteria:

- a. Correct system responses to all inputs as shown in the government approved test procedures.
- b. Resumption of the NAS En Route ATC Service, as specified in the Engineering Requirements, for all startovers and switchovers within the 10-second time limit.
- c. Correct on-line outputs and PVD presentations of the NAS operational software running in the primary processor relative to an identical 9020 scenario run.
- d. Printer output and recorded data verifies that the new/changed monitor functions perform correctly.

4.1.4 Test Conduct/Results

The NAS Operational Software Monitor tests were conducted on the SSF system at the FAA Technical Center on the following dates:

<u>Test</u>	<u>Version</u>	<u>Build</u>	<u>Date (1986)</u>
Formal	DCC	10.31DB	Sep 4
Formal	CDC	10.31CB	Sep 4
Retest 1	CDC	10.31CC	Oct 6
Retest 2	CDC	10.31CD	Oct 21
Regression 1	CDC	10.32CB	Nov 4
Regression 2	DCC	10.32DB	Nov 5
Regression 3	CDC	10.32CD	Nov 20

The formal test runs were the initial tests using the government approved test procedures to verify the performance of the Operational Software Monitor capabilities. Retests were necessary when source changes were applied to the Monitor during Builds 10.31CC, 10.31DC, 10.31CD, and 10.31DD. The regression test runs using the same government approved test procedures demonstrated solutions to problems and verified that the performance of the Monitor capabilities was not degraded by the solutions.

Minor updates were applied to the Monitor test procedure and provided to the government 1 week prior to the formal test conduct.

4.1.4.1 Formal Tests/Retests

4.1.4.1.1 Summary of DCC Formal Test Conduct

After a successful startup of the NAS operational software version 10.31DB, the Monitor scenario was used for the formal demonstration. All Monitor messages were checked for proper responses. Reconfigurations, switchovers and startovers were observed and system outage time was measured at the PVDs. Four switchovers occurred although the scenario only input three. INFO problem report No. 6292 was written. Post-test investigation attributed the unsolicited switchover to an element check report received on PAM1, while PAM2 and PAM3 were in test status. The problem report was closed, the system had responded to the GFE problem correctly.

Air Traffic Laboratory Observations

Switchovers

<u>SIM Time Occurred</u>	<u>Recovery Time (sec)</u>
23:30:06	5
23:31:04	4
00:16:00	8 (unsolicited)
00:41:05	7

Startovers

00:36:01	1
01:17:30	0

Other

00:16:54	20 - time not updated on 6 of 12 PVD's. GFE problem
----------	--

Three minor deviations to the government approved test procedures were necessary with two related to anomalies observed and one to human error. Six anomalies were encountered with three attributed to GFE, one new problem (INFO No. 6294), one known problem (INFO No. 5995), and one problem attributed to human error.

Post-test analysis yielded 21 distinct anomalies. Thirteen of these were satisfactorily explained by IBM, three were found to be GFE problems, four were software problems that resulted in INFO problem reports, and one was related to Design Issue 53. The four problems were allocated to INFO problem numbers 6334, 6338, 6339, and 6364. All problems were type II or III.

4.1.4.1.2 Summary of CDC Formal Test Conduct

Immediately after the DCC formal test conduct, the Monitor test was repeated using the CDC display system and version 10.31CB of the operational software.

Air Traffic Laboratory Observations

Switchovers

<u>SIM Time</u> <u>Occurred</u>	<u>Recovery</u> <u>Time (sec)</u>
23:30:06	7
23:31:04	7
00:41:05	7

Startovers

00:36:01	6
01:17:30	6

Other

23:32:11	Sector 17 map blinked
23:54:21	Sector 17 display blinked
00:01:00	FDB CT34 two digts overlayed
00:18:00	FDB CT34 overlayed by another FDB

Blinking displays should be considered normal because the scenario contained many reconfigurations. INFO problem report No. 6296 was written against the overlay problem. Post-test analysis revealed that the overlayed full data blocks (FDBs) were part of the scenario. The INFO problem report was closed.

One deviation from the government approved test procedure was performed when the planned shutdown did not complete at SIM time 01:45. Tapes were closed and the system was shut down manually. INFO problem No. 6295 was generated. Post-test analysis revealed that this was a GFE problem. The problem report was closed.

Post-test analysis yielded eight distinct anomalies. Three of these were satisfactorily explained by IBM, four were found to be GFE problems, and one was a software problem. INFO problem No. 6294 was opened in reference to this problem.

4.1.4.1.3 Summary of CDC Retest No. 1

Due to source changes to the Monitor software for Builds 10.31CC and 10.31DC, the government deemed it necessary to rerun the Monitor test on the CDC display system. No deviations were performed. No anomalies were observed. The retest was considered successful.

4.1.4.1.4 Summary of CDC Retest No. 2

Due to source changes to the Monitor software for Builds 10.31CD and 10.31DD, the government deemed it necessary to rerun the Monitor test on the CDC display system. No deviations were performed. No anomalies were observed. The retest was considered successful.

4.1.4.2 Regression Tests/Verification Tests

Monitor regression tests were conducted November 5, 1986, using Builds 10.32CB and 10.32DB. Both CDC and DCC tests were run. Nine outstanding INFO problem reports were verified and closed. An additional regression test was conducted on November 20, 1986, using Build 10.32CD, the Seattle ARTCC Build version.

Two new functions were successfully demonstrated during the Monitor regression testing.

- a. KVDT Continuous Alarm
- b. Inactive Status Indicator

The Monitor regression tests demonstrated the ability of the rehosted Monitor software functions to operate correctly on the HOST Computer System as specified in the HOST Engineering Requirements. All messages and functions were verified using NAS-MD-317, and NASP-5201.

4.1.4.2.1 Summary of CDC Regression Test No. 1

The first attempt at executing this test failed. The initial scenario switchover required 15 seconds to recover and the next switchover never occurred. Prior to the test, a system programmer had forgotten to return the VM storage definition to V=R. The FAA test team allowed the test to begin again, after it was demonstrated satisfactorily that the problem was caused by the VM definition.

Air Traffic Laboratory Observations

Switchovers

<u>SIM Time</u> <u>Occurred</u>	<u>Recovery</u> <u>Time (sec)</u>
23:30:06	7
23:31:04	7
00:41:05	7

Startovers

00:36:01	1
01:17:30	1

Post-test analysis revealed that two anomalies had occurred during the test run. Known INFO problem No. 7291 was encountered when a redundant PAM was reported as inactive after a switchover. This problem was discovered during the Failure/Recovery tests. A new INFO problem report was opened when it was discovered that an output message had replaced all zeroes with an "@". An additional INFO problem report was written against the DART reduction program. None of the anomalies affected the test results. The test was considered successful.

4.1.4.2.2 Summary of DCC Regression Test

This test was conducted while the entire FAA ATC laboratory was operating above the optimum air temperature. The cooling system was severely degraded, due to insufficient government furnished chilled water. During the test run it was deemed necessary to manually switchover to the relatively cooler HOST processor to preserve the integrity of the test. Additionally, all radar was lost intermittently throughout the last third portion of the test. All Monitor functions were verified successfully. INFO problem No. 7373 was written to document the cooling problem.

Air Traffic Laboratory Observations

Switchovers

<u>SIM Time Occurred</u>	<u>Recovery Time (sec)</u>
23:30:06	5
23:31:04	5
00:41:05	6
00:44:36	6 - Additional Switchover Requested by FAA Due to Coolant Problem

Startovers

00:36:01	6
01:17:30	6

4.1.4.2.3 Summary of CDC Regression Test No. 2

Due to source changes to the Monitor software for Builds 10.32CD and 10.32DD, the government deemed it necessary to rerun the Monitor test on the CDC display system. No deviations were performed. No anomalies were observed. The test was considered successful.

Air Traffic Laboratory Observations

Switchovers

<u>SIM Time</u> <u>Occurred</u>	<u>Recovery</u> <u>Time (sec)</u>
23:33:06	8
23:31:04	9
00:41:06	8

Startovers

00:36:02	7
01:17:31	7
01:31:31	7

4.2 FUNCTIONAL TESTS

4.2.1 Overview

Functional testing encompasses all the ATC real-time program elements that process data passed to them by the NAS Monitor and returns the results from distribution to their intended destinations; i.e., display systems, peripherals and interfacilities via the Peripheral Adapter Modules. This test was accomplished in its entirety by using a Government supplied scenario allowing the bulk of verification to be done by off-line data comparison and by visual aids during test conduct. The test extended over a four hour period exercising all aspects of the system based on a scenario that had been generated over a several year span and utilized extensively for system testing of new 9020 systems being released to the field.

Initial Functional testing was accomplished in four sessions between the date of August 26 and October 17, 1986. The system was exercised in a unique configuration each of the sessions as described in subsequent sections. On November 7, 1986, an FAA required regression test was successfully held. A successful problem correction test was held on December 18, 1986. These tests verified that all problems were solved and that the Host Computer System NAS operational software performed all functions as well as, or better than, the 9020 NAS operational system.

4.2.2 Test Description

The functional tests verified that the converted NAS operational software running in the primary processor of the HCS correctly performed all functions at the same or improved level of performance as in the present NAS (9020) computer system. The government furnished Baseline 500 system level functional test series was used in the testing. The Baseline 500 test runs for approximately 4 hours and is designed to test the primary ATC basic functional areas (designated test areas 501 through 506) using a common support data base defined in test area 500. The test areas are as follows:

- 501 - Controller Inputs
- 502 - Surveillance and Tracking
- 503 - R-Controller Inputs and Displays
- 504 - Update Processing
- 505 - Interfacility Testing
- 506 - Flight Plan Processing

The Functional test was run in the Loop SIM mode. All test input data for the Functional tests are contained on radar and non-radar simulation tapes. The HCS read the non-radar inputs directly from tape while radar inputs and interfacility messages were supplied via the Loop SIM interface. The functional tests were run twice, utilizing two separate configurations. In one configuration, SDR was executed in a government furnished 9020 computer. In the other configuration, the hosted version of SDR was executed in the HOST support processor. Prefiled flight plans were entered from the bulk-store file. The tests were conducted with the HCS connected to the DCC and to the CDC (two separate tests) while all test areas are run simultaneously. SAR was enabled throughout the test with a minimum SARC level 4 in effect.

The Functional test was run with the following system interfaces and devices active:

- a. PAM interface required for Loop SIM configuration.
- b. Display channels (CDC, DCC).
- c. All PAM connected devices available in the NAS SSF.

4.2.3 Success Criteria/Analysis Method

Test data were collected via three methods: on-line outputs, SAR tapes, and PVD data. The analysis requirements of these tests were

satisfied by performing a detailed comparison of all the HCS data collected during the test with equivalent 9020 computer system output data. A comparison was performed for each test case. On-line outputs, flight strips, and printer outputs were compared with corresponding 9020 computer system on-line outputs. DART and other data reduction and analysis methods were used for comparisons of SAR data. Specific DART options for these comparisons included Track, Log, and Flight. Sample PVD data were also compared by using government provided item checklists and photographs. Items such as geography, symbology, Full Data Blocks, and aircraft position were compared.

The SAR data collected were also used as the reference data for the Reconfiguration tests and the Failure/Recovery test described in this report.

The Functional tests were considered complete and satisfactory after the HCS data analysis outputs were compared with the 9020 computer system outputs and found to be equivalent or within tolerances acceptable to the government. Any non-comparisons between HCS data and 9020 computer data and other discrepancies were fully explained and documented. The specific explanation and proof provided was approved by the government prior to having the test considered satisfactory. Moreover, the test was repeated to demonstrate proper functional operation.

4.2.4 Test Conduct/Results

4.2.4.1 Formal Tests/Retests

On August 26, 1986, the HCS was connected to the DCC with Loop SIM Driver (SDR) running in the 9020D Simplex and version H10.31DA of the converted NAS software. Nine minor deviations to the government approved test procedures were necessary with four related to configuration changes, four related to procedure errors, and one human error. Three minor anomalies occurred during the test conduct, all related to GFE. One additional anomaly related to a rejected flight plan was observed in the PVD lab. None of the deviations and anomalies had an impact on the test results.

Post-test data analysis yielded 29 distinct anomalies. Sixteen of these were satisfactorily explained by IBM, four were found to be GFE problems, and the remaining nine were software problems that resulted in INFO problem reports and subsequent code changes. The nine problems were consolidated into INFO problem numbers 5113, 6314, 6352, 6180, 6344, and 2868. These were considered minor in nature, having no impact on NAS operations and the test was considered successful.

On August 27, 1986, the Functional test was repeated using the CDC system and using version H10.31CA of the operational software. Eleven deviations from the approved test procedures were experienced, two related to configuration, seven related to procedures, and two were human errors. None were significant. During test conduct, six GFE errors occurred but had no impact on the test results.

Two additional features were tested in this run, the processor instruction execution rate and the on-line edit capability.

Post-test data analysis showed that 13 of the problems seen on the DCC run also occurred on the CDC run. In addition, six new anomalies were found, three were satisfactorily explained by IBM and three resulted in code changes. INFO problem numbers 6288, 6314, and 5113 were associated. These problems were considered minor and the test was considered successful.

The processor executed at an average rate of 6.75 MIPS, well above the specified minimum and the on-line edit function worked well.

The third run was conducted on October 16, 1986, using operational software version H10.31DA, the DCC display channel, and Loop SIM (hosted SDR) running in the standby HOST processor in standalone mode. The configuration was not in accordance with the Engineering Requirement having two representative support tasks executing in the support processor throughout the test.

This had been attempted on prior runs with serious timing differences occurring between the SDR program and the NAS program. Meaningful comparison between the HOST and 9020 data was not possible with these timing problems. It was decided to allow the tests to proceed with SDR only in the support processor pending an IBM solution to the timing problem and to the requirement for multiple support process or tasks working along with SDR.

During the test conduct, a human error caused the loss of some of the HSP output data. Minor anomalies relating to GFE had no impact on test results. Post-test data analysis showed two minor anomalies, both adequately explained by IBM.

The fourth run on October 17, 1986, used operational software version H10.31CA, the CDC displays, and Loop SIM running in the standby processor in standalone mode. No anomalies or deviations were recorded during the test conduct and no new problems were uncovered during post-test analysis.

Except for the requirement to have SDR running under VMCP with other tasks, both run three and run four were considered successful.

During the analysis of the four runs, 41 potential problems were reported. Eleven were DART problems and one was a printer problem. Of the 29 NAS operational problems, all have been resolved to the FAA's satisfaction except for the SDR support processor requirement.

4.2.4.2 Regression Tests

A Functional Baseline 500 Regression test was conducted on November 7, 1986, with system H10.32CB. In this test, the HCS was connected to the CDC Display Channel with the SDR running in the 9020D Simplex System. Analysis of data collected during this run showed no derogation of the system.

4.2.4.3 Problem Correction Test

A Functional Baseline 500 Problem Correction Verification test was conducted on December 18, 1986, with system H10.32DD. In this test, the HCS was connected to the DCC Display Channel with the hosted SDR running in the HOST standby processor under VM. Two additional support tasks were running under VM concurrent with SDR.

The purpose of this test was to verify that the problem described in INFO Problem Report No. 7084 and Request for Action (RFA) 147 was corrected.

Test witnesses reported no deviations or anomalies during test conduct. Analysis of data collected during this run revealed no additional problems. The hosted SDR ran correctly and without loss of time. The problem described in INFO Problem Report No. 7084 and RFA 147 was deemed corrected. This completed all requirements for functional tests.

4.3 CAPACITY AND RESPONSE TIME TESTS

4.3.1 Overview

The purpose of this test was to ensure that the HCS is capable of handling projected future work loads of up to 600 controlled aircraft. This load is anticipated for the middle 1990s time period. The most significant requirement of the test was to process the maximum load without exceeding 43% processor utilization with all resource monitoring simultaneously activated. A total of 24 individual tests with varying load constraints and resource monitoring functions activated were exercised to accomplish the total test. At the completion of each test an intensive data analysis was accomplished to ensure internal saturation during peak loads did not occur.

A series of 24 Capacity and Response Tests were held between September 12 and October 10, 1986. Various minor problems were documented but no major problems occurred. An FAA required regression test held on November 7, 1986, verified that software fixes did not significantly change the Host Computer System performance characteristics. This test was successful except for one major problem. A successful FAA required regression test was held on November 25, 1986, to verify the fix to the problem found during the November 7 test. The 26 tests including 2 regression tests verified the resource monitoring and data recording functions of the HCS and furnished extensive baseline data on the overhead computer utilization required by various resource monitoring and data collection functions, singly and in combination, at different HCS workload levels. HCS capacity and response times were verified to be well within the NAS requirements.

4.3.2 Test Description

Three different types of scenarios were executed during the tests: Baseline 604 Scenario, HOST Workload Scenario, and Special Message Scenario. The Baseline 604 Scenario was designed to maintain a

continuous steady-state track load of 444 tracks. The HOST Workload Scenario was designed to provide steady-state track load of 200-, 400-, or 600-tracks. The 600-track version of the HOST Workload Scenario represents a workload level projected for the year 1995. The third type of scenario, the Special Message Scenario, was designed to simulate specific operational situations and includes keyboard messages which cause the system to respond with predetermined program executions. Unlike the Baseline 604 Scenario and the HOST Workload Scenario, the Special Message Scenario was not designed as a workload scenario.

All Capacity and Response Time tests were performed with the En Route Minimum Safe Altitude Warning (EMSAW) and En Route Metering (ERM) functions activated. The Conflict Alert (CA) function was activated in all tests except those using the Baseline 604 Scenario; this scenario was executed with CA deactivated because of an excessive rate of CAs resulting from many instances of violations of CA separation parameters.

Each scenario was run on both the DCC and the CDC. A total of 24 tests were conducted, supplemented by two Regression tests using the 600-track HOST Workload Scenario. The purpose of the first Regression test was to verify that software fixes implemented during and after the formal test activities did not significantly change the performance characteristics of the HCS. The second Regression test was conducted to verify a fix to a problem identified during the first regression test (see discussion on INFO No. 6475 in paragraph 4.3.3.2). A list of the 26 tests is presented in Table 6.

During the Capacity and Response Time tests, on-line and off-line resource monitoring data pertaining to the utilization of the processor, channels, peripherals, program elements, software addresses, and interrupts were collected. As shown in Table 7, the tests consisted of calibration runs and data collection runs. The objective of the calibration runs was to provide baseline HCS on-line resource monitoring data unaffected by off-line resource monitoring recording overhead. By activating off-line resource monitoring recording during the data collection runs, the overhead caused by this recording was measured.

TABLE 6. LIST OF CAPACITY AND RESPONSE TIME TESTS

<u>Test</u>	<u>Scenario</u>	<u>Display Channel</u>	<u>Date of Test</u>
1	Baseline 604 Scenario	CDC	10/02/86
2	Baseline 604 Scenario	CDC	10/02/86
3	Baseline 604 Scenario	DCC	10/01/86
4	Baseline 604 Scenario	DCC	10/01/86
5	Host Workload Scenario 200-Tracks	CDC	10/10/86
6	Host Workload Scenario 200-Tracks	CDC	10/10/86
7	Host Workload Scenario 200-Tracks	CDC	10/09/86
8	Host Workload Scenario 200-Tracks	DCC	10/04/86
9	Host Workload Scenario 200-Tracks	DCC	10/04/86
10	Host Workload Scenario 200-Tracks	DCC	10/04/86
11	Host Workload Scenario 400-Tracks	CDC	09/24/86
12	Host Workload Scenario 400-Tracks	CDC	09/24/86
13	Host Workload Scenario 400-Tracks	CDC	10/04/86
14	Host Workload Scenario 400-Tracks	DCC	09/25/86
15	Host Workload Scenario 400-Tracks	DCC	09/25/86
16	Host Workload Scenario 400-Tracks	DCC	10/09/86
17	Host Workload Scenario 600-Tracks	CDC	09/16/86
18	Host Workload Scenario 600-Tracks	CDC	09/12/86
19	Host Workload Scenario 600-Tracks	CDC	09/16/86
20	Host Workload Scenario 600-Tracks	DCC	09/18/86
21	Host Workload Scenario 600-Tracks	DCC	09/12/86
22	Host Workload Scenario 600-Tracks	DCC	09/18/86
23	Special Message Scenario	CDC	10/01/86
24	Special Message Scenario	DCC	10/01/86
25*	Host Workload Scenario 600-Tracks	CDC	11/07/86
26*	Host Workload Scenario 600-Tracks	CDC	11/25/86

* Regression tests.

TABLE 7. SUMMARY OF 26 CAPACITY AND RESPONSE TIME TEST CHARACTERISTICS

Test No.	Test Scenario	Display Channel	Data Coll		Calib	Test Duration (hrs)
			1	2		
1	604	CDC	N	N	Y	2.0
2	604	CDC	Y	N	N	2.0
3	604	DCC	N	N	Y	2.0
4	604	DCC	Y	N	N	2.0
5	200	CDC	N	N	Y	2.5
6	200	CDC	Y	N	N	2.5
7	200	CDC	N	Y	N	2.5
8	200	DCC	N	N	Y	2.5
9	200	DCC	Y	N	N	2.5
10	200	DCC	N	Y	N	2.5
11	400	CDC	N	N	Y	2.5
12	400	CDC	Y	N	N	2.5
13	400	CDC	N	Y	N	2.5
14	400	DCC	N	N	Y	2.5
15	400	DCC	Y	N	N	2.5
16	400	DCC	N	Y	N	2.5
17	600	CDC	N	N	Y	2.5
18	600	CDC	Y	N	N	2.5
19	600	CDC	N	Y	N	2.5
20	600	DCC	N	N	Y	2.5
21	600	DCC	Y	N	N	2.5
22	600	DCC	N	Y	N	2.5
23	SMG*	CDC	Y	N	N	1.5
24	SMG*	DCC	Y	N	N	1.5
25**	600	CDC	Y	N	N	1.5
26**	600	CDC	Y	N	N	1.5

* Special Message Scenario (SMG)

** Regression tests

TABLE 7. SUMMARY OF 26 CAPACITY AND RESPONSE TIME TEST CHARACTERISTICS (CONTINUED)

Data Recorded

Test No.	HRT	TAR	SAR	REMON	DLOG	AMP	CA	EMSAW
1	N	N	N	N	N	N	N	Y
2	N	Y	Y	Y	Y	Y	N	Y
3	N	N	N	N	N	N	N	Y
4	N	Y	Y	Y	Y	N	N	Y
5	N	N	N	N	N	N	Y	Y
6	N	Y	Y	Y	Y	Y	Y	Y
7	Y	N	Y	Y	Y	Y	Y	Y
8	N	N	N	N	N	N	Y	Y
9	N	Y	Y	Y	N	Y	Y	Y
10	Y	N	Y	Y	N	Y	Y	Y
11	N	N	N	N	N	N	Y	Y
	N	Y	Y	Y	N	N	Y	Y
12	N	Y	Y	Y	Y	Y	Y	Y
13	Y	N	Y	Y	Y	Y	Y	Y
14	N	N	N	N	N	N	Y	Y
15	N	Y	Y	Y	N	Y	Y	Y
16	Y	N	Y	Y	N	Y	Y	Y
17	N	N	N	N	N	N	Y	Y
18	N	Y	Y	Y	Y	Y	Y	Y
19	Y	N	Y	Y	Y	Y	Y	Y
20	N	N	N	N	N	N	Y	Y
21	N	Y	Y	Y	N	Y	Y	Y
22	Y	N	Y	Y	N	Y	Y	Y
23*	N	Y	Y	Y	N	N	N	Y
24*	N	Y	Y	Y	N	N	N	Y
25**	N	Y	Y	Y	Y	Y	Y	Y
26**	N	Y	Y	Y	Y	Y	Y	Y

* Special Message Scenario (SMG)
 ** Regression tests

In both of the calibration runs and data collection runs, all on-line resource monitoring recordings were activated. On-line resource monitoring consisted of utilization data for the following: processor, channels, memory, peripherals, interrupts and program elements. In the data collection runs, one of two program timing analysis tools was used: Timing Analysis Recording (TAR) was used in Data Collection run 1, and the HRT was used in Data Collection run 2. In addition, the System Analysis Recording (SAR) and REMON functions were active in all data collection runs. The SAR recording level was changed during the data collection runs (i.e., SARC4 to SARC1) in compliance with the Engineering Requirement. The Baseline 604 Scenario and the HOST Workload Scenario data collection runs included the activation of Aircraft Management Program (AMP) and CDC Data Log (DLOG), when applicable.

Two 600-track HOST Workload Scenario runs (tests 17 and 20) were extended to obtain HCS performance data with all resource monitoring tools activated (i.e., SARC4, TAR, REMON, HRT, AMP, DLOG, and on-line resource monitoring). Also, two 200- and two 400-track HOST Workload Scenario runs (tests 8, 10, 14, and 16) were extended to obtain processor utilization data for comparison with utilization estimates provided in the Resource Monitoring Analysis Report (CDRL item B050).

The 24 formal Capacity and Response Time tests were conducted on two NAS operational software Builds. The Baseline 604 Scenario and Special Message Scenario tests performed using the NAS operational software Build H10.31, while the HOST Workload Scenario tests were conducted with Build W10.31B. Different Builds had to be used because the HOST Workload Scenario tests required changing the definition of the Universal Data Set (UDS) adjacent airspace in addition to increasing table sizes to prevent saturation of queues and tables. The regression tests were conducted using the NAS operational software Build W10.32D, which was the system delivered to the Seattle Center in November 1986.

Each of the three scenarios, the Baseline 604 Scenario, HOST Workload Scenario, and Special Message Scenario, was run on both the DCC and CDC in the Loop-SIM mode using the 9020D system to drive the HCS. The Loop-SIM mode, which permits the simulation of interfacility messages, is also used to input radar data into the HCS from an external source for a better emulation of the operational system. The HCS primary processor executed the NAS operational software and the support processor executed the non-NAS software, the DART, and NAS Standby system. The System Measurement Instrument (SMI), an IBM-supplied hardware monitoring tool, was connected to the primary processor to provide processor utilization, channel utilization, and instruction execution rate in MIPS. In addition, the Monitoring and System Support Facility (MSSF), which is part of the HOST Computer System, was used to obtain processor utilization and channel utilization of the primary and support processors.

During the conduct of all the Capacity and Response Time tests, the FAA team witnesses were positioned at various locations in the computer room and the display laboratory to observe test inputs,

events, and expected results as specified in the Capacity and Response Time tests procedure (CDRL Item B072-OPS). All significant events and unplanned deviations were documented in witness logs during the tests.

4.3.3 Success Criteria/Analysis Method

The test analysis was performed by reviewing test witness logs, HCS and 9020D messages sent to the HSPs, medium speed printers (MSPs), and keyboard printers (KPRs). Specifically, the following computer data were used in the analysis:

- a. HCS Operational Messages (HSP)
- b. Resource Monitoring Messages and Operational Messages (KPR1)
- c. Resource Monitoring Tape Start or End Times (KPR2)
- d. Status of Support Jobs (MVS KPR, SMART)
- e. Conflict Alert Data (CA HSP data reduced from tape)
- f. Loop-SIM Operational Messages (9020D HSP)
- g. 9020D Operational Messages (9020D IOT)
- h. Status of CDC or DCC (Display Channel IOT)
- i. MIPS Rate, Processor, and Channel Utilization (SMI, REDUC)
- j. HCS Response Time (DART Response)
- k. Functional Aspects of HOST Processing (DART Flight, Log, and Track)
- l. Storage Utilization (REMON)
- m. HCS On-Line Resource Monitoring Data (SURP)
- n. Processor and Channel Utilization (MSSF)
- o. Traffic Statistics (AMP)
- p. Communications Between the HCS and the CDC (DLOG)
- q. Processor, Channels, Peripherals, Interrupts, Program Elements, Software Address and Software Category Statistics and Response Times (HRT REDUC)

- r. Processor, Channel, Peripheral, Interrupt, Program Elements, and Software Category Statistics and Response Time (TARP REDUC)
- s. Storage and Program Element Statistics (REMON)

For all tests, the local outputs were reviewed to ensure that the system performed as expected. The response times for the radar, local, and remote source messages (Priority Classes 2, 3, 4, 5, and 6) were measured and compared to those specified in NAS-MD-318. Statistics were collected for the following: subsystem utilizations, track load, and proposed and active flight plans. The local outputs and resource monitoring data generated during the testing of the 200-track HOST Workload Scenario, Baseline 604 Scenario, and the Special Message Scenario were compared to data obtained from running these scenarios on the 9020.

The emphasis of the Capacity and Response Time test analysis was on evaluating the HCS performance using the 600-track HOST Workload Scenario. These tests were also used to evaluate the accuracy of HCS resource monitoring tools. Specific HCS applications and monitor functions were analyzed by comparing HCS outputs with 9020 GFE DART, flight, log, and track data for the 600-track HOST Workload Scenario tests.

4.3.4 Test Conduct/Results

4.3.4.1 Formal Tests/Retests

The Capacity and Response Time Test analysis demonstrated that the HCS performance in terms of processor capacity and response times meets the Engineering Requirement specification. In the course of testing and analysis, several software problems were identified and documented in the HCS INFO problem data base.

4.3.4.1.1 Processor Utilization Results

During the Baseline 604 Scenario tests, both CDC and DCC, the HCS processed a steady-state track load of approximately 450 tracks. The track loads in the Baseline 604 Scenario tests (tests 1, 2, 3, 4) are presented in Figure 5.

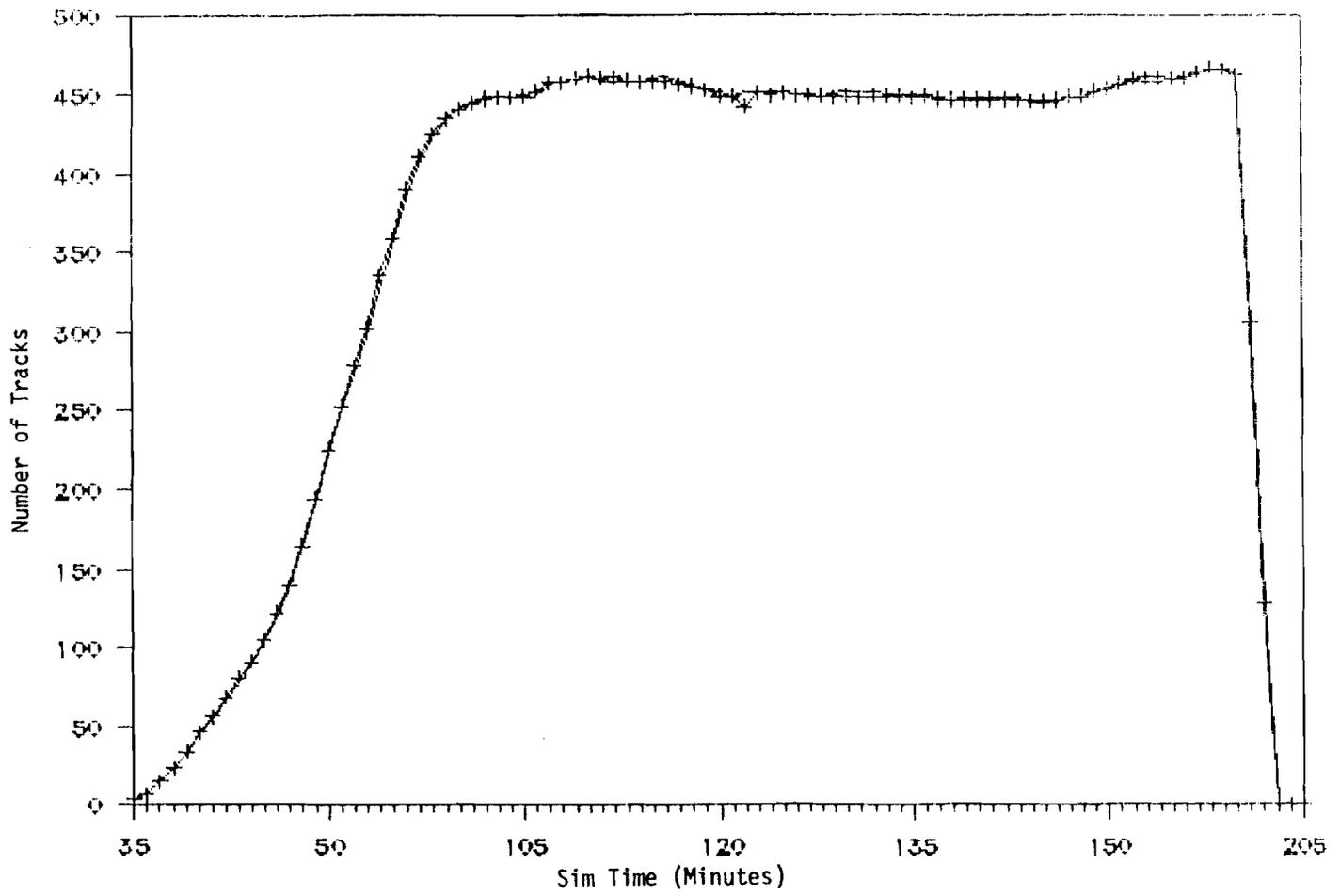


FIGURE 5. TRACK LOAD VS. TIME BASELINE 604 SCENARIO

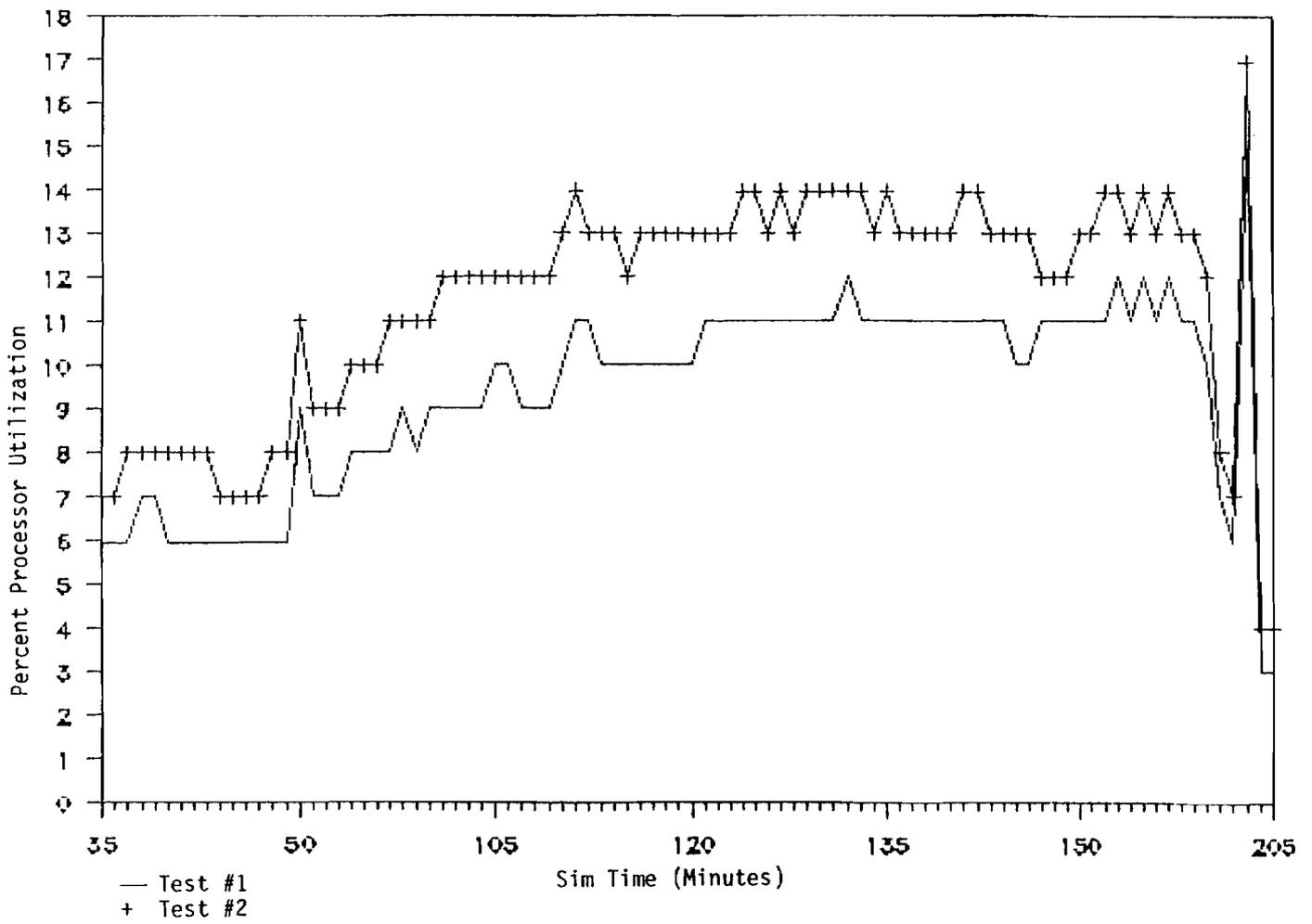


FIGURE 6. PROCESSOR UTILIZATION, CDC TESTS 1 AND 2

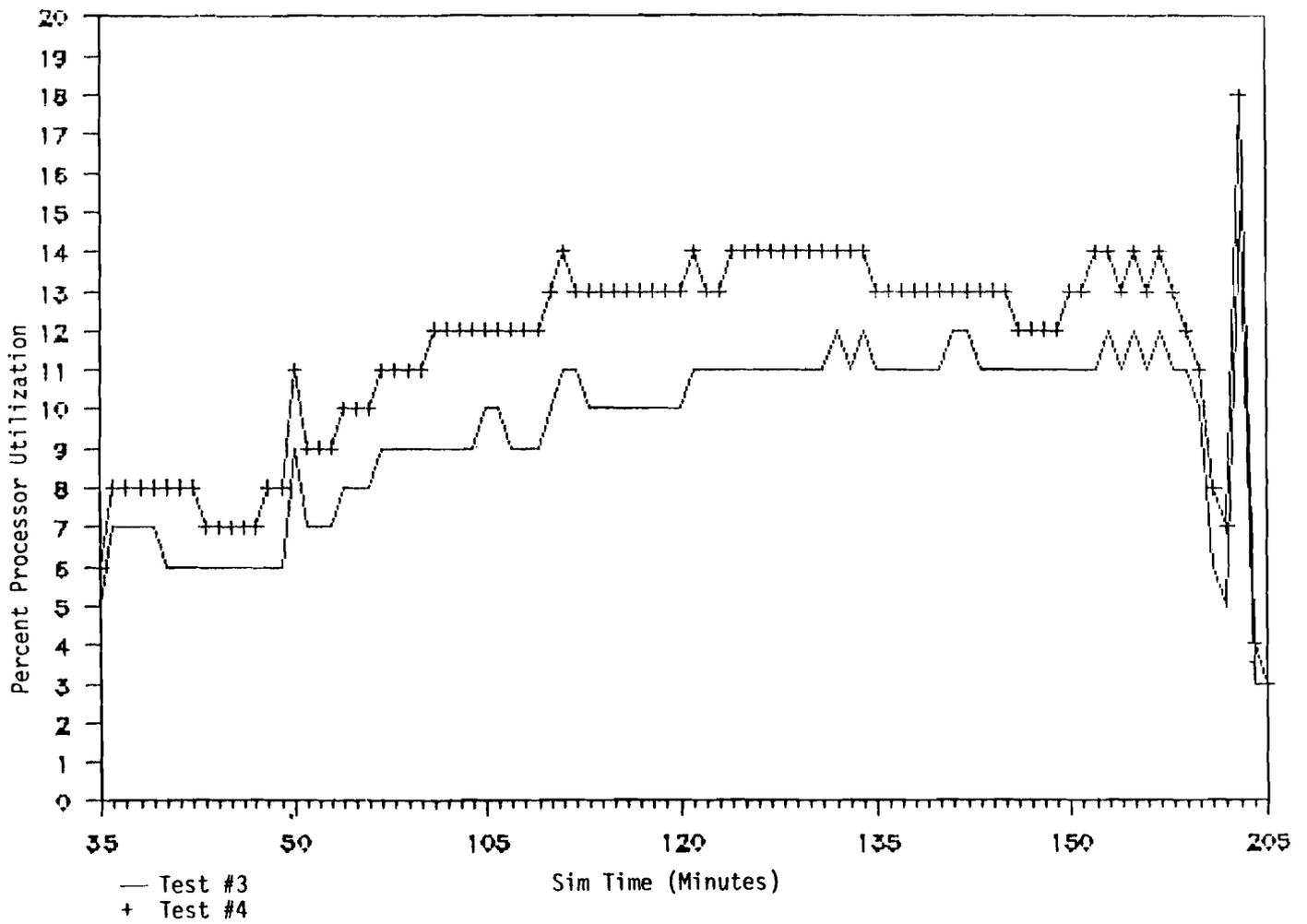


FIGURE 7. PROCESSOR UTILIZATION, DCC TESTS 3 AND 4

The maximum measured processor utilization with on-line resource monitoring recording, SAR, TAR, REMON, AMP, and CDC DLOG was 14 percent (Figures 6 and 7) except at the end of the session during planned shutdown. As shown in Figures 6 and 7, the processor utilization increased momentarily during the planned shutdown (i.e., time 0200), because of the overhead associated with terminating all resource monitoring and flight data processing, which is similar to what the 9020 exhibits upon shutdown. The difference between the maximum processor utilization for the calibration runs (tests 1, 3) and data collection runs (tests 2, 4) was between 1 and 4 percent.

A steady-state track load of 200-, 400-, and 600-tracks was maintained throughout all HOST Workload Scenario testing. Figure 8 shows the track loads for all HOST Workload Scenario tests conducted with the DCC. Although the track loads for tests 9, 15, and 21 are shown in Figure 8, similar load profiles were also applied to the other HOST Workload Scenario tests.

The processor utilization data for the HOST Workload Scenario, CDC, calibration tests are presented in Figure 9. As shown in the Figure, the maximum processor utilization values measured during the 200-, 400-, and 600-track tests, before SIM time 1330, were 10, 17, and 26 percent, respectively. At 1330, processor utilization increased because all resource monitoring tools were activated at that time (note that this is not the normal configuration and was used for test purposes only); that is, after 1330, HRT and TAR were active simultaneously. This caused processor utilization to increase by 1, 3, and 14 percent in the 200-, 400-, and 600-track tests.

The processor utilization data for the HOST Workload Scenario calibration tests using the DCC are shown in Figure 10; they were virtually the same as those in the CDC tests. At 1330, all resource monitoring tools were activated during the 600-track HOST Workload Scenario run (test 20), as in the CDC test. The maximum processor utilization value measured during this test interval was 39 percent, as compared to 40 percent for the 600-track HOST Workload Scenario, CDC run (test 17).

The data collection runs, with on-line and off-line resource monitoring functions activated for the HOST Workload Scenario, CDC tests, are presented in Figures 11 and 12. In the data collection runs, one of two program timing analysis tools was used: TAR in data collection run 1, and the HRT in data collection run 2. Processor utilization data for collection run 1, which used "normal resource monitoring", are shown in Figure 11. The term "normal resource monitoring" refers to the following on-line and off-line resource monitoring functions activated: SAR, TAR, REMON, AMP, and CDC DLOG. As shown in Figure 11, the maximum measured processor utilizations for data collection run 1 were 13, 22, and 32 percent, respectively.

The processor utilization data for the HOST Workload Scenario data collection run 2 using the CDC are shown in Figure 12. The activation of the HRT function increased the maximum processor utilization value for the 600-track HOST Workload Scenario run (test 19) to 39 percent. The value is 7 percent higher than in data collection run 1. However, when both TAR and HRT were active simultaneously, the maximum processor utilization was 40 percent. The increase in processor utilization for test 19 after time 1330 was caused by planned shutdown. A planned shutdown for tests 7 and 13 was executed at time 1340 and is not reflected in Figure 12.

The processor utilization data for the HOST Workload Scenario, DCC, data collection run 1 are shown in Figure 13. Similar maximum processor utilization values for data collection run 1 were obtained from the corresponding CDC tests (Figure 11).

The processor utilization data for the HOST Workload Scenario, DCC, data collection run 2 are shown in Figure 14. The maximum processor utilization value measured was 37 percent for the 600-track HOST Workload Scenario run. The difference between data collection run 1 and data collection run 2 was 4 percent for the DCC tests, as compared to 7 percent for the CDC tests. An increase in processor utilization for test 22 after time 1330 was caused by planned shutdown. A planned shutdown for tests 10 and 16 was executed at time 1340 and is not reflected in Figure 14.

The analysis confirmed that the HCS processed a workload of 600 tracks with "normal resource monitoring" active within the Engineering Requirement specification of 43 percent; the maximum processor utilization measured under this condition was 33 percent. Even with all on-line and off-line resource monitoring functions activated (not a normal configuration in an operational environment), the HCS did not exceed the Engineering Requirement specification maximum processor utilization.

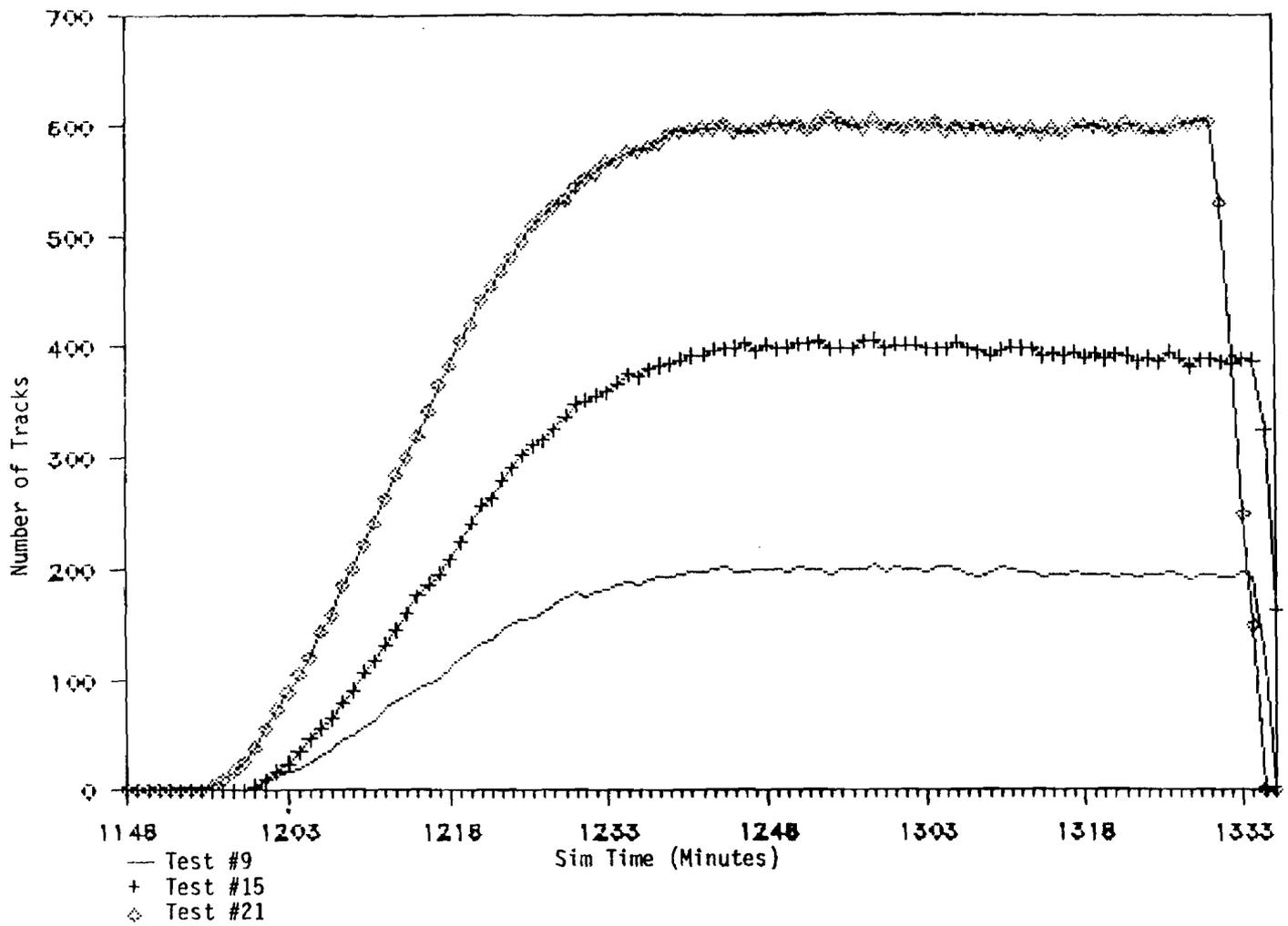


FIGURE 8. TRACK LOAD VS. TIME HOST WORKLOAD SCENARIO (TAR)

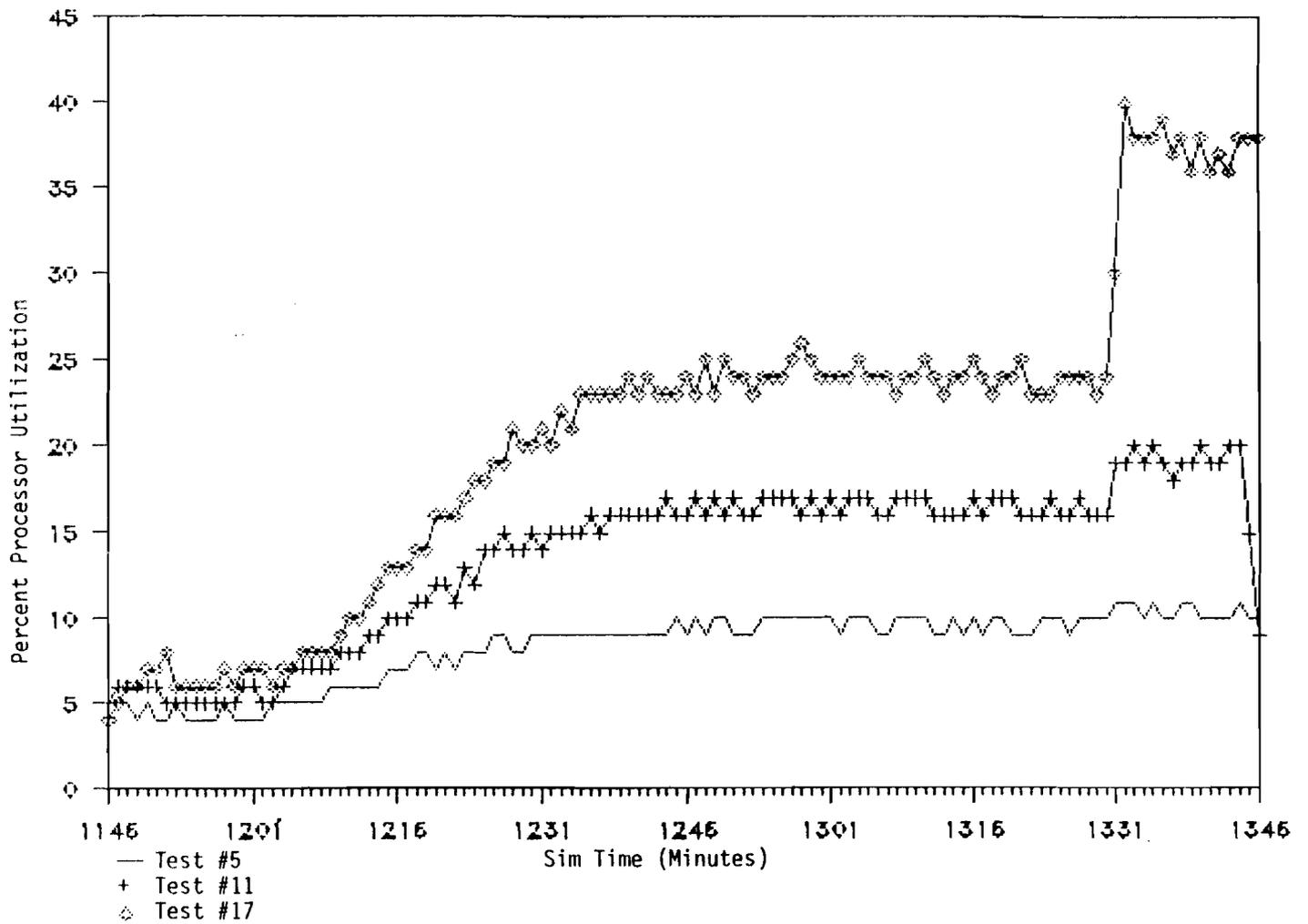


FIGURE 9. PROCESSOR UTILIZATION, CDC TESTS 5, 11, AND 17

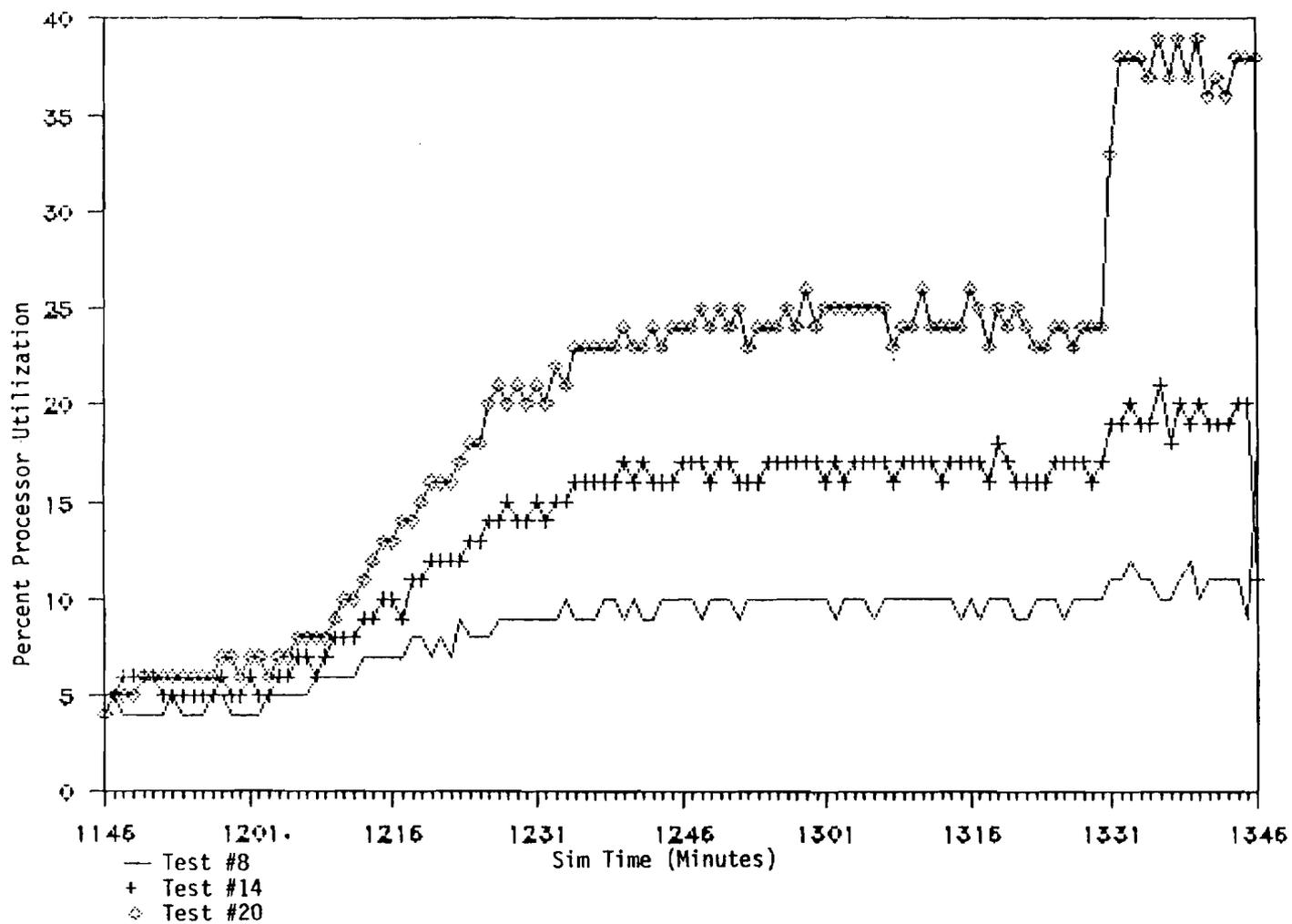


FIGURE 10. PROCESSOR UTILIZATION, DCC TESTS 8, 14, AND 20

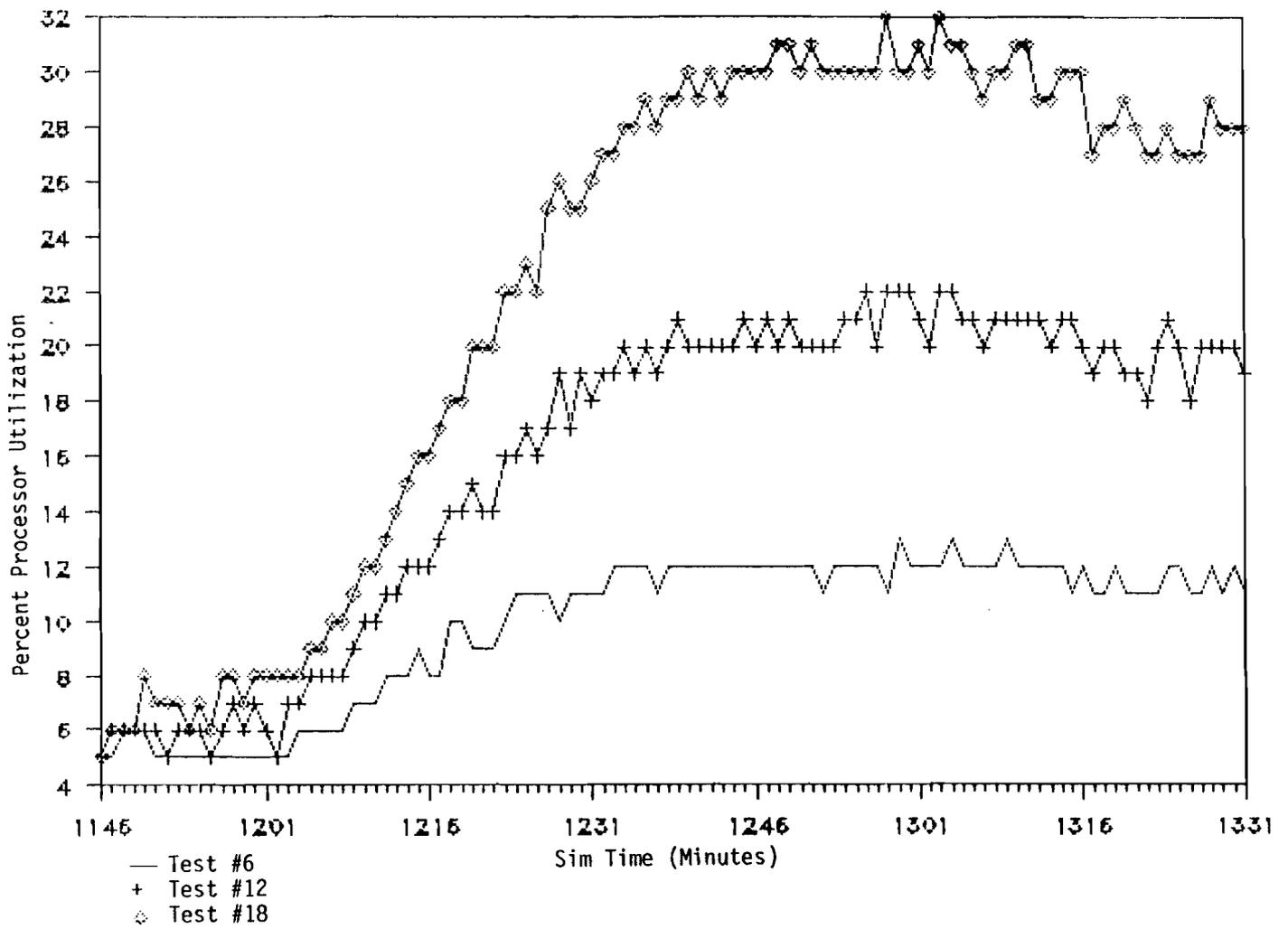


FIGURE 11. PROCESSOR UTILIZATION, CDC TESTS 6, 12, AND 18

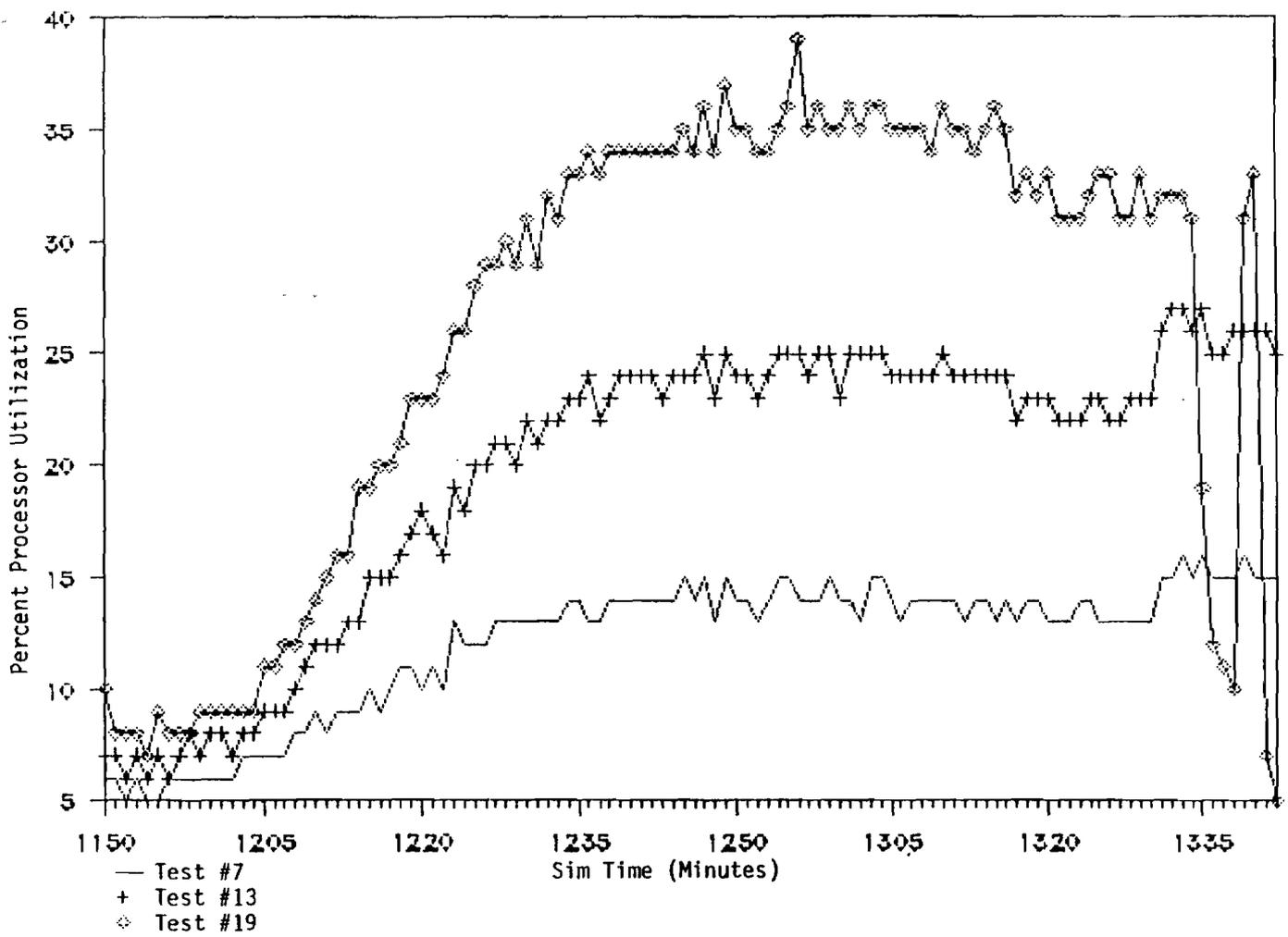


FIGURE 12. PROCESSOR UTILIZATION, CDC TESTS 7, 13, AND 19

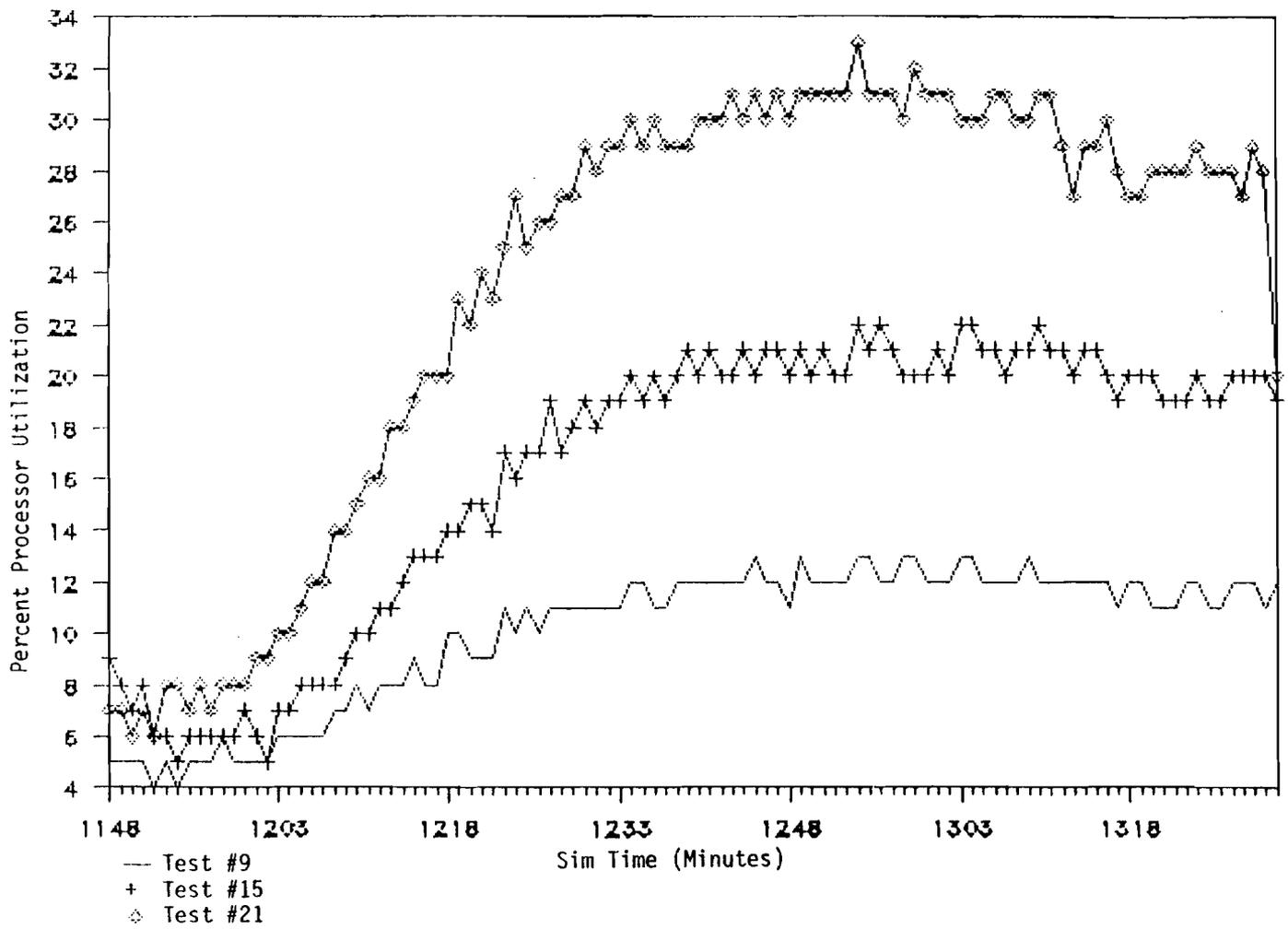


FIGURE 13. PROCESSOR UTILIZATION, DCC TESTS 9, 15, AND 21

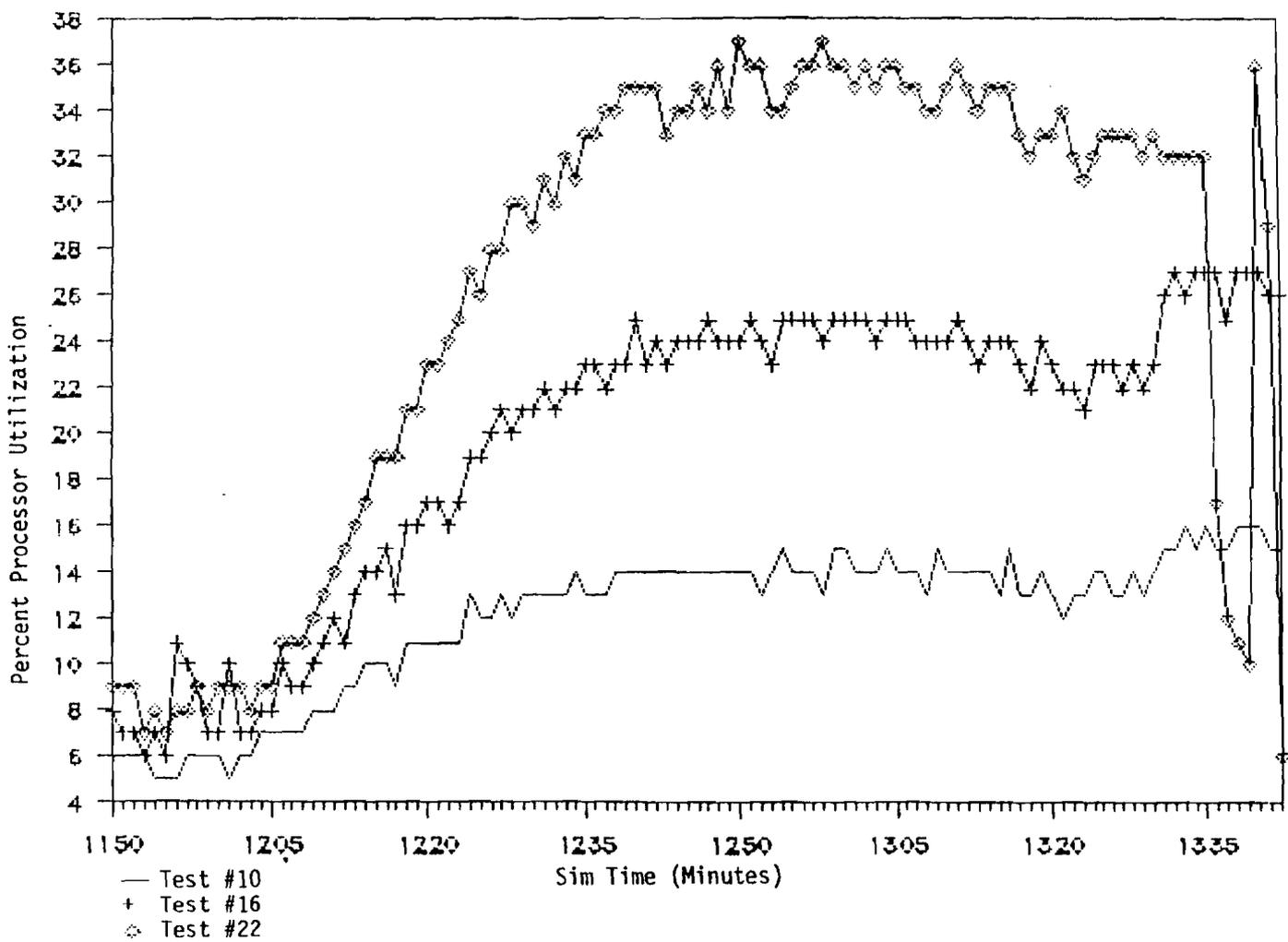


FIGURE 14. PROCESSOR UTILIZATION, DCC TESTS 10, 16, AND 22

4.3.4.1.2 Response Time Results

The HCS P2, P3, P4, P5, and P6 response time messages were evaluated for compliance with the Engineering Requirement and NAS-MD-318 requirements. These response times were measured using two tools: DART Response and the Response Time Tool (RTT) were used for P3 through P6 messages, while HRT REDUC and TAR REDUC were used to obtain P2 response times. The response times of the six tests that used the 600-track HOST Workload Scenario and the last regression test (test 26) are presented in Table 8. The table contains the mean and 90th percentile measurements as compared to the NAS-MD-318 specified values. As shown in this table, all HCS response times were well within the NAS-MD-318 requirement.

Note that in some cases, the 90th percentile was less than the mean; this was caused by the 0.5 second resolution of SAR data and an abnormal message distribution.

A data reduction problem was discovered during the Special Message Scenario test analysis of the DART Response data, which revealed that P6 messages failed both the mean and 90th percentile requirements. This problem was investigated and it was determined that the anomaly resulted from inaccuracies in DART processing rather than slow HCS response times for P6 messages. The problem was corrected by eliminating invalid message pairs in the DART program. The 600-track test results were unaffected.

FAA analysis revealed that the DART Response tool needs to be modified to eliminate certain mismatches of input-output message pairs to provide more accurate response time results. Since the response times produced by DART Response were well within the NAS-MD-318 requirements, the few mismatches would not have significantly affected the test results. The RTT program matches more input-output message pairs than DART Response and, thereby, measures HCS response times more accurately. A few RTT mismatches, which were discovered during the HOST Workload Scenario test analysis, were subsequently fixed by modifying the RTT program. However, there is a need to validate that all possible message pairs (including those that do not occur in the capacity test scenario) are correctly handled by both DART Response and RTT.

TABLE 8. RESPONSE TIME SUMMARY FOR 600-TRACK
HOST WORKLOAD SCENARIO TESTS (IN SECONDS)

<u>Test 17</u>											
<u>Test Time</u>	<u>P2</u>		<u>P3</u>		<u>P4</u>		<u>P5</u>		<u>P6</u>		<u>Tool Used</u>
	<u>Mean</u>	<u>90</u>	<u>Mean</u>	<u>90</u>	<u>Mean</u>	<u>90</u>	<u>Mean</u>	<u>90</u>	<u>Mean</u>	<u>90</u>	
1245-1315	-	-	-	-	-	-	-	-	-	-	DART/ REDUC
1315-1330	-	-	-	-	-	-	-	-	-	-	
*1332-1347	(1)	(2)	0.253	0.5	0.281	0.5	0.234	0.5	0.718	1.5	
1245-1315	-	-	-	-	-	-	-	-	-	-	RTT
1315-1330	-	-	-	-	-	-	-	-	-	-	
*1332-1347	-	-	0.11	0.5	0.19	0.5	0.59	1.5	0.35	1.0	
NAS-MD-318											
Requirement	1.5	2.0	1.5	3.0	2.0	4.0	3.0	6.0	4.0	8.0	
Notes:											
	(1)	0.590 (HRT REDUC),		0.583 (TAR REDUC)							
	(2)	0.7 (HRT REDUC),		0.6 (TAR REDUC)							
	*	All on-line and off-line tools activated									
	-	Data not generated during calibration tests									

<u>Test 18</u>											
<u>Test Time</u>	<u>P2</u>		<u>P3</u>		<u>P4</u>		<u>P5</u>		<u>P6</u>		<u>Tool Used</u>
	<u>Mean</u>	<u>90</u>									
1245-1315	0.633	0.7	0.128	0.5	0.406	0.5	0.472	0.5	0.800	1.5	DART/ REDUC
1315-1330	0.631	0.7	0.156	0.5	0.335	0.5	0.406	0.5	0.750	1.0	
1245-1315	-	-	0.100	0.5	0.150	0.5	0.630	1.5	0.400	1.0	RTT
1315-1330	-	-	0.080	0.5	0.240	0.5	0.550	1.0	0.330	0.5	
NAS-MD-318											
Requirement	1.5	2.0	1.5	3.0	2.0	4.0	3.0	6.0	4.0	8.0	

TABLE 8. RESPONSE TIME SUMMARY FOR 600-TRACK
HOST WORKLOAD SCENARIO TESTS (IN SECONDS)
(CONTINUED)

<u>Test 19</u>											
<u>Test Time</u>	P2		P3		P4		P5		P6		<u>Tool Used</u>
	<u>Mean</u>	<u>90</u>									
1245-1315	0.561	0.5	0.121	0.5	0.414	0.5	0.457	0.5	0.824	1.5	DART/
1315-1330	0.604	0.6	0.266	0.5	0.316	0.5	0.347	0.5	0.726	1.0	REDUC
1245-1315	-	-	0.090	0.5	0.290	0.5	0.640	1.5	0.410	1.0	RTT
1315-1330	-	-	0.100	0.5	0.310	0.5	0.620	1.0	0.380	0.5	
NAS-MD-318 Requirement	1.5	2.0	1.5	3.0	2.0	4.0	3.0	6.0	4.0	8.0	

<u>Test 20</u>											
<u>Test Time</u>	P2		P3		P4		P5		P6		<u>Tool Used</u>
	<u>Mean</u>	<u>90</u>									
1245-1315	-	-	-	-	-	-	-	-	-	-	DART/
1315-1330	-	-	-	-	-	-	-	-	-	-	REDUC
*1332-1347	(1)	(2)	0.250	1.0	0.312	0.5	0.328	0.5	0.843	1.5	
1245-1315	-	-	-	-	-	-	-	-	-	-	RTT
1315-1330	-	-	-	-	-	-	-	-	-	-	
*1332-1347	-	-	0.210	1.0	0.300	0.5	0.940	4.5	0.570	1.5	
NAS-MD-318 Requirement	1.5	2.0	1.5	3.0	2.0	4.0	3.0	6.0	4.0	8.0	

Notes: (1) 0.590 (HRT REDUC), 0.583 (TAR REDUC)
(2) 0.7 (HRT REDUC), 0.6 (TAR REDUC)
* All on-line and off-line tools activated
- Data not generated during calibration tests

TABLE 8. RESPONSE TIME SUMMARY FOR 600-TRACK
HOST WORKLOAD SCENARIO TESTS (IN SECONDS)
(CONTINUED)

Test 21

<u>Test Time</u>	<u>P2</u>		<u>P3</u>		<u>P4</u>		<u>P5</u>		<u>P6</u>		<u>Tool Used</u>
	<u>Mean</u>	<u>90</u>									
1245-1315	0.587	0.6	0.132	0.5	0.285	0.5	0.585	0.0	0.812	1.5	DART/ REDUC
1315-1330	0.587	0.6	0.136	0.5	0.285	0.5	0.031	0.0	0.695	1.0	
1245-1315	-	-	0.080	0.5	0.090	0.5	0.600	1.0	0.42	0.5	RTT
1315-1330	-	-	0.070	0.5	0.050	0.5	0.430	0.5	0.34	0.5	
NAS-MD-318 Requirement	1.5	2.0	1.5	3.0	2.0	4.0	3.0	6.0	4.0	8.0	

Test 22

<u>Test Time</u>	<u>P2</u>		<u>P3</u>		<u>P4</u>		<u>P5</u>		<u>P6</u>		<u>Tool Used</u>
	<u>Mean</u>	<u>90</u>									
1245-1315	0.597	0.7	0.144	0.5	0.425	0.5	0.535	0.5	0.851	1.5	DART/ REDUC
1315-1330	0.609	0.6	0.156	0.5	0.289	0.5	0.113	0.0	0.667	1.0	
1245-1315	-	-	0.160	0.5	0.260	0.5	0.700	2.0	0.480	1.0	RTT
1315-1330	-	-	0.080	0.5	0.160	0.5	0.510	0.5	0.340	0.5	
NAS-MD-318 Requirement	1.5	2.0	1.5	3.0	2.0	4.0	3.0	6.0	4.0	8.0	

Test 26

<u>Test Time</u>	<u>P2</u>		<u>P3</u>		<u>P4</u>		<u>P5</u>		<u>P6</u>		<u>Tool Used</u>
	<u>Mean</u>	<u>90</u>									
1245-1315	0.581	0.6	0.195	0.5	0.296	0.5	0.429	0.5	0.824	1.5	DART/ REDUC
1315-1330	0.580	0.6	0.175	0.5	0.171	0.5	0.179	0.0	0.746	1.0	
NAS-MD-318 Requirement	1.5	2.0	1.5	3.0	2.0	4.0	3.0	6.0	4.0	8.0	

Note: Response Time data are presented for test 26 and not test 25 because test 26 used the most recent HCS software version.

4.3.4.1.3 MIPS and Resource Monitoring Measurements

The SMI REDUC output confirmed that the HCS processed approximately 7.3 MIPS during the 600-track HOST Workload Scenario tests. This value surpassed the Engineering Requirement specification of 4.3 MIPS. The Engineering Requirement did not specify maximum utilization requirements for HCS channels, peripherals, program elements, and interrupts. However, the utilization data measured by the various on-line and off-line resource monitoring tools were collected and compared. Analysis confirmed that other than the three REDUC problems discussed in paragraph 4.3.3.2 all HCS resource monitoring tools produced approximately the same utilization data.

4.3.4.2 Regression Tests/Verification Tests

One critical TYPE I problem occurred during test 25 involving the "REMI OFF" message. This message is used to deactivate HRT and the on-line reporting of utilization data for the following items: processor, channels, storage peripherals, program elements, interrupts, and software addresses. When the "REMI OFF" message was entered during test 25, an I/O lockout occurred in the operational system. The problem was documented as INFO No. 7370 and the fix was successfully demonstrated during the second regression run (test 26).

It was discovered during the P2 message analysis that the HCS REDUC program did not account for Radar Input Processing subprogram (RIN) processing time (INFO No. 7137). RIN performs message identification, validity-checking, rho-theta filtering, coordinate conversion, radar sort box determination, selective rejection, and Mode C pressure correction for input radar data. If RIN's processing were accounted for in the REDUC program, the HCS P2 response time would increase by 8 milliseconds above the currently reported figure of 560-630 milliseconds for a 600-track load. The fix for this type II problem was not demonstrated during the regression tests.

A software problem in the AMP program was discovered during the analysis of the HOST Workload Scenario and the Baseline 604 Scenario tests. The AMP program produced erroneous track load statistics (INFO 7735). Other related AMP problems were discovered during the Baseline 604 Scenario and HOST Workload Scenario test analysis. The fix for this type II problem was not demonstrated during regression testing although these problems have since been fixed by the FAA on a new AMP release.

One type III problem occurred during a 400-track HOST Workload Scenario run (test 11). The problem involved the "REMI OFF" message. When the "REMI OFF" message was entered, an unsuccessful switchover was attempted by the system. It was discovered that a switchover occurred because the PAMs were not configured as available to NAS Standby and VM. The problem was documented as INFO No. 6475.

During the 600-track HCS HSP analysis, it was discovered that 300-word pool blocks became saturated during planned shutdown (INFO No. 7020). To fix this type III problem, the number of 300-word pool blocks,

which is adaptable, was increased from 100 to 300. The fix was successfully demonstrated during test 26.

When the CDC DLOG outputs were analyzed for the 600-track HOST Workload Scenario tests two problems were discovered and documented in INFO No. 5541. The first problem documented that DLOG message times were garbled. The second problem documented that aircraft data blocks were missing. The fixes for these type III problems were not demonstrated during the regression tests.

During the conduct of the Capacity and Response Time tests, output messages to the KVDT were occasionally printed twice (INFO No. 5911). It was later found that this problem had been identified during the HCS Live Radar test and had been included in that test's INFO data base. The fix for this type III problem was not demonstrated during the regression tests.

Each of the on-line and off-line HCS resource monitoring tools was analyzed for the 600-track HOST Workload Scenario tests. Two software problems (INFO No. 7245 and No. 7562) associated with the REDUC program, which affected the reported processor utilization data and program element statistics, were discovered. INFO No. 7245 addressed an erroneous mean execution time of a program element in the REDUC SVC statistics summary. The second problem, INFO No. 7562, documented the fact that the processor utilization statistics, as reported by the TAR function, were lower than those reported by HRT by approximately 2 percent. An analysis of these problems revealed that both existed in the current 9020 software and were not HCS problems.

A number of other unplanned test inputs, events, and unexpected results were observed during the conduct of the 26 Capacity and Response Time tests. These minor deviations, which were recorded in the test witness logs, had no significant effect on the execution or success of the Capacity and Response Time Tests.

4.4 RECONFIGURATION TESTS

4.4.1 Overview

Reconfiguration testing verified the HCS's ability to reconfigure associated equipments; disk storage units, printers, terminals, tape units, display interfaces, PAM equipments, channels, etc., all of which are required to be redundant in and out of the system. Reconfiguration test cases were induced both by manual request and unit failures. The principle requirement of this test was to prove there was no single point of failure throughout the system. The test was run in a real-time environment with both the primary and support computers active.

A series of reconfiguration tests were held on October 7 and 8, 1986. Various minor problems were documented but no major problems occurred. FAA required regression tests were successfully held on November 4, 5, and 11, 1986, with no major problems. On November 13, 1986, a successful problem verification test was held. All tests verified

that the HCS performed correct reconfigurations in response to element failures or operator requests without loss of Air Traffic Control functions.

4.4.2 Test Description

The Reconfiguration tests verified the ability of the HCS, while executing the NAS operational software, to perform reconfigurations in response to unit failures, operator requests for reconfigurations, and failures in the PAM and the Display Channel. Moreover, Reconfiguration tests demonstrated that a single failure did not degrade the ATC system operation and demonstrated the capability of the HCS operator to visually monitor the status of each unit and subsystem.

Reconfiguration testing verified the correct response to failures and manual requests for reconfiguration in the following system elements:

- a. DAS Channel
- b. DAS Controller
- c. DAS Unit
- d. Tape Channel
- e. Tape Controller
- f. Tape Unit
- g. RDC (CDC and DCC)
- h. RDC Channel
- i. RDC Interface
- j. PAM
- k. Channel-to-Channel Adaptor
- l. Line Printer
- m. Console Printer
- n. KVDT

Reconfiguration tests were conducted while the HCS was executing the Baseline 500 Functional Test Scenario in the primary processor. The HCS Support processor was executing a minimum of two representative support tasks during the Reconfiguration tests. The Baseline 500 Functional Test Scenario was run a minimum of 5 minutes after the completion of each reconfiguration.

Two system runs were conducted for these tests: one run with the DCC configured system, and the other run with the CDC configured system. The test runs included induced element failures and operator requests for reconfiguration.

Data to be used for on-line and post-test analysis were collected during conduct of the Reconfiguration tests. Data for the post-test analysis was collected on a SAR using SARC level 4.

4.4.3 Success Criteria/Analysis Method

The on-line test analysis conducted during the test run consisted of a visual inspection of PVDs, the console printer, and the status KVDTs. The on-line analysis verified that the HCS performed the correct reconfigurations in response to the element failures and operator requests for reconfiguration, and that no loss of ATC functions occurred. After the test run was complete, and the on-line analysis indicated successful operation, a post-test analysis was conducted. The post-test analysis consisted of a detailed analysis of the SAR data generated by the test run and was used to determine if the induced element failures and subsequent reconfigurations had any impact upon ATC operational software functions or data. The data resulting from the baseline 500 scenario for the Functional test was used as a reference to compare data collected during the Reconfiguration tests.

The tests were considered successful when the HCS demonstrated: (1) its ability to reconfigure failing elements out of the operational system, (2) its ability to switch in the proper backup elements, and (3) the induced element failures with their resulting reconfigurations did not impact normal operation of the ATC operational functions or data.

4.4.4 Test Conduct/Results

A Formal test and a Regression test were conducted for each of the display channels (DCC and CDC) and a CDC Verification test resulted in five tests being conducted.

The Reconfiguration test was considered successful. The test verified the ability of the HCS hardware and software to be successfully reconfigured and to recover from induced failures.

The HCS successfully detected, analyzed, and reported each failure, and maintained operational configuration for the ATC functions without any degradation of performance.

4.4.4.1 Formal Tests/Retests

The Formal tests were conducted using NAS operational software version 10.31DC for the DCC test on October 8, 1986, and version 10.31CC for the CDC test on October 7, 1986, at the FAA Technical Center. There

were four deviations and two anomalies encountered during the conduct of the DCC test. During the CDC test, four deviations and four anomalies were encountered.

4.4.4.1.1 Summary of DCC Formal Test Conduct

Of the four deviations and two anomalies encountered during the test conduct, only the unexpected switchover that occurred when a PAM 2 error was induced could not be readily identified. The remaining deviations and anomalies were related to a GFE hardware problem, incorrect insertion of induced errors, and the result of coding failures.

The majority of PVD outages resulting from induced errors were 8 seconds or less in duration. There were three PVD outages that were of 12-15 seconds in duration and were related to errors induced in the DCC. An extensive PVD outage of 1 minute 34 seconds occurred when the error was induced at the wrong location. This error was successfully repeated at the correct location.

The hard copy analysis of the printouts indicated minor problems. None of the problems had a significant impact to the test results.

All DART reduction analysis data was compared to Functional test data and any miscompares were sufficiently resolved.

4.4.4.1.2 Summary of CDC Formal Test Conduct

There were four deviations and four anomalies encountered during the test conduct. Since DBUG 52 did not obtain the required data during an unexpected switchover, INFO problem No. 6477 was generated to document this and the correction was verified on November 13, 1986. An incorrect manual entry, incorrect error insertion, and not routing the output to the backup device were the major remaining deviations and anomalies.

Three of the observed PVD outages were 9 seconds or less. The remaining two PVD outages were 1 minute, 47 seconds for a CDC display channel induced error and 9 minutes, 35 seconds during an erroneous fault insertion which was successfully retried.

The hard copy analysis disclosed message not documented in NAS-MD-317, superfluous characters in I/O check report, erroneous data in I/O check report, intervention required sense data has excessive trailing zeroes, table overflow caused monitor messages to be lost/discarded, translate problem with KPR device dependent processor for certain characters, and two start-of-messages output without an intervening end-of-message.

All DART reduction analysis was compared to Functional test data and any miscompares were sufficiently resolved.

4.4.4.2 Regression Tests/Verification Tests

The Regression tests were conducted using NAS operational software version 10.32DB for the DCC test on November 4 and 5, 1986, and version 10.32CB for the CDC test on November 11, 1986, at the FAA Technical Center. Four deviations and one anomaly were encountered during the DCC test conduct. The CDC test conduct encountered only two deviations.

A problem verification test was successfully conducted on November 13, 1986, to verify corrections to problems with rerouting of KVDT and KPR outputs and with use of DEBUG 52.

4.4.4.2.1 Summary of DCC Regression Test

During the test conduct on November 4, 1986, three deviations were encountered: a GFE hardware problem, an 11-second PVD outage that was repeated successfully, and deferral of steps 200 through 210 since an FAA engineer was not available to perform DCC bugs. On November 5, 1986, steps 200 through 210 were performed. During the performance of step 200, an HTM abort occurred. This problem was documented as INFO problem No. 7295. Step 200 was then repeated and performed successfully.

With the exception of three PVD outages, the majority of PVD outages resulting from induced errors were 9 seconds or less. The first exception resulting in a PVD outage of 11 seconds occurred after an induced Applications abort. During the second exception, a 2-minute 9-second outage occurred as a result of an induced DCC display error. The third exception occurred during the first attempt to induce a Display Channel error (step 200), resulting in a 7-minute PVD outage.

No problems were encountered during the hard copy analysis of the printouts and the DART reduction analysis.

4.4.4.2.2 Summary of CDC Regression Test

Two deviations to the procedures were encountered during the CDC Regression test conducted on November 8, 1986. A wrong message entry and skipping of steps 240 through 270 due to INFO problem No. 7374 dealing with rerouting of KVDT and KPR outputs. No anomalies were encountered during the test.

The PVD outages resulting from induced errors were 7 seconds or less.

The hard copy analysis of the printouts indicated; incorrect configuration summary report, NAS-MD-317 conflict regarding assignment of functions to tape, I/O check report against non-existent physical device addresses, table overflow caused monitor messages to be lost/discarded, and incorrect "General Information" messages.

The DART reduction analysis indicated that no problems were encountered.

4.4.4.2.3 Summary of CDC Verification Test

Steps 240 through 270 were skipped during the conduct of the CDC Regression test on November 8, 1986. These steps dealt with KVDT and KPR errors. INFO problem No. 7374 was written to document a problem with the logic using alternate channel/alternate device without trying the primary channel/alternate device first. Code was added to correct this INFO problem for the rerouting of KVDT and KPR outputs.

During the conduct of the CDC Formal test on October 7, 1986, use of DBUG 52 did not obtain the required data during an unexpected switchover. INFO Problem No. 6477 was written to document this. Code was added to correct this problem.

On November 13, 1986, steps 240 through 270 and DBUG 52 were retested using the CDC system and the INFO problem correction was verified as being correctly implemented by a successful test run.

4.5 FAILURE/RECOVERY TESTS

4.5.1 Overview

Unlike Reconfiguration testing, this test was aimed at the ability of the computer subsystem to recover from internal failures. Dependent upon severity of the failure, the computer subsystem failures induced, either caused the system to recover itself by means of a startover or to recover itself by switchover. Further failures were induced without the Support processor available causing the system to continue operation in a degraded mode. Planned manual switchovers were also exercised. All startovers and switchovers were required to occur within a 10 second time frame.

On October 20 and 21, 1986, the Failure/Recovery tests were held. One major problem and various minor problems were documented during these tests. FAA required regression tests were held on November 4, 8, and 13. Verification tests were held on November 18 and 20, 1986, during which all major problems were verified as resolved. All tests demonstrated that the HCS successfully performed startovers or switchovers without loss of Air Traffic Control functions in response to failures other than those tested during the Reconfiguration tests.

4.5.2 Test Description

Failure/Recovery tests were performed on the processor subsystems including the SCMS processors, to verify the capability of the HCS to recover from two types of failures:

- a. Cases in which the primary processor is able to recover automatically. The startover process was tested.
- b. Cases in which the primary processor must be changed. The switchover process was tested.

Specifically, these tests exercised the capability of the HCS to recover from failures other than those tested in Reconfiguration testing, and its ability to perform scheduled switchovers in accordance with section 3.7.3.3 of the Engineering Requirement. Failure Recovery testing included the following tests:

- a. Manual Switchover - Demonstrate suspension, termination, or correct completion of an orderly shutdown of jobs executing in the support processor during an orderly shut down, a switchover of ATC operations from the primary processor to the support processor, and the establishment of the new support processor into the standby mode.
- b. Recoverable Failure in the Primary Processor Subsystem - Demonstrate completion of a correct system startover in response to a recoverable failure in the primary processor within the time requirement specified in section 3.2.1.2 of the Engineering Requirement.
- c. Non-Recoverable Failure in Primary Processor - Demonstrate switchover to the support processor within the specified 10-second time requirement.
- d. Support Processor Failure During a Requested Switchover - Demonstrate that the primary processor correctly resumes normal ATC services within the required time specification during a manually requested switchover of ATC functions from the primary processor to the support processor and a concurrent support processor subsystem failure.
- e. Failure in Support Processor - Demonstrate that failures in the support processor subsystem do not affect the primary processor.

Failure/Recovery tests were conducted while the HCS was executing the Baseline 500 series test scenario. The HCS support processor subsystem executed a minimum of two support tasks and the NAS operational monitor in a standby mode throughout the test conduct.

A full complement of KVDTs, console printers, and line printers were configured to each processor subsystem in accordance with the Engineering Requirement as follows:

<u>Processor</u>	<u>KVDT</u>	<u>KPR</u>	<u>HSP</u>
Primary	12	7	1
Secondary	10	4	1
SCMS	3	1	0

After each startover/switchover, all primary and support peripheral input/output devices were tested to verify that they were interfacing with the proper processor subsystem.

Two system runs were conducted for these tests: one run with the CDC configured system, and the other run with the DCC configured system. The test runs included operator switchover requests and induced hardware failures. The Baseline 500 Functional test scenario was run a minimum of 5 minutes after the occurrence of each switchover request or induced hardware failure.

Data used for on-line and post-test analysis were collected during conduct of the system runs. Data for the post-test reduction and analysis was collected on a SAR using SARC level 4.

4.5.3 Success Criteria/Analysis Method

The on-line test analysis conducted during the test run consisted of a visual inspection of PVDs, the console printer, and the status KVDT. The on-line analysis verified that the HCS responded correctly to the subsystem failures and that the startover and switchover operations were completed within the required time specification. After the test run was complete, and the on-line analysis indicated successful performance, a post-test analysis was conducted. The post-test analysis consisted of a detailed analysis of the SAR generated by the test run and was used to determine when recovery of ATC functions was achieved and the corresponding time interval required to accomplish recovery. The data from running the Baseline 500 Scenario for the Functional test was used as a reference to compare data collected during the failure/recovery tests.

The Failure/Recovery tests were considered successful when the HCS correctly responded to all the Failure/Recovery test cases, and demonstrated that the NAS En Route ATC Service was resumed as specified in section 3.2.1.2 of the Engineering Requirement.

4.5.4 Test Conduct/Results

4.5.4.1 Formal Tests/Retests

The Failure/Recovery Formal tests were conducted with NAS Operational Software releases 10.31CD (CDC version) and 10.31DD (DCC version). The Build included fixes specifically for the Failure/Recovery test; a fix for INFO problem No. 6374 which prevents unsolicited switchovers, and a fix for INFO problem No. 7018 that insured the recovery time of switchovers met the specification of the Engineering Requirement.

4.5.4.1.1 Summary of DCC Formal Test Conduct

The initial formal test of the NAS Operational Software Failure/Recovery test was conducted on the SSF system at the FAA Technical Center on October 20, 1986. All steps of the government approved test procedure were completed.

The test began with a demonstration of the HCS's ability to startup with a reduced set of computer resources. During the DCC initial program load, the DCC reported an element check resulting in the system configured to a single channel. The system was returned to dual channel operation (test deviation). This problem was attributed to the GFE DCC system. The HCS support processor subsystem was initiated with a minimum of two support tasks and NAS standby under VM/MVS. The following startover/switchover test cases were conducted with the indicated recovery times:

<u>Test Case</u>	<u>Recovery Time (sec)</u>
Startover due to memory failure	7
Manual switchover (SWVR)	6
Switchover due to display channel failure	6
Manual switchover with support processor failure	4
Manual switchover with support processor failure prior to switchover complete	14 *
ABORT startover	8
Switchover due to thermal failure	7
Switchover due to memory failure without redundant memory available	6

* RFA 57 allows up to 20 seconds for this type of recovery

After completing the manual switchover with a support processor failure, it was noted that CIOT2 would not accept keyboard entries. Intervention was required to restore CIOT2 and INFO problem No. 7217 was written. Each time NAS standby was IPLed, a ready-to-not-ready interrupt was performed to clear a PROG470 on the system console KVDT (INFO problem No. 7032).

4.5.4.1.2 Summary of CDC Formal Test Conduct

A successful startup with the NAS Operational program running on the primary processor subsystem and NAS standby with two support tasks running under VM/MVS on the support processor subsystem was performed. The first test case, an attempted manual switchover, failed. The displays stopped updating. INFO problem No. 7211 was written. The entire system was reIPLed and the step repeated with no anomalies. The following startover/switchover test cases were conducted with the indicated recovery times:

<u>Test Case</u>	<u>Recovery Time (sec)</u>
Manual switchover (SWVR)	Failed
SWVR repeated	7
Switchover due to Interrupt Handler clobber	8
Manual switchover with support processor failure (reject)	3
Manual switchover with support processor failure prior to switchover complete	15 *
Switchover due to disk channel error	9
Switchover due to MSSF warmstart	7

* RFA 57 allows up to 20 seconds for this type of recovery

With the exception of the manual switchover, all steps of the test procedures were completed satisfactorily. However, two previously reported problems were observed; one relating to the standby KVDT (INFO No. 7032), and the configuration/summary reporting KPR2 configured to controller 260 when it was configured to controller 280 (INFO No. 7135). Deviations were performed to work around these problems without a significant impact to the test.

4.5.4.1.3 Analysis of Formal Test Conduct

Of the 61 Engineering Requirements allocated to the Failure/Recovery test by the Master Test Plan (CDRL B070), 56 were successfully demonstrated. The five Engineering Requirements not verified were all related to the INFO problem reports written during the formal test. The Failure/Recovery Formal test was only partially successful considering that a type I-Critical Mission Performance INFO problem (No. 7211) was discovered during the CDC test run on October 21, 1986.

4.5.4.2 Regression Tests/Verification Tests

The formal test runs were the initial tests using the government approved test procedures to verify the performance of the Operational Software Failure/Recovery capabilities. The regression test runs using the same test procedures were to demonstrate solutions to problems and to verify that the performances of the Failure/Recovery capabilities were not degraded by the solutions to problems. Additionally, two ECRs were tested during the DCC regression test runs: ECR020 Mandatory Switchover and ECR021 Manual Intervention Startover. Testing was accomplished using additions to the DCC test procedure.

The DCC regression test run of November 4, 1986, failed and was rerun on November 13, 1986, after the problem was resolved and sourced patches were applied to the NAS Operational Program.

Following the Regression test runs, verification of solutions to INFO problem No. 6373 (DBS Abort) and INFO problem No. 7275 (all zero matrix) were performed on November 18 and 20, 1986, respectively.

4.5.4.2.1 Summary of DCC Regression Test No. 1

The DCC Regression test run of November 4, 1986, was performed using NAS Operational Software release 10.32DB. The following test cases were conducted with the indicated recovery times:

<u>Test Case</u>	<u>Recovery Time (sec)</u>
Startover due to memory failure	7
Manual switchover (SWVR)	6
Mandatory Switchover (MSVR)	5
Switchover due to display channel failure	5
Manual switchover with support processor failure	4
Manual switchover with support processor failure prior to switchover complete	13 *
ABORT startover	8
Switchover due to thermal failure	FAILED
Switchover due to thermal failure repeated	7
Switchover due to memory failure without redundant memory available	6
Switchover due to thermal failure repeated	6

* RFA 57 allows up to 20 seconds for this type of recovery

After the switchover due to an induced display channel error, PAM 1 went to inactive status instead of redundant. INFO problem No. 7291 was written. When the power/thermal error was induced in the primary processor, the PVDs stopped updating after the system switched to the new primary processor. NAS went into a wait state and entries at CIOT1 were not accepted. The system was IPLed and the step was repeated with no anomalies and a recovery time of 7 seconds. INFO problem No. 7290 was written.

At the conclusion of the test, prior to plant shutdown, the system was reconfigured and the power/thermal failure was repeated with no anomalies.

4.5.4.2.2 Summary of CDC Regression Test No. 1

The CDC Regression test run of November 8, 1986, was performed using NAS Operational Software release 10.32CB.

All steps of the government approved test procedure were completed. The procedure used was the exact procedure used during the CDC Formal test run. The following test cases were conducted with the indicated recovery times:

<u>Test Case</u>	<u>Recovery Time (sec)</u>
Manual Switchover (SWVR)	9
Switchover due to Interrupt Handle clobber	8
Manual switchover with support processor failure (reject)	4
Manual switchover with support processor failure prior to switchover complete	15 *
Switchover due to disk channel error	9
Switchover due to MSSF warmstart	8

* RFA 57 allows up to 20 seconds for this type of recovery

All steps of the procedure completed as expected. No INFO problem reports were written. After the MSSF warmstart switchover, KPR2 was reported to be configured to controller 260 but was actually configured to controller 280 (INFO problem No. 7135). Prior to planned shutdown complete, CDC was inadvertently turned off, causing operator intervention to complete the shut down.

4.5.4.2.3 Summary of DCC Regression Test No. 2

The DCC Regression test was rerun on November 13, 1986, using NAS Operational Software release 10.32DC. This version included a fix for INFO problem No. 7290 (new primary failed after SWVR) discovered during the DCC Regression test run of November 4, 1986. The FAA deemed it necessary to rerun the entire test. The following test cases were conducted with the indicated recovery times:

<u>Test Case</u>	<u>Recovery Time (sec)</u>
Startover due to memory failure	8
Manual switchover (SWVR)	5
Switchover due to display channel failure	18
Manual switchover with support processor failure	4
Manual switchover with support processor failure prior to switchover complete	13 *
ABORT startover	8
Switchover due to memory failure without redundant memory available.	5
Switchover due to thermal failure	6

* RFA 57 allows up to 20 seconds for this type of recovery

An induced display channel error causing a switchover, required 18 seconds to restore the air traffic functions on the new primary processor. At this time, the government test witnesses halted the test until IBM could provide a satisfactory explanation of the 18-second recovery. After a core dump analysis, IBM concluded that following the induced channel error, the start I/O was successful. The channel timeout for the DCC system is fixed at 10 seconds. FAA personnel confirmed that this value was optimized on the 9020 DCC system. After the channel timed out in 10 seconds, the switchover was performed in about 7 seconds. The total outage as viewed on the displays equaled 18 seconds. The explanation satisfied the test witnesses, the system was restored to the configuration prior to the 18-second switchover, and the test case rerun. This switchover was performed in 6 seconds.

Intervention was required to switch some devices to the primary processor following the switchover. This is INFO problem No. 7141.

Due to the delay caused by the analysis of the 18-second switchover, the optimum SIM time to perform INFO problem No. 7290 verification had passed. This step was skipped, the test run was completed, and then the scenario restarted and the step was executed successfully. However, 1 minute after the 6-second switchover, a DBS ABORT occurred causing an additional 8 seconds of display loss. This is known INFO problem No. 6373.

4.5.4.2.4 Verification of Solutions for INFO Problem Reports

On November 18, 1986, using NAS Operational Software version 10.32DD, IBM successfully demonstrated the solution to INFO problem No. 6373 (DBS ABORT). Steps from the approved test procedures were used.

On November 20, 1986, using NAS Operational Software version 10.32CD, IBM successfully demonstrated the solution to INFO problem No. 7275 (all zero matrix on 3814 switch). A special procedure was developed since this problem could not be reproduced using the approved test procedure.

4.5.4.2.5 Analysis of Regression/Verification Testing

All 61 Engineering Requirements allocated to the Failure/Recovery test by the Master Test Plan (CDRL B070) were successfully demonstrated. All type 1 INFO problem reports written against the Failure/Recovery test were resolved and verified. The following INFO problem reports written against the Failure/Recovery test were unresolved as of November 21, 1986:

<u>INFO Problem No.</u>	<u>Problem Class</u>	<u>INFO Abstract</u>
7141	II	Devices lost on SWVR until interrupt
7217	II	CIOT2 not initiated after SWVR
7291	II	PAM 1 went to "I" status after SWVR

4.6 LIVE RADAR TESTS

4.6.1 Overview

Live Radar testing utilized radar sites adapted to the Technical Center facility to acquire and process radar returns from target-of-opportunity aircraft and a planned target track generated by an aircraft supplied by the government and flown in accordance to a specified flight plan. The Technical Center ARTS III facility was interfaced to realistically furnish hand-off actions in both directions, to/from the HCS. During the test, a switchover from the Primary to the Support processor was induced to ensure no impact in a live situation.

Live Radar tests were held on September 15 and 17, 1986, without any major problem. These tests successfully demonstrated that the HCS could properly execute the NAS operational system utilizing live radar inputs in an operational environment.

4.6.2 Test Description

This test demonstrated the ability of the HOST Computer System, while executing the NAS Operational Software, to process real-time (live) inputs from actual radar sites to track aircraft, to transmit/receive real-time interfacility messages to/from an ARTS III facility, and to process manual inputs from and outputs to actual hardware devices interfaced with the HCS. The test was conducted using the full complement of HCS hardware. The test was conducted once with the HCS connected to the CDC and once with the HCS connected to the DCC. During each test the HCS was interfaced with the available multiple long-range radar sites connected to the FAA Technical Center and with an ARTS III test site located at the FAA Technical Center. The Universal Data Set (UDS) adaptation contained in the HCS included this ARTS III. The ARTS III was executing a software version that was compatible with the operational software running in the HCS and was tracking some of the same live targets-of-opportunity as the HCS. In addition, a controlled aircraft supplied by the government was used for the test. The aircraft flew in accordance with a government supplied flight plan, was tracked by the HCS, and was monitored at a control sector. A minimum of four control sectors (D- and R-controller positions) were used during the test.

Each test was run for more than 2 hours. Targets-of-opportunity were tracked in the HCS. Tracks were initiated manually and automatically through the input of flight plan data. Tracks were maintained on discrete beacon, non-discrete beacon (Mode C and non-Mode C), and primary radar trails. The tracks included straight and level flights and altitude transitions. The Mode C tracks were distributed in altitude. The tracks were distributed in the radar coverage such that the tracks occurred in preferred coverage of each radar site. Tracks were handed off between the HCS and the ARTS III in both directions. The Track Record (RT) action was taken for a subset of the tracks initiated.

Input actions were entered manually from the following devices:

- a. Computer Entry Devices (CED): the alphanumeric keyboard and the quick action keys at the D- and A-controller positions
- b. Data Entry Controls (DEC): the alphanumeric keyboard, trackball, quick action keys, and category/function controls on the R-controller's console
- c. Keyboard Video Display Terminals

At a minimum, at least one message of each of the following types were entered during the test:

- a. Flight Data Messages
 1. Flight Plan (FP)

2. Amendment (AM)
 3. Assigned Altitude (QZ)
 4. Code Modification (QB)
 5. Discrete Code Request (DQ)
 6. Qualifier Modification (QB)
 7. Reported Altitude (QR)
- b. Track Control Actions
1. Accept Handoff (QN, QZ)
 2. Coast Track (QT)
 3. Drop Track Only (QX)
 4. Initiate Handoff (QN, QZ)
 5. Track (QT)
- c. Display Control Actions
1. Code Delete (QB)
 2. Code Insert (QB)
 3. Data Block Offset (QN, QZ)
 4. Forced Data Block (QN, QZ)
 5. Point Out (QP)
 6. Request/Suppress Data Block (QP)
 7. Modify Altitude Limits (QD)
- d. Information Request Messages
1. Flight Plan Readout Request (FR)
 2. Radar Coverage Control Site Status Request (YR)
 3. Radar Site Status/Summary Request (ZS)
 4. Range Bearing Readout (LA)

5. Range/Bearing/Fix Readout (LB)
6. Registration/Collimation Analysis Status Report (ZR)
7. Trackball Coordinates Readout (KB)
8. Track Recording Status Report (RP)
9. QP 3 (AALO)

e. Supervisory Messages

1. Change Parameter (CP)
2. Conflict Alert On-Off (CA)
3. Conflict Alert Status Request (RK)
4. E-MSAW Control (E)
5. E-MSAW Status Request (ER)
6. Printout Routing Control (PC)
7. Radar/Beacon Parameter Modification (ZM)
8. Radar Coverage Mode Control (MY)
9. Radar Coverage Site Operational Acceptability (YS)
10. Radar Data Counts Request (ZC)
11. Radar Site Test Message Report (ZT)
12. Track Recording (RT)

The above messages were entered from multiple devices simultaneously. Ten percent of the messages, each of a different type, were entered with format and/or content errors in addition to being entered correctly.

While there were a minimum of five tracks active at each of a minimum of four radar display positions, a switchover to transfer ATC processing from the primary to the support processor was executed. A minimum of two representative jobs were executing in the support processor throughout the test. SAR data were collected during the test with a minimum recording level of SARC 4.

4.6.3 Success Criteria/Analysis Method

Verification of correct processing was established via post-test analysis of all data collected during the test, which included: all

hard copy outputs, observer test logs, DART reductions of SAR data (e.g., LOG, TRACK, HISTORY), and data collected to verify correct radar data processing. Analysis areas included:

- a. Responses to inputs
- b. Outputs (format and contents) at all devices
- c. Processing of surveillance data received from multiple radar sites (including input processing, coordinate conversion, and selective rejection)
- d. Track/Datum Correlation for each track class
- e. Automatic tracking functions
- f. Processing of automated alerts (E-MSAW and Conflict Alert), if they occurred during the test
- g. Processing after a switchover

The Live Radar test was considered complete and satisfactory after the test was conducted with no aborts and all analyses verified correct operation of the HCS. All discrepancies were fully explained and documented. The specific explanation and proof provided were approved by the government prior to having the test considered satisfactory.

4.6.4 Test Conduct/Results

The Live Radar test was run once with the DCC and once with the CDC. The HOST test with the DCC ran on September 15, 1986, using operational software version H10.31DB. As part of the planned test procedure, a Bulk Store Create was executed to provide a real time (Universal Coordinate Time) flight data base for en route sectors. At the beginning of the test, the Riverhead radar site failed due to an open telephone circuit between the site and the FAA Technical Center. Since the radar data supplied by the Trevoise site would satisfy the test requirements, the test was continued. A Bulk Store Create was executed to compensate for the test delay by providing a flight data base with current real times. Test personnel initiated tracks on targets of opportunity and executed the test procedures. The support system was processing 2 support jobs throughout the test. The HOST ran the entire 2 hours with no aborts. Observers reported that track initiation, track maintenance and display outputs operated correctly. Handoff/accept actions, beacon, altitude and route amendments, and display control actions were used. Tracking included discrete beacon, non-discrete beacon, and primary data. As required by the formal test procedures, a specific track load was established at each PVD, and switchover was executed.

Flight Plan and Track data on the FAA-supplied controlled aircraft were successfully transferred to and from the ARTS III facility via the PAM interfacility adapters. Throughout its flight, the controlled aircraft track was monitored and handed off between operational

sectors. Minor anomalies were observed related to displayed Mode C and the adapted climb/descent rate for the aircraft type used. It was concluded that the anomalies were not HOST problems. The time display on the PVDs indicated a loss of 5 seconds during switchover which satisfied the test requirement.

Throughout the test, PVDs and the HSP contained data from EMSAW and CA processing. The on-line outputs were visibly scanned by observers to determine if significant problems occurred. None were noted.

As part of the formal test procedures, sector position operators initiated random tracks to increase the load to 200, and the operators initiated Halo displays to verify that the specified maximum (90) could be obtained. Both of these activities were successful.

To guarantee that two support jobs would always be running in the support processor, three support jobs were continuously submitted. DART, REMON, and SIM jobs were queued and executed until the switchover when the support processor became primary. The on-line monitor indicated that support system utilization was continuously high, often exceeding 85 percent as the support jobs made use of the resources. A planned shutdown was successfully executed to terminate the test.

In general, no significant HOST problems were reported. The on-line outputs were scanned to determine if significant problems occurred which were not otherwise noted. None were detected.

The test with the CDC ran on September 17, 1986, using operational software version H10.31CB. As part of the planned test procedure, a Bulk Store Create was executed to provide a real time (Universal Coordinate Time) flight data base for en route sectors. Shortly after HOST initialization, the Riverhead radar site failed due to a hardware problem at the surveillance site, and delayed the test. Since the radar data supplied by the Trevoise site would satisfy the test requirements, the test was continued. A Bulk Store Create was executed to provide a flight data base with current real times. Test procedure execution was intentionally delayed for an additional 15 minutes in consideration of the time required for a Bulk Create in the 9020 replay. After the delay, test personnel operated the en route sector positions in the ESSF, initiated tracks on targets of opportunity, and executed the test procedures. After 23 minutes, data from the Riverhead site appeared usable, and a YS ON message was entered to instruct the system to use the data. The support system was processing two support jobs throughout the test. The HOST ran the entire 2 hours with no aborts.

The CDC run repeated the events of the prior DCC run. Targets of opportunity were tracked along with the FAA supplied controlled aircraft. Minor correlation errors occurred. Mode C discrepancies were rated as in the DCC run. None of the anomalies were HOST problems. The planned switchover required 8 seconds. EMSAW and CA outputs were considered reasonable. Both the 200 track load and the 90 Halo test were successful. Three support jobs were continuously

submitted on the support processor. An error occurred related to the support system conversational monitor that had no impact on this test. Planned shutdown was successful.

Since indepth data analysis was performed for other AP tests, comparative analysis of the Live Radar test was limited to subsets of the reduced data. These data were selected for analysis of HOST radar data processing and tracking immediately before and after switchover, controlled aircraft tracking, ARTS III data transfers, and input/output processing.

After acquiring reference data from 9020 replays of the HOST tests, manual data comparisons were performed. The data which were analyzed compared favorably, but some problems were detected and were investigated.

Two problem reports were written against support software (DART). In addition, the data indicated that tracking anomalies occurred for a small number of tracks, and the same kinds of anomalies occurred in the 9020 as well as in the HOST. It was concluded that the problems resulted from limitations in the recording process.

The following conclusions are based upon conduct of the Live Radar test with the CDC and the DCC display systems:

- a. The HOST test satisfied the Engineering Requirements.
- b. The HOST successfully ran with live inputs from actual long range radar sites, an ARTS III system interface, and manual inputs to and outputs from actual hardware positions.
- c. While the use of live interfaces did not present a test requirement to the HOST different from the simulation test mode, the unplanned structure of the operational traffic and the unplanned radar site failure increased confidence that the HOST will operate satisfactorily in the ARTCC.
- d. Some problems were noted and documented as HIPRs.
- e. Although switchovers during the Live Radar test runs were successful, tracking anomalies were detected in the data for some tracks. Similar anomalies occurred during the 9020 runs and appear to result from the limitations inherent with using recovery data for startover.

4.7 ON-LINE CERTIFICATION TESTS

4.7.1 Overview

On-Line Certification (OLC) testing consisted of a re-Hosted capability used throughout the NAS to certify that systems are operationally sound. OLC encompasses verification processes in eight

areas including flight data processing, input message processing, reconfiguration, and a variety of radar performance and quality tests.

On-Line Certification tests were held on September 23 and 30, 1986. An FAA required retest was successfully held on October 10, 1986, to retest discrepancies observed previously. All tests verified that the HCS could execute the NAS operational program while performing On-Line Certification of the NAS hardware and software.

4.7.2 Test Description

The hosted On-Line Certification (OLC) Program was tested using an OLC scenario input and a test case output against which the test results were compared. The OLC functions tested included the following:

- a. Test Area 1 - OLD Input Messages
- b. Test Area 2 - Flight Data Processing
- c. Test Area 3 - Radar Performance Monitoring
- d. Test Area 4 - Real Time Quality Control
- e. Test Area 5 - Quick Analysis of Radar Site
- f. Test Area 6 - Radar Processing and Tracking
- g. Test Area 7 - Reconfiguration
- h. Test Area 8 - Live Radar Analysis

All testing was accomplished using the HOST 10.31DB (DCC) or 10.31CB (CDC) software.

4.7.3 Success Criteria/Analysis Method

The objective of this test was to verify that the HOST Computer System could execute the NAS software while performing On-Line Certification testing of the NAS hardware and software. This was determined by executing a series of certification simulation files and entering manual input messages to exercise all functions of On-Line Certification applicable to the HOST Computer System. Responses to these predefined scenarios were evaluated for timeliness and accuracy. The testing required interfacing with both the DCC and CDC display systems.

Successful completion of any given test area was determined primarily through observing responses at the SEIOT (KPR4) and hardcopy output at the MSP. Additional outputs reflecting critical responses to the OLC test scenario were observed at the HSP and the sector 3 PVD.

While an immediate evaluation could be made of most inputs during testing, an analysis of all the hardcopy outputs from each test was

made to determine if there were any undetected anomalies. This was accomplished by performing a detailed analysis of all hardcopy output for each of the test runs. The hardcopy was reviewed for correct responses to inputs and matched with 9020 hardcopy comparison data of equivalent processing.

4.7.4 Test Conduct/Results

Testing began on September 23, 1986, with the CDC portion of the test plan being performed first. This testing consisted of test area 5, QARS, and that portion of test area 7, reconfiguration applicable to the CDC. With this portion of the testing completed, the HCS was brought down and reconfigured for the DCC display system.

Testing on the HCS with the DCC began with test area 1, Validation of OLD input messages, and continued with test area 2, Flight Data Processing I/O, and test area 3, Radar Performance Monitoring. Because of electrical storms in the local area, testing had to be terminated for the night due to several interruptions causing a loss of both the PAMs and the DCC. Testing would be continued at a later date without the need for retesting any already completed test.

There was only one major discrepancy considered detrimental to the success of the test observed during this portion of the testing, an RDA abort which was later determined to have been caused by a lightning hit.

On September 30, 1986, testing was continued with test area 4, Real Time Quality Control. Without any further interruptions, the remaining test areas, test area 5, Quick analysis of radar site (QARS), test area 6, Radar processing and tracking, the remainder of test area 7, Reconfiguration, and test area 8, Live radar analysis were completed. During this portion of the testing, two discrepancies were observed that required retesting.

For those areas which were not completed satisfactorily, additional testing was performed on October 10, 1986. This test was completed successfully with no outstanding discrepancies.

4.8 FAA TECHNICAL CENTER SYSTEM ACCEPTANCE TESTS

4.8.1 Overview

This was the final Acceptance test performed at the FAA Technical Center irrespective of Regression testing. This test utilized recorded live radar introduced into the system at the Common Digitizer requiring the radar processing functions to be exercised in their entirety. Simulated key strokes coordinated with the live radar tracks together with manual inputs from the PVDs for selected tracks were used to initiate and control the targets. Adjacent site interactions were simulated in accordance to the radar driver scenario. To complete the HCS test activity, Dynamic Simulation, an on-line training vehicle was exercised during this test.

FAATC Acceptance tests were successfully held on October 27 and 28, 1986. Regression acceptance tests using an updated version of the HCS software were successfully held on November 8 and 10. These tests verified the capability of the HCS to execute the NAS operational system using recorded live radar and manual inputs.

4.8.2 Test Description

The Contractor conducted a system acceptance test at the FAA Technical Center. The test was conducted after completion of all the other FAA Technical Center tests as specified in sections 4.2.1, 4.2.2, and 4.2.3 of the Engineering Requirement. The Recorded Live Radar test was used as the FAA Technical Center System Acceptance test to verify the correct operation of the converted NAS operational software with recorded live data inputs and live manual actions. The test exercised the hardware interfaces and associated software used to process live radar data and manual input actions.

4.8.3 Success Criteria/Analysis Method

The government provided the test inputs necessary to conduct the FAA Technical Center System Acceptance test. The test was conducted and the test data analyzed as described in the latest revision of MTR-83T3-01, "HOST Computer System Test With Recorded Live Radar Data, Volumes I, II, and III."

The FAA Technical Center System Acceptance test was considered complete and satisfactory after the HCS data analysis outputs were compared with the 9020 computer system outputs, and found to be equivalent or within tolerances provided in GFE Recorded Live Radar Documentation - Analysis Data. Any non-comparisons between HCS data and 9020 computer data and other discrepancies were fully explained. The specific explanation and proof provided was approved by the government prior to having the test considered satisfactory. Moreover, the test was run again to demonstrate proper functional operation.

The following analysis data and techniques were used for the FAA Technical Center System Acceptance test:

- a. On-Line Printouts - All on-line printouts were used for analysis.
- b. Observer Logs - Visual observations recorded on observer logs were compared with the expected results listed in the test script. Deviations were further analyzed and reconciled.
- c. DARC Data - The verification of DARC flight plan readout was accomplished by comparison with the reference data contained in MITRE document MTR 83T3-03, as modified by MITRE letter W105-0022.

d. DART Reduction - Data recorded on the SAR tapes were processed using DART options such as HISTORY, TRACK, FLIGHT, LOG, IOSUMMARY. These DART reports were used to verify:

1. Radar Data Processing
2. Flight Data Processing
3. Automatic Tracking
4. Input and Output Message Processing
5. Subsystem Interfacing

Some of the analyses were modified because of GFE PTRs associated with DART.

4.8.4 Test Conduct/Results

A formal test and a regression test was conducted for each display channel (DCC and CDC) resulting in four tests being conducted.

The overall assessment of the FAA Technical Center System Acceptance test is that it was successful. None of the anomalies reported had an adverse impact on the success of the test or the validity of the test data.

4.8.4.1 Formal Tests/Retests

The formal tests were conducted using NAS operational software DCC version 10.31DD on October 28, 1986, and CDC version 10.31CD on October 27, 1986. No deviations to the test procedures were noted and the test cases were run in accordance with the approved redline procedures. As a result of data analysis, eight problems were identified (28-01 through 28-08). Two of these problems generated an INFO problem report (INFO No. 7289 and No. 7804). In addition, IBM's post-test analysis uncovered a problem with erratic altitude information (INFO Problem No. 7834) that was determined to be GFE.

4.8.4.1.1 Summary of DCC Formal Test Conduct

During the test conduct, one minor problem was noted with a paper jam in KPR6 causing the output to be routed to the backup KPR4. The problem had no effect on the test and demonstrated the proper reassignment from the primary device to the backup device.

The highlights of the test were:

- a. Planned startover at SIM time 1427 took 7 1/2 seconds.
- b. Flight tracking resumed approximately 1 minute and 8 seconds following the switchover.
- c. Planned switchover at SIM time 1421 took 6 seconds.
- d. Planned shutdown at SIM time 1430 took 1 minute.

Analysis of the on-line printouts indicated that no significant anomalies were noted. However, DART reduction of the SAR tapes noted three problems (28-01 through 28-03). A summary of the three problems and their resolutions is as follows:

- 28-01 Radar data counts percentages were different between HCS and 9020. This was determined to be a GFE problem with the 9020 comparison data.
- 28-02 DART IOSUMMARY did not provide a breakdown for KVDT and IOT outputs. This is a DART problem documented as INFO problem No. 7289 which has since been fixed by IBM.
- 28-03 DART log flight plan updates were missing the uniform time update information. Timing differences between the Bell and Howell VR-3700 radar playback and the HCS simulation tape were determined to be the cause.

4.8.4.1.2 Summary of CDC Formal Test Conduct

The CDC test run used scripted manual input messages entered by the IBM test team. During the test, an anomaly resulting in two CDC equipment reconfigurations was caused by a problem in the CDC and was considered to be a minor problem.

The highlights of the test were:

- a. CDC equipment reconfiguration at SIM time 1337 and 1343
- b. Planned startover at SIM time 1417 took 8 seconds
- c. Planned switchover at SIM time 1421 took 7 seconds
- d. Planned shutdown at SIM time 1430 took 2 minutes

Analysis of the on-line printouts indicated that no significant anomalies were noted. DART reduction of the SAR tapes noted five

problems (28-04 through 28-08). A summary of the five problems and their resolutions is as follows:

- 28-04 I/O check reports for CDC channel errors were output on the HSP and MSP. This was caused by a CDC hardware problem that was recreated during a 9020 test run.
- 28-05 Conflict Alert pair contains incorrect speed and heading. This is a GFE problem documented as INFO problem No. 7804.
- 28-06 Beacon and primary was not correlated when using DART HISTORY for one AID. Two distinct radar messages were received at SIM time 133641 and was not considered to be a system problem.
- 28-07 CTA miscompare when using DART flight option. This was due to SAR data loss when a planned switchover and startover occurred on the HCS. This analysis was considered successful.
- 28-08 Altitude update missing when using DART log option. Late manual entry occurred because CDC had completed an unexpected reconstitution.

4.8.4.2 Regression Tests/Verification Tests

The regression tests were conducted using NAS operational software DCC version 10.32DB on November 10, 1986, and CDC version 10.32CB on November 8, 1986. An IR (11166873) and a problem report (28R-01) was written as a result of problems encountered during an unexpected DCC abort. The remaining problems encountered during data analysis were previously documented in the formal test runs.

4.8.4.2.1 Summary of DCC Regression Test Conduct

An unexpected DCC abort was encountered during a planned switchover and resulted in loss of PVD data for 1 minute and 9 seconds. The attempt to dump core data failed and a DRG3 was lost. A problem report and an IR were written about this. Unnecessary disk files were deleted due to lack of disk space during support job execution.

The highlights of the test were:

- a. Planned startover at SIM time 1417 took 6 1/2 seconds
- b. Planned switchover at SIM time 1421 took 1 minute, 9 seconds as a result of the DCC abort
- c. Planned shutdown at SIM time 1430 took 2 minutes.

DART reduction of the SAR tapes confirmed the three problems encountered during Formal DCC test (28-01 through 28-03). In addition, a problem report (28R-01) was generated. A summary of the problem and its resolution is as follows:

28R-01 The transfer of core dump data from the DCC to HCS failed. Channel contention occurred due to the switchover and DCC abort occurring at the same time. This was determined to be an acceptable condition.

4.8.4.2.2 Summary of CDC Regression Test Conduct

There were no deviations from the scripted manual inputs and no anomalies were observed during the test. Highlights of the test were:

- a. Planned startover at SIM time 1412 took 7 1/2 seconds
- b. Planned switchover at SIM time 1421 took 9 1/2 seconds
- c. Planned shutdown at SIM time 1430 took 2 minutes

No additional problem reports were written. Those problems encountered during data analysis were previously documented during the Formal CDC test (28-04 through 28-08).

5 SUMMARY

Testing of the identified 26 test areas culminated in a total of 79 formal tests being run including 12 Regression Tests. All hardware tests except Performance Testing were repeated for each of the three systems; SSF, CS/SD and RMA installed at the Technical Center. All tests requiring display laboratories were conducted twice, once for checkout on the Computer Display Channel (CDC) System and once on the Display Channel Complex (DCC) System. Capacity and Response Time testing alone was comprised of 24 tests, 12 for each display suite. The 12 Regression Tests were conducted to assure that the fixes for the many problems identified and resolved throughout the test period did not create additional problems. In addition, as indicated in Tables 1, 2 and 4, frequent retests were required before a test area was accepted as complete. Retest requirements depended on the criticality of problems that surfaced during initial testing. These requirements determined whether a test was rerun in its entirety or whether specified areas were rerun to verify problem report fixes.

Extensive data reduction and analysis was performed to thoroughly evaluate test results. A cross-section of technical expertise thoroughly reviewed the data. As previously indicated in Sections 2 and 3, many problem reports were written and retests made as a result of this in-depth analysis. Technical experts from all NAS En Route organizations contributed to this evaluation.

In summary, the total HOST test program at the FAA Technical Center was considered a total success. The system was extensively tested in a test bed environment. Some risk remained when the HCS was implemented at 20 ARTCC's since there are no two centers that are identical, either in amount of equipment or environment. However, further confidence in the success of this program has resulted from the successful implementation of the HCS, which occurred during the production of this report, at the initial six centers to receive the system. It is currently controlling air traffic in the Seattle, Houston, Denver, Boston, Washington, and Chicago areas, totally replacing the antiquated 9020 Central Computer Complex.

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National Airspace System Plan for Facilities, Equipment, and Associated Development, FAA, Washington, DC, April 1985. .

ACRONYMS

AMP	Aircraft Management Program
AP	Acquisition Phase
ASB	Automated System Build
ATC	Air Traffic Control
CA	Conflict Alert
CCC	Central Computer Complex
CCR	Configuration Control Register
CDC	Computer Display Channel
CED	Computer Entry Device
CMS	Conversational Monitor System
COMPOOL	COMMON POOL
CP	Change Parameter
CPU	Central Processing Unit
CRD	Computer Readout Display
CS/SD	Central Support/Software Development
DART	Data Analysis and Reduction Tool
DAS	Direct Access Storage
DASD	Direct Access Storage Subsystem
DCC	Display Channel Complex
DCP	Design Competition Phase
DEC	Data Entry Control
DLOG	Data Log
ECR	Engineering Change Request
EMC/EMI	Electromagnetic Compatibility/Electromagnetic Interference
EMSAW	En Route Minimum Safe Altitude Warning

ER	Engineering Requirement
ERM	En Route Metering
ESI	Electrostatic Interference
FDB	Full Data Block
FP	Flight Plan
GFE	Government Furnished Equipment
HCS	HOST Computer System
HIPR	HOST Interim Problem Report
HRT	High Resolution Timer
HSP	High Speed Printer
I/O	Input/Output
IPAT	Interface Path Analysis Tester
IPL	Initial Program Load
KPR	Keyboard Printers
KVDT	Keyboard Video Display Terminal
MDM	Maintenance Diagnostic Monitor
MIPS	Million Instructions Per Second
MSP	Medium Speed Printer
MSSF	Monitoring and System Support Facility
MVS	Multiple Virtual Systems
NAS	National Airspace System
NST	New System Test
OLC	On-Line Certification
OLTS	On-line Test System
OLTSEP	On-line Test Stand-alone Executive Program
PAM	Peripheral Adapter Module
QARS	Quick Analysis of Radar Site

QRO	Quality Reliability Officer
REMON	Resource Monitoring
RFA	Request For Action
RIN	Radar Input Processing Subprogram
RMA	Reliability, Maintainability, Availability
RSCS	Remote Spooling Communication System
RTT	Response Time Tool
SAR	System Analysis Recording
SCMS	System Control and Maintenance Support
SDR	SIM Driver
SMART	System Monitor Analysis Real Time
SMI	System Measurement Instrument
SSF	System Support Facility
TAR	Timing Analysis Recording
TDB	Table Data Build
UDS	Universal Data Set
VM	Virtual Machine
VMCP	Virtual Machine Control Program



APPENDIX A

The following personnel have contributed to the successful HOST Test Program. Many were not included in the formal HOST acceptance testing but participated in Failure Mode tests, Site Simulation tests, and HOST Verification tests at the FAA Technical Center. Problems found during these tests had a profound impact on the development of the system and its eventual acceptance in the formal test program described in this report. The depth of testing could not have been accomplished without the dedication and knowledge of each individual.

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EMMONS, ROBERT	RMS	FAA TECHNICAL CENTER
EVANS, THERESA	RMS	FAA TECHNICAL CENTER
GOLAS, WAYNE	RMS	FAA TECHNICAL CENTER
HAYES, FRAN	RMS	FAA TECHNICAL CENTER
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SMITH, MARK	RMS	FAA TECHNICAL CENTER
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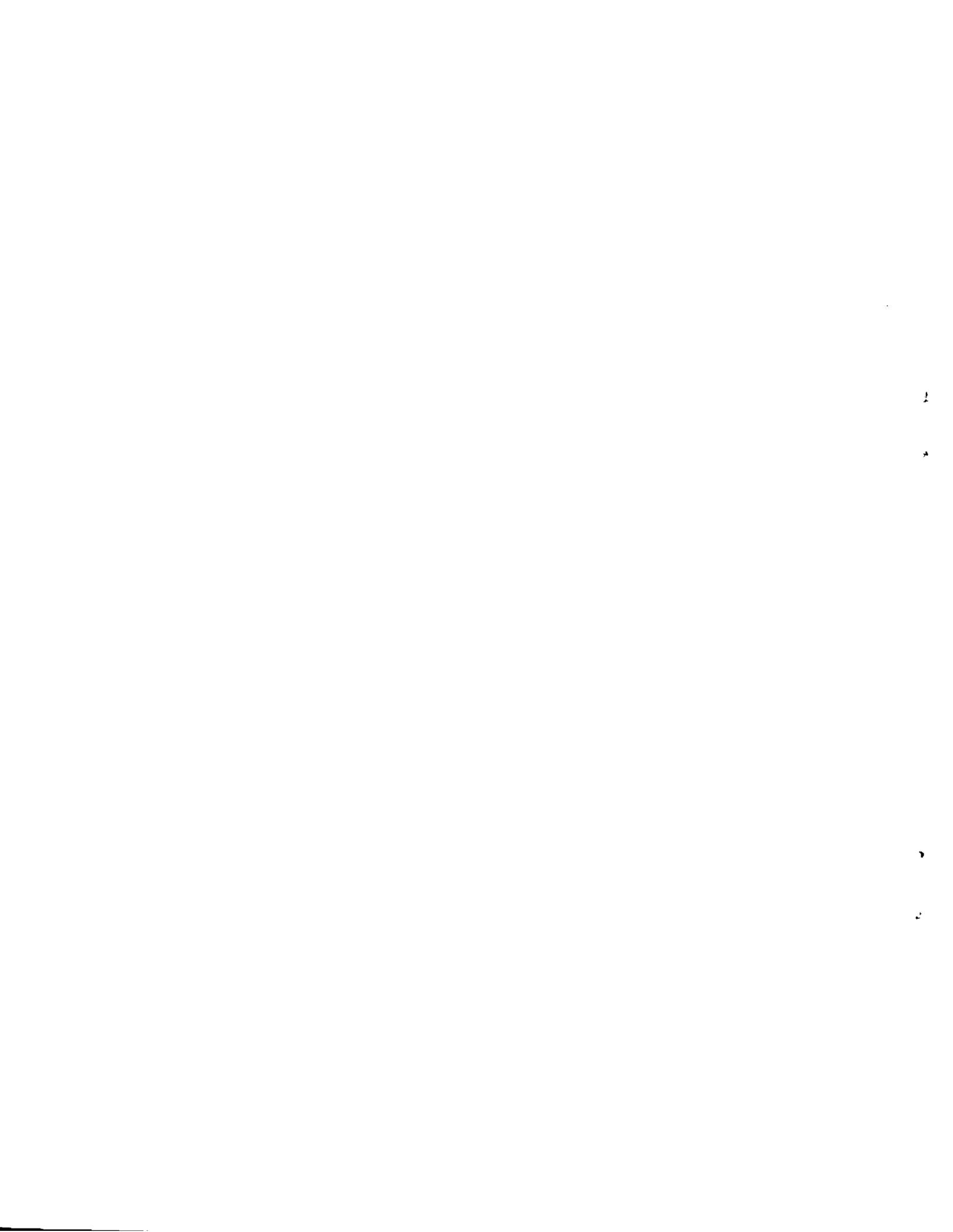
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GLOVER, JACK	AT	CHICAGO ARTCC
GUBA, GERALD	AT	CLEVELAND ARTCC
HANCOCK, JON	AT	OAKLAND ARTCC
HARRISON, CHARLES	ATR-330	FAA WASHINGTON HQTRS
HENKLE, GREGG	AT	INDIANAPOLIS ARTCC
HEVELONE, JAMES	AT	CLEVELAND ARTCC
HIGHSMITH, THERESE	AT	SEATTLE ARTCC
HILL, BOB	AT	
HOSIC, DELBERT	AT	JACKSONVILLE ARTCC
HOWARD, KEN	AT	ALBUQUERQUE ARTCC
JOHNSON, ROBERT	AT	ALBUQUERQUE ARTCC

JONES, MIKE	AT	INDIANAPOLIS ARTCC
KLEIN, JERRY	AT	ATLANTA ARTCC
KULLAS, LEONARD	AT	SEATTLE ARTCC
LUCOCK, RENAE	AT	DENVER ARTCC
MANNING, LEWIS L.	ATR-210	FAA WASHINGTON HQTRS
MCPHERSON, MIKE	AT	CHICAGO ARTCC
MENTAL LARRY	AT	CLEVELAND ARTCC
MOEHLE, DOUG	AT	MINNEAPOLIS ARTCC
MUSSELLMAN, GERALD D.	AT	FORT WORTH ARTCC
NAUGLE, JOANN	AT	CLEVELAND ARTCC
ROBINSON, NEIL	AT	SALT LAKE CITY ARTCC
ROW, ROGER	AT	SEATTLE ARTCC
RUNNER, GEORGE	AT	CHICAGO ARTCC
SLOAN, JERRY	AT	OAKLAND ARTCC
TAYLOR, BRYAN	AT	SEATTLE ARTCC
ULANCH, ROBERT	AT	WASHINGTON ATRCC
WINN, GARY	AT	SEATTLE ARTCC
WISCHMANN, G.	AT	MINNEAPOLIS ARTCC
WILLIAMS, ROBERT	AT	SEATTLE ARTCC
YOUNG, ROLAND	AT	BOSTON ARTCC
HEADRICK, LEWIS	SEI	FAA WASHINGTON HQTRS
KRASINSKI, FRANK	SEI	FAA WASHINGTON HQTRS
LIBERMAN, GENE	SEI	FAA WASHINGTON HQTRS
MAGEE, JIM	SEI	FAA WASHINGTON HQTRS
MARPLE, RALPH	SEI	FAA WASHINGTON HQTRS
MOREHOUSE, CHUCK	SEI	FAA WASHINGTON HQTRS
PHULL, MOHINDER	SEI	FAA WASHINGTON HQTRS
PORTER, BILL	SEI	FAA WASHINGTON HQTRS
TEDFORD, ANN	SEI	FAA WASHINGTON HQTRS
SELLERS, JOHN	SEI	FAA WASHINGTON HQTRS
BOEGER, ED	AF	KANSAS CITY ARTCC
BRUNER, JAMES	AT	CHICAGO ARTCC
CATALON, FRANK	AF	CHICAGO ARTCC
HOLLAND, BILL	AF	JACKSONVILLE ARTCC
KENNEDY, ALBERT	AF	CHICAGO ARTCC
LIGHT, DENNIS	AF	SEATTLE ARTCC
MARTIN, SANDRA	CO AF	CHICAGO ARTCC
YEPSER, LLOYD	AF	CHICAGO ARTCC
BOUWER, LEE	ACC	ACADEMY
LUNN, JANE	AT	INDIANAPOLIS ARTCC
TODHUNTER, FRED	AT	ATLANTA ARTCC
WEBER, CHARLES	AT	MINNEAPOLIS ARTCC
WHITTAKER, DOYLE	AT	WASHINGTON ARTCC
BOLANDER, CLARENCE	AF	CHICAGO ARTCC
DOLOSIC, JOYCE	CO AF	CHICAGO ARTCC
GUYER, ROSE	CO AF	CHICAGO ARTCC
HOSS, AL	AF	CHICAGO ARTCC
VANBOEKEL, MIKE	AF	CHICAGO ARTCC
KEMP, WILL	AF	CHICAGO ARTCC
MAZUC, PAT	AF	CHICAGO ARTCC
HARTRANFT, HELEN	ATR-560	FAA TECHNICAL CENTER
MYERS, DUANE	AF	ALBUQUERQUE ARTCC
BRANIFF, TOM	AF	LOS ANGELES ARTCC
GRIFFIN, HASKEL	AF	MIAMI ARTCC

SHIPLER, DEL
GARDNER, JOHN
WEBER, NEVILLE
PACKARD, BILL
ROBERTSON, BILL
SEEGERS, JACK
THOMAS, RON
PIECH, RICHARD

AF
AF
ALG
AF
AF
AF
AF
ACT-610

INDIANAPOLIS ARTCC
ALBUQUERQUE ARTCC
FAA WASHINGTON HQTRS
MIAMI ARTCC
FORT WORTH ARTCC
ALBUQUERQUE ARTCC
HOUSTON ARTCC
FAA TECHNICAL CENTER



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