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TACAN/DME DIGITAL DATA BROADCAST DESIGN PLAN

Vol. IV – Ground Equipment

September 1974

Final Report

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16. Abstract

The Digital Data Broadcasting Design Plan implements the system engineering process for the purpose of defining with supporting rationale a recommended ground/airborne equipment configuration and flight test program. This plan documents an approach to verify the operational significance and technical feasibility of utilizing existing DME and TACAN to provide the function of broadcasting data to aircraft for use in support of area navigation in addition to its normal function. The Design Plan is structured as follows in five volumes:

Volume I - Operational Analysis
Volume II - Synthesis of the Data Transmission and Formatting Techniques
Volume III - Airborne Equipment
Volume IV - Ground Equipment
Volume V - Flight Test Program

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4.1 Introduction

This Volume of the DDB Design Plan describes the operation and design of the ground-based Data Generator, its associated programming hardware and the DDB Monitor. The Data Generator and Monitor will be packaged together in a standard equipment rack. The programming hardware will be packaged separately.

The Data Generator will contain all necessary controls, logic circuits and interface circuits to provide pulses to the Transponder for adding digital data to the reply and squitter pairs. The design is based on the Asynchronous Data System Concept (ADS) described in Volume 2. The programming hardware will be used to provide the man-machine interface for performing the data programming functions for the Read-Only Memories which will store the data to be transmitted. The proposed equipment configuration has been selected on the basis of the following desirable system characteristics:

1. Reprogrammable, non-volatile memories.
2. Convenient, versatile programming and reprogramming capability.
3. Equipment simplicity.

The Monitor portion of the equipment will contain all the necessary functions to assure that the DDB equipment is operating properly. This equipment will contain Read-Only Memories which are identical to those used in the Data Generator. The monitor will receive the

actual transmitted RF pulses as its basic input and will decode and synchronize to the word sequence being broadcast. After this synchronization is acheived the monitor will perform a bit-by-bit comparison of each transmitted word and the corresponding word stored in its memory. The design details are presented in Section 4.3.2.

The equipment will be designed in such a manner that either a single or dual installation can be incorporated into each station. Provisions will be made for patching various transfer and control function cables and associated logic circuits to accommodate various single/dual installation options.

The sections which follow describe the overall system concept design details and associated interfaces between each of the DDB ground equipments and the TACAN/DME Transponders and TMC Units.

4.2 Overall Description

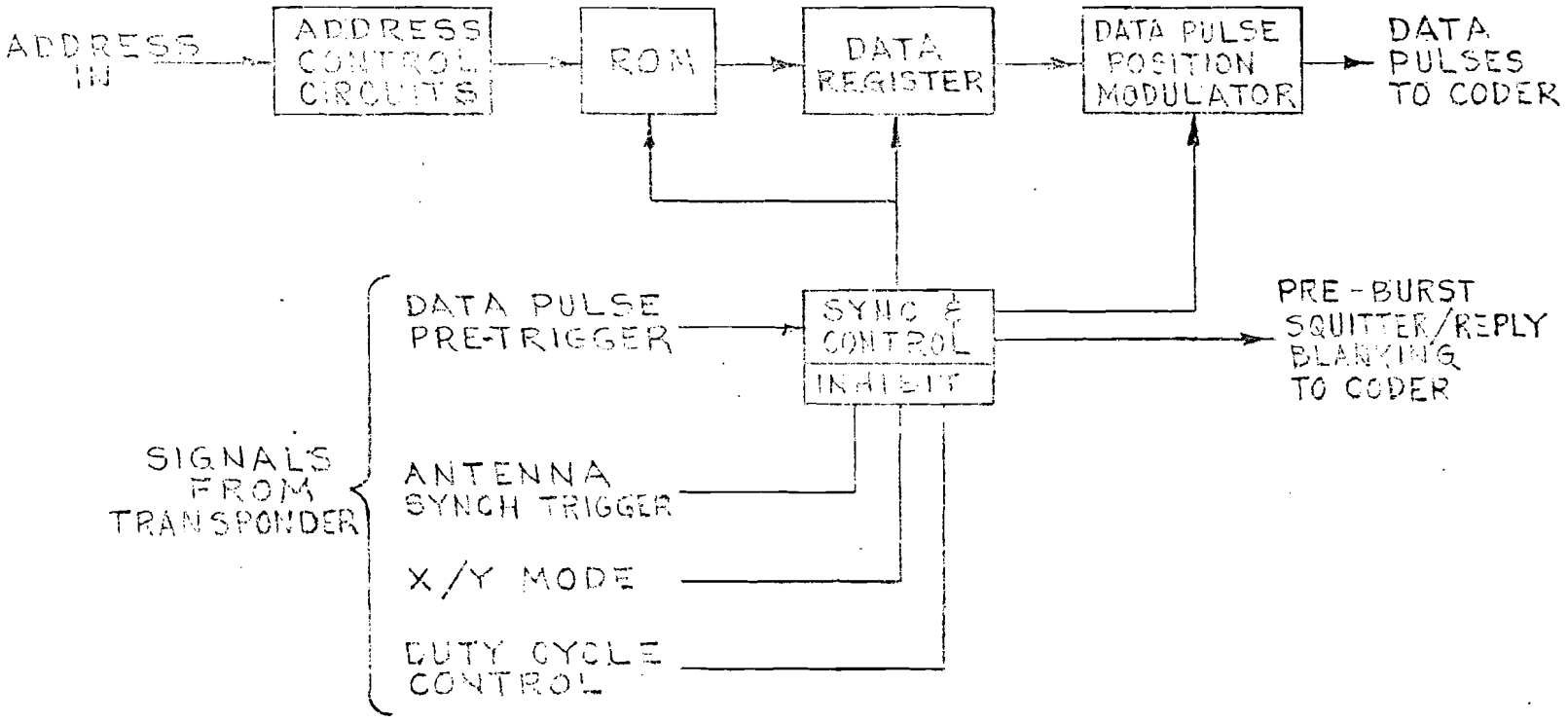
4.2.1 Data Generator

Each Data Generator will be specially programmed to broadcast data for its specific VORTAC station. Each station will be programmed to transmit data in accordance with the required station and waypoint data designated to support the arrival and departure routes for the various traffic flows.

The number of traffic flows and the amount of data required for each flow will determine

the amount of data which must be stored in the Data Generator's memory. The "duty cycle" of the data transmission will be directly related to the data quantity and the required system cycle time. References made throughout the rest of this Volume to "duty cycle control" refer to the control of the duration when no data is added to the squitter or reply pairs between two successive data word groups. (It was indicated in Volume 2 that all words would be either 30 or 24 bits long and each distinct word would be sent twice, in two word groups. At the end of each group the Data Generator will be disabled for a period of time determined by the quantity of data which must be sent, the system cycle time and the Transponder reply rate.)

A simplified block diagram of the Data Generator and its associated input-output interface is shown in Figure 4-1. Four ROM chips are arranged in a 256 word by 32 bit non-volatile reprogrammable unit. (For this application, each data word will occupy less than the 32 bits of storage which are available). Since the worst cast word count for a given flow is 194 words (see Volume 2, page 31) the proposed data memory capacity of 512 words (two ROM units) is sufficient to store enough data for two "worst case" traffic flows. In most stations which require less than 194 words per traffic flow, the number of different flow patterns which can be stored will be proportionately greater. The equipment will be designed in such a manner that memory capacity will be



SIMPLIFIED BLOCK DIAGRAM AND INTERFACE

FIG. 4-1

a variable depending on the particular installation. The organization of the ROM PC cards and the card baskets will allow addition of 256 x 32 bit memory units on the basis of the quantity desired for any particular application. For the purpose of the present Engineering Model design, 512 words of memory will be adequate to demonstrate over all system capability.

The specific stored words which are required for a given flow of traffic are accessed by an appropriate address start and stop code to the address control circuits. For example, if the NE traffic flow was to be used in a given station and the associated data was contained in word positions 157 to 298, the address control limits would simply be set to those two numbers. The address control circuits would thus start sending out word number 157 and continue to 298 and then recycle back to 157. Another flow pattern might be stored in word positions 299 through 376. Whenever the traffic flow is to be changed the address limits would automatically be switched over to the new numbers upon operator command. This can be accomplished locally or through remote operation of the system with the telephone dialing equipment.

The ROM data so accessed is transferred into a shift register upon command from the Synch and Control circuits. Each bit is clocked (by a TACAN/DME Data Pulse Pre-Trigger from the Transponder Coder) into the Pulse Position Modulator which established the appropriate pulse timing for adding data or word synch

pulses to the TACAN/DME pulse pairs. These data and word synch pulses are sent to the Transponder Coder where they are combined with the normal TACAN/DME pairs prior to entering the Transponder Modulator. Inhibit circuits are provided to properly exclude data from being transmitted under various conditions described in Volume 2. A duty cycle control permits manual adjustment of the data "off time" between word groups as previously described.

Detailed descriptions of the operation of the above circuits are presented in Section 4.3.1.

Each ROM will be programmed by means of Teletypewriter, Minicomputer and ROM Interface complex. This will be explained in detail in Section 4.4. Whenever a program change is required for a given station, a spare ROM will be programmed and substituted for an existing unit. The original memory can then be reprogrammed as a spare or simply retained for future program changes.

4.2.2 Test Monitor Control (TMC)

The purpose of the data broadcast TMC equipment is to provide failsafe monitoring and testing of the operations of both dual and single digital data broadcast installations. The existing TMC equipments are provided with a rack of accurate test equipment including counters, oscilloscopes and pulse generators. Additional test circuits such as sequence

generators, code converters, alpha-numeric displays and thumbwheel switches will be used to test the programming of the monitor reference memories, the recovered digital data and the selection and timing circuits of the broadcast unit and TMC.

With the exception of the remote flow pattern selection, the digital data TMC is completely independent of the digital data broadcast equipment and transponder. The monitor simply operates off the detected RF pulses. The monitor shall alarm if an error exists in two consecutive words. This error can be the result of the loss or gain of a data bit or loss of word sync. The monitor shall also alarm if a word is repeated other than two consecutive times and in the case where the duty cycle is longer than 30 sec.

In a dual installation both monitors are paralleled and both will be required to sense an abnormal condition to produce transfer or shutdown of the digital data broadcast equipment.

4.2.3 Control and Transfer

This section describes the operation of the DDB Data Generator and Monitor equipments which are installed in a dual configuration. If the Engineering Model or any subsequent station equipment is installed in a single configuration, the Control and Transfer functions will be modified by simple wiring changes to the appropriate equipment interface cables.

For dual installations the data broadcast Control and Transfer unit shall interface with either the RTC-1, RTC-2 or RTC-3 TMC. The interface shall operate from a remote location, and equipment necessary for remote alarms and remote DDB control will be provided. The interface unit will include provision for local or remote operation for troubleshooting and repair. Indicator lights and CW tone will give visual identification both locally and remotely of operating Data Generator and Monitor equipment and of those which have exhibited a fault.

The local control will also permit operation of either monitor or either data broadcast unit without danger of transfer being made by remote control. Local control permits test, calibration and maintenance of the equipment without shutdown of the data broadcast capability. The remote operation under which condition the equipment is normally operated permits selection and transfer of equipment by telephone dialing. Automatic transfer shall permit unattended operation with the control in the remote position. Reset of the equipment shall permit unattended operation with the control in the remote position. Reset of the equipment shall also be controlled from either the local or remote location. The operating data broadcast unit upon reset shall than be termed the "Main" unit with the other unit becoming the "Standby" unit.

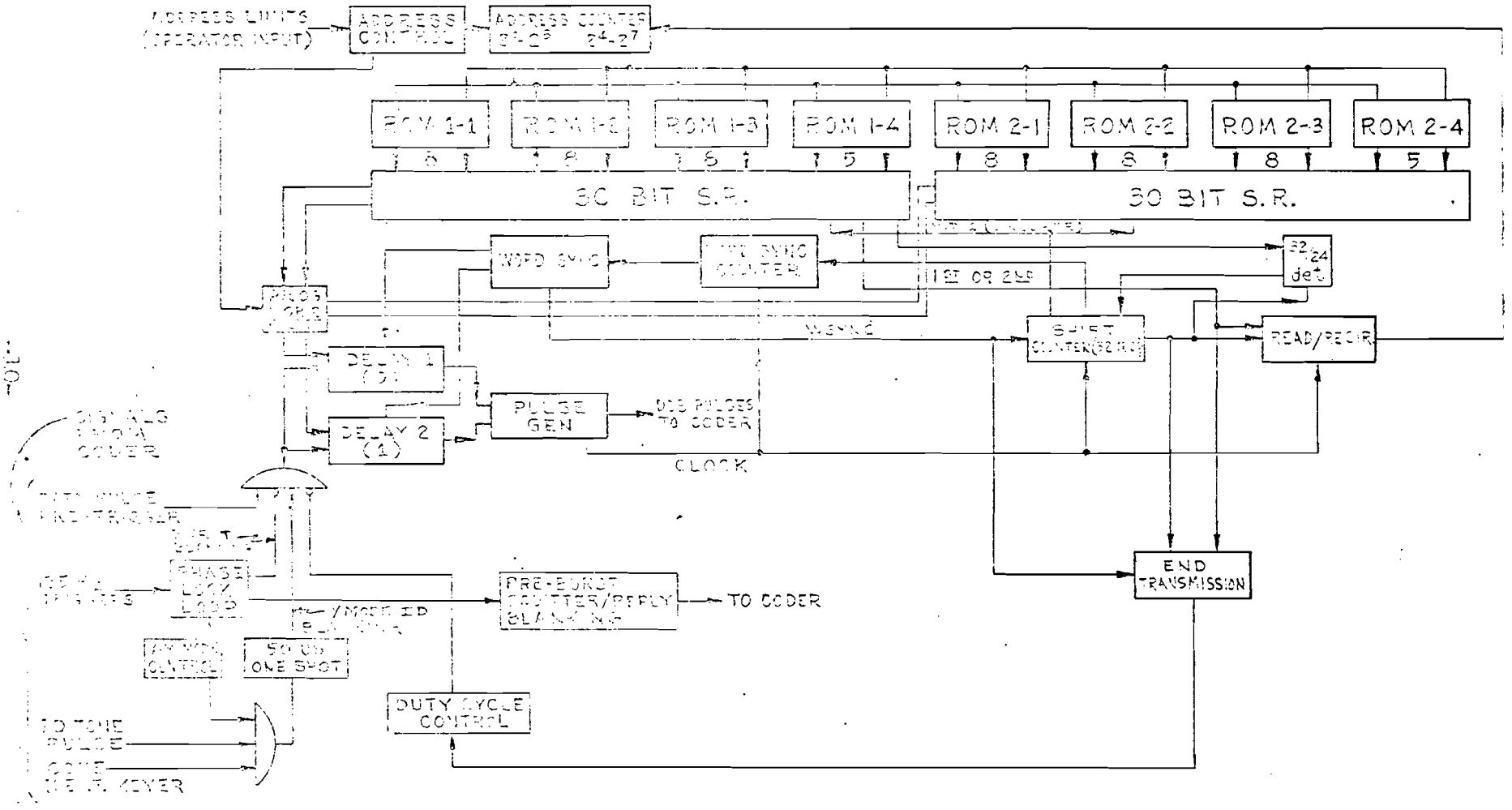
Dialing codes will be assigned to the broadcast and TMC units to provide remote dialing over the existing remote control telephone line. Combinations of numbers when dialed will then transfer,shut down or reset the various equipment in accordance with the selected code.

4.3 Electrical Design

4.3.1 Data Generator

The section of the Design Plan describes functional operation of the Data Generator. The equipment block diagram is shown in Figure 4-2. It is recalled from Volume 2 that each data word will be sent twice. The first bit of each word will be used to identify whether it is the first or second word of a two word group. This bit will therefore alternate between a "1" and "0" and will not be stored in the data memory. Therefore, each 30 or 24 bit word will require 29 or 23 bits of memory respectively.

This data is stored in the Read-Only Memory (ROM) and is accessed by a memory access counter. The data is stored in the order in which it is used. Word sync data is also generated outside the ROM by a work sync counter, which receives an input from the shift counter. Its function is to provide word sync levels preceeding and following each DDB word. Word sync and data levels enable the delay networks to provide output pulses to the coder following a data request from the coder.



DATA GENERATOR - FUNCTIONAL BLOCK DIAGRAM

FIGURE 4-2

All counting and shift operations occur after data pulse generation, in order that inhibit functions (to be described) can inhibit pulse outputs without destroying information not transmitted. If shifting occurred before transmission and the output pulses were then inhibited, an error would be generated. The output pulses are fed to the coder, to generate the appropriate RF data pulses which are added to the normal TACAN/DME pulse pairs.

Following the complete transmission of each two word group, further transmission is inhibited by a duty cycle control to maintain a fixed data rate.

The address counter is also operator controlled, since not all VORTAC stations will use the entire 512 memory locations.

No data is transmitted with Y Mode identification outputs, although data is produced with Y Mode equalizer outputs. Data is also inhibited when reference bursts are present (see Volume 2). These conditions must be anticipated so that data output may be inhibited. These inhibit controls also provide squitter/reply blanking during a short interval preceding each reference burst to prevent pairing of squitter and burst information which might be decoded as erroneous DDB data. (See Volume 2).

The paragraphs which follow provide more detailed descriptions of each of the major functional elements of the Data Generator Sub-System.

4.3.1.1 Memory

The basic chip for the Digital Data Broadcast will be a reprogrammable Read-Only Memory (ROM). The device chosen has a capacity of 256 - 8 bit words. Four of these chips will provide a capability of 256-32 bit words which makes up one memory unit. Since the maximum word length in DDB is 30, one memory unit provides a storage capability of 256 DDB words.

The memory selected is available from at least two sources, INTEL and Microelectronics International. The memory is programmed initially by connecting the address lines to a 40V source which is considerable above the normal read levels.

Reprogramming of the memory is possible with these devices by exposure of the chip to a source of ultraviolet light to erase the old data and subsequently programming the ROM with - How? new information. The entire memory must be reprogrammed. Partial programming is not possible. The package selected is directly compatible with T^2L integrated circuits.

The above device was selected over the more common ROM types because common ROM devices are made from special masks and once made they cannot be changed, other than by chip replacement. The mask is used to make any number of memory devices all with identical stored information. Since all VORTAC stations require different information, separate masks would be necessary for each station. This alternative

is expensive and requires stocking of a great number of individual items. It is therefore rejected for this application.

Another alternative considered was a PROM Programmable Read-Only Memory) in which permanent storage is developed by burning out diodes or Nichrome fuses in the chip. These can be programmed for automatic operation. They cannot be reprogrammed except for very special cases. In the event of errors or possible desirable changes in the program, the change must be altered by chip replacement. These would be, however, a viable alternative after the information to a particular VORTAC station is deemed permanent.

Random Assess Memories (RAM's) could also be used. However, extensive design would be necessary to harden the memory against power or equipment malfunctions. Difficulty in programming the RAM off-site and inserting it in the equipment is also a problem. The reprogrammable ROM selected overcomes all of the objections stated and is thus EDMAC's choice for the storage of DDB data.

4.3.1.2 Memory Address

The DDB will be stored in a fixed order. A counter consisting of ten flip-flops representing 2^0 to 2^9 will be stepped, thereby reading a new set of data for each step. All four ROM chips (two extra bits are provided to allow expansion to 2048 words) will be

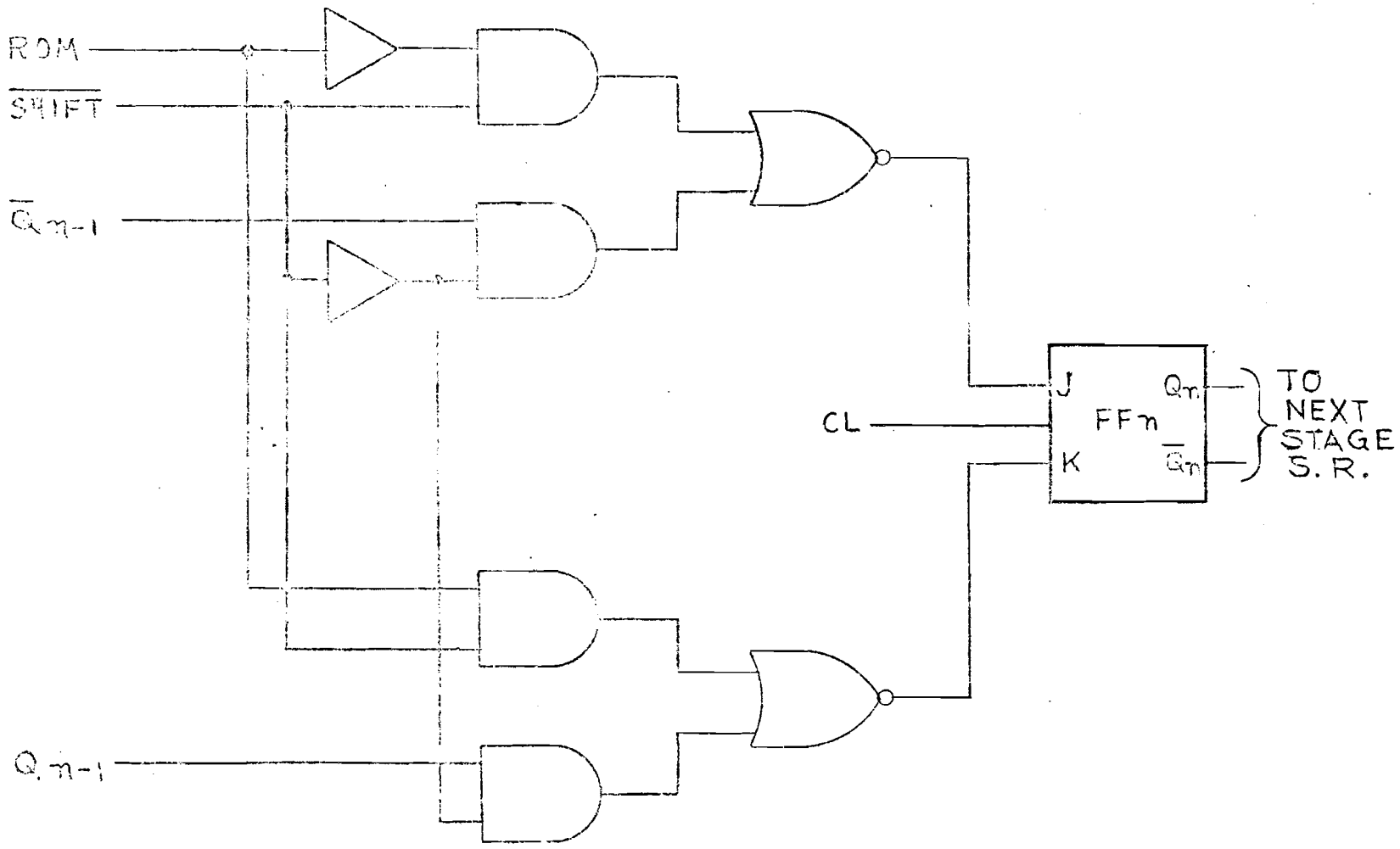
addressed simultaneously for simplicity of address and readout circuitry. The data from the ROM Unit will be read into a parallel-fed shift register which serves as a temporary memory. See Figure 4-3 for a typical shift register stage. The address counter will be asynchronous (ripple) design. Synchronous design cannot be justified in that the data rate is low, and the extra complexity is unwarranted.

The address counter will be stepped following transmission of the last data bit. There is always a substantial delay between DDB groups to insure proper duty cycle operations. The new data will have been ready throughout most of this period. The Counter can be started and stopped at any count so that the same storage unit can be used for all stations.

4.3.1.3 Data Request and Timing

The address counter, shift counter and word sync generator all derive their timing from an impulse from the coder. This is essentially a pre-trigger for DDB data. A counter is inhibited by inhibiting the clock impulse derived from the coder to the particular counter.

The identification of a DDB impulse as a logical "1" or a logical "0" is determined by the time relationship to the normal TACAN/DME pulse pair. Therefore, when a data request impulse is sensed, which also has a fixed relationship to the pulse pair, a delayed data impulse is generated. Two delay networks



PARALLEL IN, SERIAL OUT S.R. (TYPICAL)

FIG. 1-2

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are used, one each for the logical zero or one condition.

The selected condition will be determined by the state of the shift register output. The shift register output may, of course, be overridden by the word sync generator which will activate both delay circuits to provide word sync information. Both the shift register and the word sync generator may be inhibited by the signals previously described, thereby inhibiting both delay networks and transmitting the pulse pair without data.

4.3.1.4 Data Generation

Data is stored temporarily in a 30 bit shift register. Since the information is to be used serially, it is much more convenient to use data in a shift register than to use data directly from the ROM. Each word group is transmitted twice (see Volume 2). As data is shifted serially through control logic to the coder, it is recirculated once into the same shift register, thereby eliminating the necessity of storing each word twice in the ROM. An identifying digit is inserted during recirculation to identify the transmitted word as the first or second group. A Parity bit is stored in the ROM. Parity check is not performed on the identifying digit. This digit is also used to control the change of address. If the second group is being generated after the last digit the address will be changed to the ROM.

The shift impulses will be counted by a binary counter identified as the shift counter in the block diagram. This counter will stop at either 23 or 29, depending upon the length of the word transmitted. Both shift and change address signals will take place after generation of a data bit, to simplify timing.

The shift mechanism is interrupted by various signals, and data from the shift register is inhibited from transmission. Data will not be transmitted during the 15 Hz North reference burst or the 135 Hz Auxiliary burst. Also, during Y Mode ID Tone, data is added only to the equalizing pairs (see Volume 2). At each end of the DDB information a word sync group will be generated. This is a group of two pulses immediately following a pulse pair, for each of three seccessive pulse pairs. (except as blanked due to reference or Y Mode Identifier controls, above). These word sync groups will be generated by a word sync generator which counts the groups and inhibits the shift counter during word sync generation. All DDB pulses are synchronized to the last pulse of the TACAN/DME pulse pair. Since this pulse has the shortest interval to the time of data transmission, timing errors are minimized.

4.3.1.5 Squitter and Reply Blanking

Under some conditions, it is possible for reference bursts to combine with squitter or reply outputs such that an erroneous data pulse may be detected. It is essential that such

combinations ar eliminated. Therefore, a squitter blanking signal will be generated from the 15 Hz on 135 Hz reference bursts. This blanking gate will occur 45 microseconds before each X Mode burst and 75 microseconds before each Y Mode burst (see Volume 2). These blanking gates will be obtained by phase locking to the antenna reference triggers and extracting an appropriately timed pulse prior to each burst to initiate the blanking gate.

4.3.1.6 Duty Cycle Control

All data will be sent in two word groups, which utilize successive reply and squitter pairs. When the two word group and word synch have been broadcast, the Data Generator is inhibited such that no data is attached to a number of subsequent pulse pairs. The exact number of pulse pairs containing no data is determined by the duty cycle control which is manually adjusted at each station as a function of data volume and cycle time.

This duty cycle, as applied to the DDBS, will inhibit DDB data when the duty cycle is exceeded. One possible method of generating an inhibit gate is to derive a voltage proportional to the rate of squitter pulses generation. This is accomplished by generating a pulse of variable width after each squitter or reply pair, and integrating these pulses. The pulse width, being variable, provides an operator input. The pulses are then added to

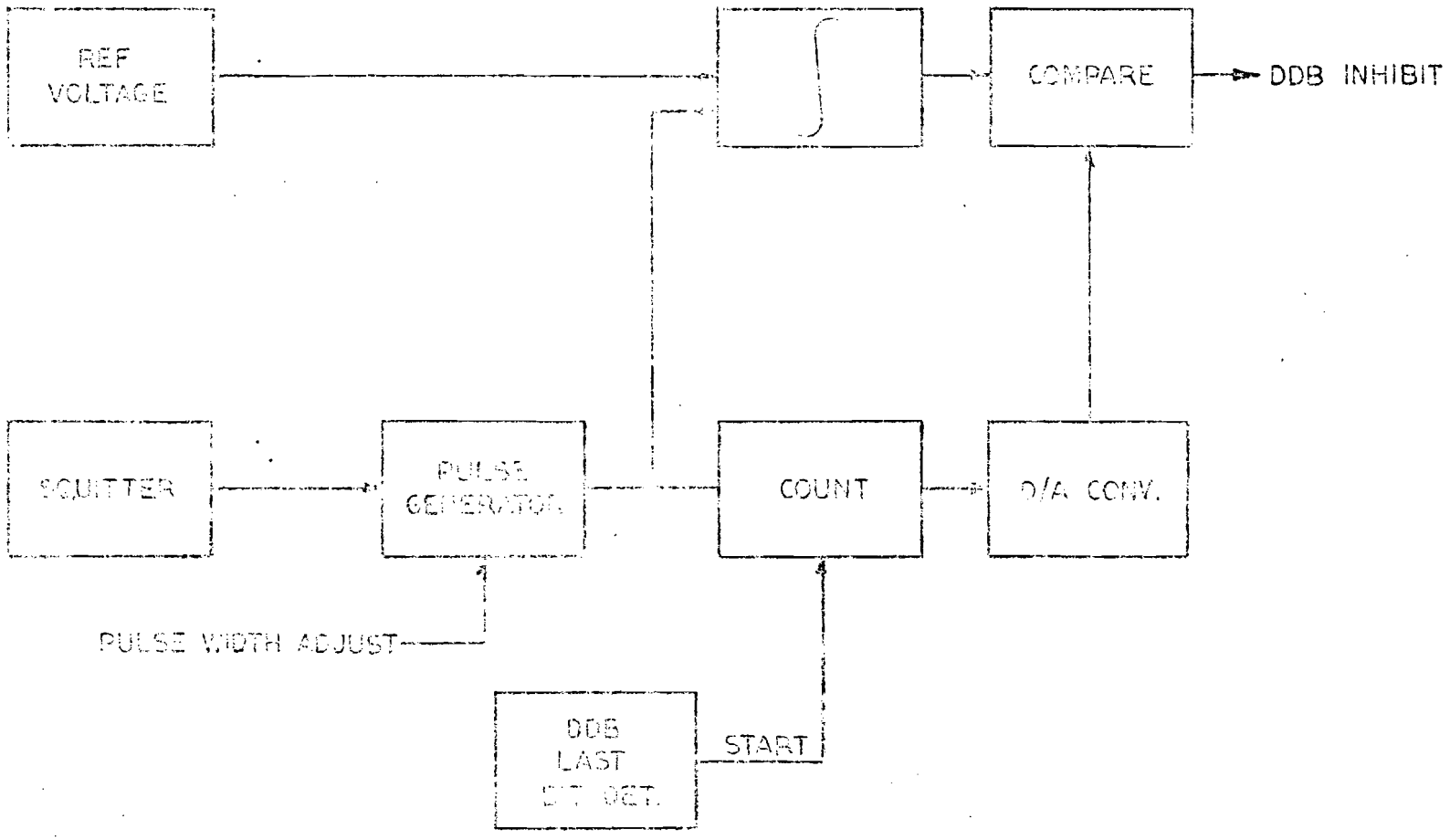


FIG. 4-4
DUTY CYCLE CONTROL

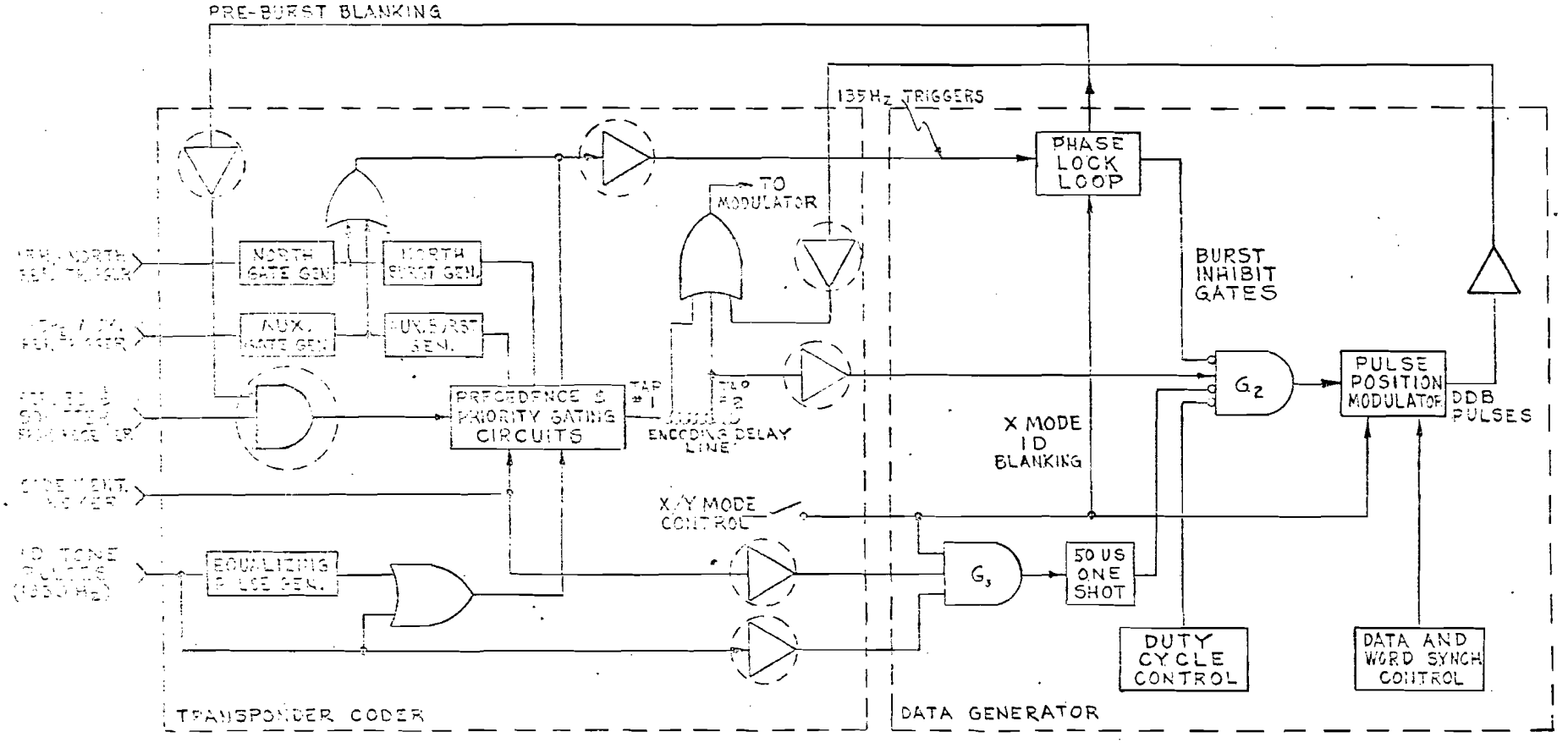
a reference voltage and integrated, providing a D.C. level proportional to the rate. (see Figure 4-4)

A ramp generation (or its digital counterpart, the staircase) is then initiated. This is compared to the rate voltage. An inhibit gate is initiated with the ramp, and stopped when a comparison is reached, thus controlling the duty cycle of the DDBS by inhibiting data output.

The delay between data groups may be as great as 0.1 seconds. Although delays of this magnitude may be generated by analog techniques, a staircase generator is less susceptible to drift and power supply changes, and in general is a more stable approach. The staircase will consist of a counter, stepped by successive TACAN/DME pulse pairs, and a ladder network. At the end of the gate (when comparison occurs) the counter will reset remaining so until the end of the next data group.

4.3.1.7 Interface With Transponder

This section describes the interface which is required between the Data Generator and Transponder to accomplish the addition of data pulses to the TACAN/DME pulse pairs. The entire interface will be accomplished by a set of interconnections between the Data Generator and the Coder, as shown in Figure 4-5. In order to provide a maximum of flexibility, the Coder



NOTE: ALL ELEMENTS OF THE CODER WHICH ARE CIRCLED IN DOTTED LINES REPRESENT CIRCUITS WHICH MUST BE ADDED TO THE PRESENT EQUIPMENT TO PROVIDE THE DDB INTERFACE

FUNCTIONAL DIAGRAM OF DATA GENERATOR-CODER INTERFACE

FIGURE 4-5

modifications required to support the DDB function will be designed on the basis of having the DDBS interface with either the existing Coders or those which will be equipped with a Y Mode modification.

Figure 4-5 shows each of the I/O lines isolated by buffer amplifiers which will basically consist of level shifters and drivers to properly match the tube circuit signals in the coder with the logic circuits in the Data Generator. Circuits which must be added to existing Coders are shown in dotted circles. The basic input to the Data Generator is the output of the second tap of the encoding delay line. Whenever this trigger is received by the Data Generator, the logic circuits will add appropriately timed data pulses or word synch pulses, or add no data, depending on the state of the data control logic.

There are three basic inhibit functions which prevent data from being generated. These are shown as inhibit inputs to G_2 in Figure 4-5. The first is the Burst Inhibit Gate which prevents data from being added to pulse pairs which form the Reference Bursts. These gates will be developed by a phase lock loop which locks to the combined 15 Hz and 135 Hz antenna reference triggers. The second inhibit function will eliminate data from being added to ID Tone Pulses in the Y Mode of operation. This is discussed in detail in Section 2.2.6.7 of Volume 2.

Whenever Y Mode is in use and ID Tone Pulses are being generated, a 50 microsecond one shot will be triggered to blank the ID pulses which appear at tap #2 of the encoding delay line, but not the equalizing pulses. The third inhibit function will be derived from the duty cycle control which determines the effective "off time" of the Data Generator after each two word group is broadcast.

The DDB pulses developed by the Pulse Position Modulator are sent to the Coder where they are added to the encoding delay line output prior to being sent to the Transponder Modulator. The same Phase Lock Loop which generates the Burst Inhibit Gates will also generate a pre-burst blanking gate to prevent squitter or reply pairs from being transmitted just prior to a reference burst. (This blanking is necessary to prevent burst pulses from being erroneously interpreted as data pulses. This problem is described in detail in Section 2.2.6.4 of Volume 2) This blanking gate is sent to gate #2 in the Coder. This gate will prevent reply/squitter pulses from the Receiver from being inserted into the Coder's priority gating logic.

4.3.2 Test Monitor Control (TMC)

The primary functions of the Digital Data Broadcast TMC is to monitor the transponder output signals, separate the Digital Data Broadcast messages from the other signals, check for validity with a parity check, and check for

validity using digital comparators to compare the received words with a stored monitor reference memory, identical to the one located in the Data Generator. Figure 4-6 is a block diagram of the Data Broadcast TMC.

The input to the monitor is the detected RF signal via the half-amplitude detector in the existing TMC equipment. The pulses are then shifted down a digital delay line where two operations occur simultaneously. Down the delay line are located two windows, 12 usec or 30 usec apart depending on which mode of operation is used (X or Y). When a pulse appears in both of these windows simultaneously indicating a TACAN pulse pair, both the data A and B positions are investigated for data or word sync pulses. The monitor reference memory is synchronized to the transmitted data by detection of the identification words. Once the memories are synchronized, the data following three consecutive word sync pulses is loaded into a 30 bit shift register for parity check and bit by bit comparison with the monitor reference memory.

Since the order of data transmission is three word-sync pulses, a data word, three more word-sync pulses, a repeat of the data word and three more word-sync pulses, the monitor memory is stepped to the next word after the reception of three groups of three word sync pulses.

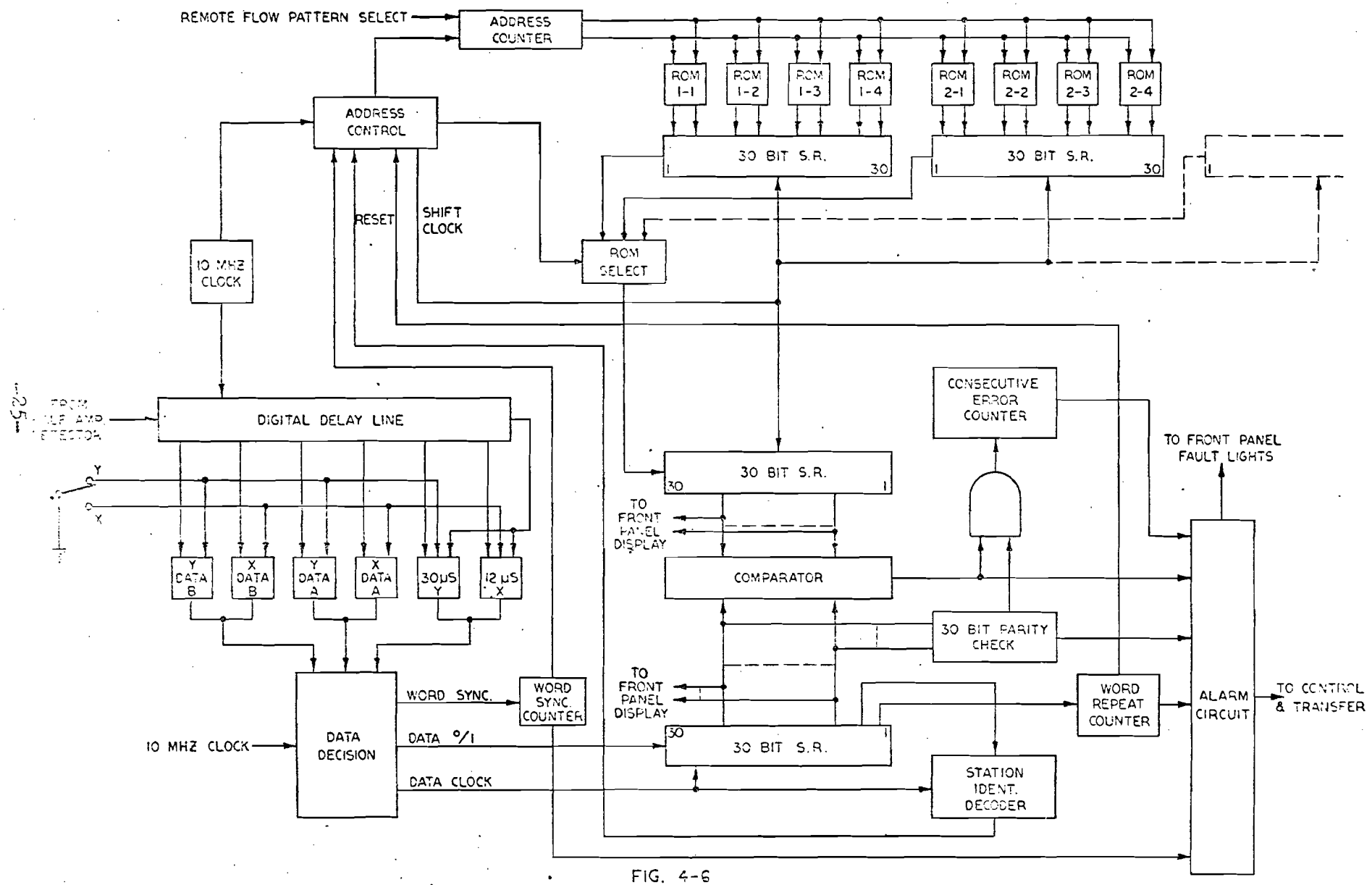


FIG. 4-6
DATA BROADCAST TMC BLOCK DIAGRAM

An alarm is sounded when one or more errors occur in two consecutive words. This error could be the result of invalid parity check or bit by bit comparison. An alarm is also activated if a word is repeated other than two consecutive times or if a complete flow pattern is not generated at least once every 30 seconds.

For purposes of testing and troubleshooting, the monitor detects and decodes the binary information into alpha-numeric displays.

Work selection for dispaly purposes from either the recovered Digital Data Broadcast or the monitor reference memory is accomplished via a front panel thumbwheel switch. Refer to the mechanical design, Section 4.5, for a more detailed description of the front panel.

The monitor reference memory is programmed identically to the data broadcast memory. For a detailed description of this process of programming refer to Section 4.4.

4.4 Programming of the Read-Only Memory

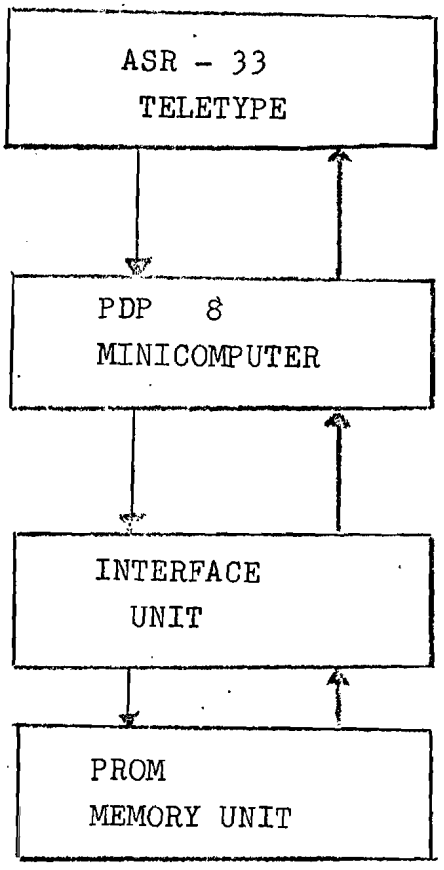
The selected ROM is erased by exposing the device to ultraviolet light and subsequently reprogrammed by connecting appropriate terminals of the memory to -40 V. It is possible, of

course, to manually perform the connections for each bit stored. Since ther are 29 bits or 23 bits stored for each piece of data, (the first bit of each word is inserted externally) with a possibility of 256 data words per memory unit, it is obvious that such an operation is tedious and prone to error. The problem is further compounded in that each VORTAC station requires different DDB data than any other, and will very likely have more than one possible traffic flow and hence more than one set of data per station.

It is essential, then to provide a user oriented mechanism by which data can be typed, checked, and errors corrected. The method should not be so singular that only one type of memory device is usable. The selected technique can be used with the reprogrammable ROM, or, with some modification, with field programmable types, if such are later desired.

Data entry, for convenience of the operator in both entering data and checking the data before programming the chips, will be typewritten with a hard copy out by means of a teletypewriter (TTY). A means to store the entire BBD information before programming is also necessary, so that format accuracy may be assured and any desirable changes implemented. See block diagram, Figure 4-7.

Data input, therefore, will be from a teletype and small general purpose computer. The storage needed for 256 - 29 bit words is 7424 bits. Some storage is also necessary for control and bookkeeping functions, so memory



Typical Computerized

Memory Programmer

Figure 4-7

in the order of 12,000 bits is desirable. Less input data would, of course, reduce memory requirements. It is possible to reduce the amount of computer storage by entering each 29 bit message in the ROM directly. The ROM programming however, requires ten repetitions of a 20 microsecond impulse at a 2% duty cycle, for a total of 100 sec. per 29 bit word. The advantage of inserting and checking all the DDB information before the ROM is programmed, therefore, is obvious.

The program used for data insertion should be user oriented. Inputs should mode in a conversational mode with the computer. A typical example might for instance be:

17. STATION IDENTIFIER AND COVERAGE CLASS- - - This statement would represent a request from the computer to the user, after which the user would type in the required information. This type of format is much more easily verified than presenting an operator with a sheet containing numbers only, without attaching any identifying nomenclature.

An address buffer will interface the computer with the ROM. This will provide the necessary -40 V. levels necessary for ROM programming cycle, will provide the 20 milliseconds pulse width, and will cycle the memory through the 10 repetitions required for storage. The computer will be informed of the completion of the cycle and proceed to the next cycle. The programming process in the ROM can therefore continue without operator presence.

A parity bit is written in the ROM with each word. Inclusion of parity with the data enables another test to be performed on the ROM prior to its use. In addition, loss of parity in data is an important cause for suspicion. If the first or second group identifier were missing, the data could still be useful.

Upon completion of the entering of DDB data in the ROM, the contents will be read and compared with the stored data in the computer. Any errors will be presented for operator confirmation.

Possible computers for use in this system are:

Digital Equipment Corporation
- PDP-11
- PDP-8

Data General
- NOVA 1200
- NOVA 800

Varian
- 620 L

Intel
- Intellec 8

Two of the above equipments were assessed to be the most cost-effective for the DDBS. These are Digital Equipment's PDP-8 and Intel's Intellec 8. These are described in the paragraphs below.

The Digital Equipment Corp.'s PDP-8 with a normal 4K of memory (4096 -12 bit words) is directly compatible with an ASR-33 teletype. The DDB data must be stored, then, in a

minimum of three slots in the PDP-8 core. A more desirable method is to use four slots using the remaining digits as address for the ROM. The core will then be strobed four times, filling a buffer register in the interface unit with address and data information. When data transfer is complete, a flag is turned on (flip-flop signal to computer) to inhibit further information transfer. A counter internal to the PDP-8 will keep track of the transfer cycles. A block diagram of the computer-ROM interface is shown in Figure 4-8.

Following data transfer, the interface unit will develop the voltages and timing impulses necessary for ROM recording. When the recording cycle is complete, the flag is again turned off, allowing the computer to generate the next cycle. When all recording cycles are complete, the computer will proceed to read the ROM, comparing the contents with the core memory.

The PDP-8 can be programmed to display any errors to the operator. If no errors are found, it will display a "no errors" message, indicating that the memory process is complete and correct.

An alternative to the Digital Equipment Corporation PDP-8 system is being marketed by Intel, called the Intellec 8. This entire system includes a small computer with an interface module specifically designed for programming Intel ROM devices. This computer is programmed through an ASR-33 teletype, as is the PDP-8. This system is being investigated thoroughly for possible cost savings.

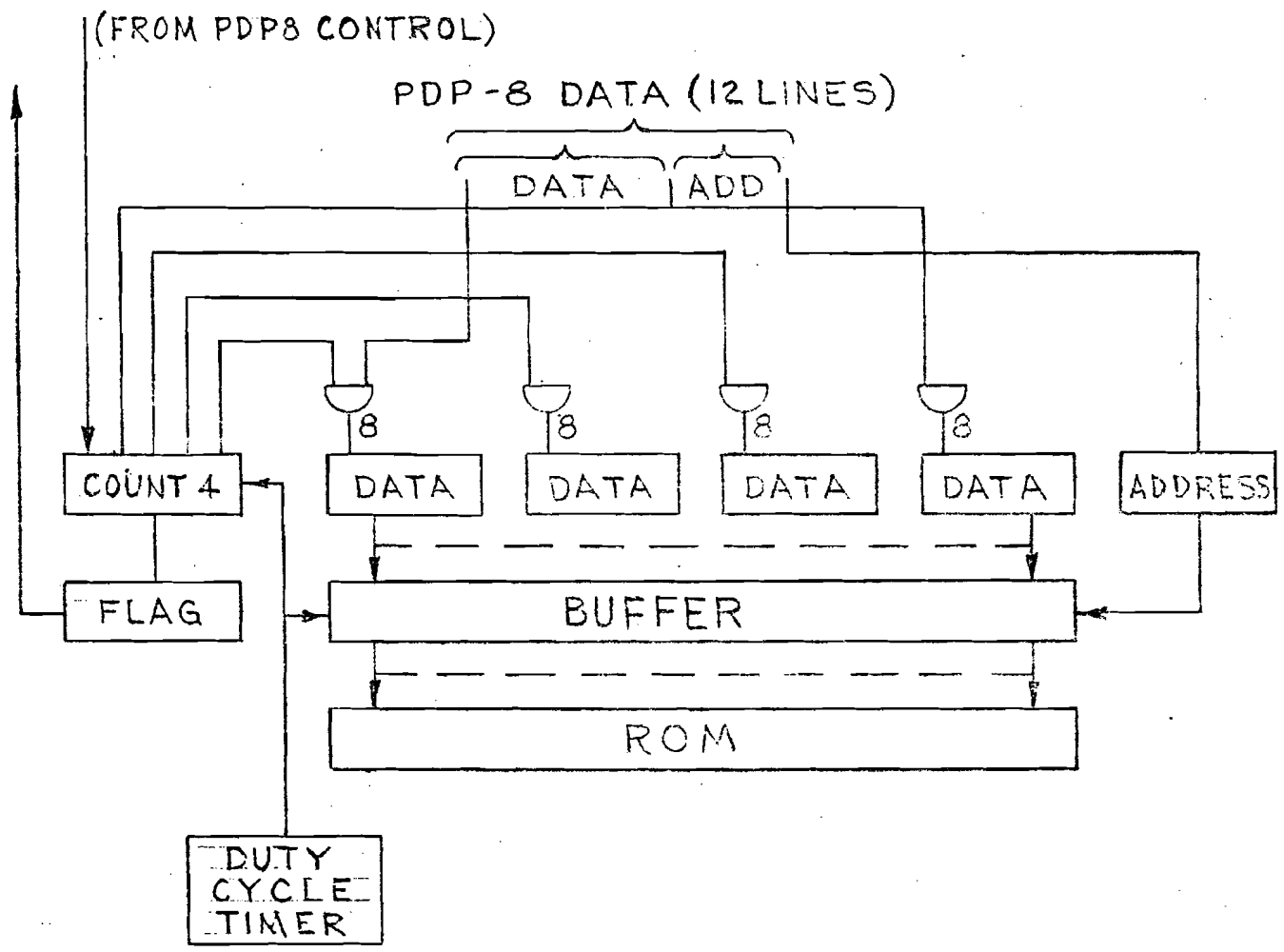


FIGURE 4-8. BLOCK DIAGRAM OF PDP-8 TO ROM INTERFACE.

The operation of the Intellec 8 system parallels that of the PDP-8 system previously described, without the need for design of an interface unit. The decision will be made shortly, based upon delivery and cost information.

4.5 Mechanical Design

One monitor unit and one Data Generator Unit will be included in a single drawer. The units will be packaged in individual card baskets of 15 cards each. Provision is included for expansion of each memory bank to 8 units 2048 words). Each ROM unit is packaged on a PC card without other circuitry, since the programming levels are different from read levels. The Monitor and Data Generator share a power supply but are otherwise independent.

The front panel control for the Data Generator is the duty cycle control (a manual control with a locking device to prevent inadvertent mis-setting). The X-Y Mode control and address control are driven from remote terminals. A switch for remote or local operation is provided on the control-transfer panel.

Associated with the monitor is a set of four thumbwheel switches to manually select a data word. This is a troubleshooting aid to allow visual diaplay of DDB words (see Figure 4-9). The display also will be on the Data Generator/Monitor panel. Other indicator

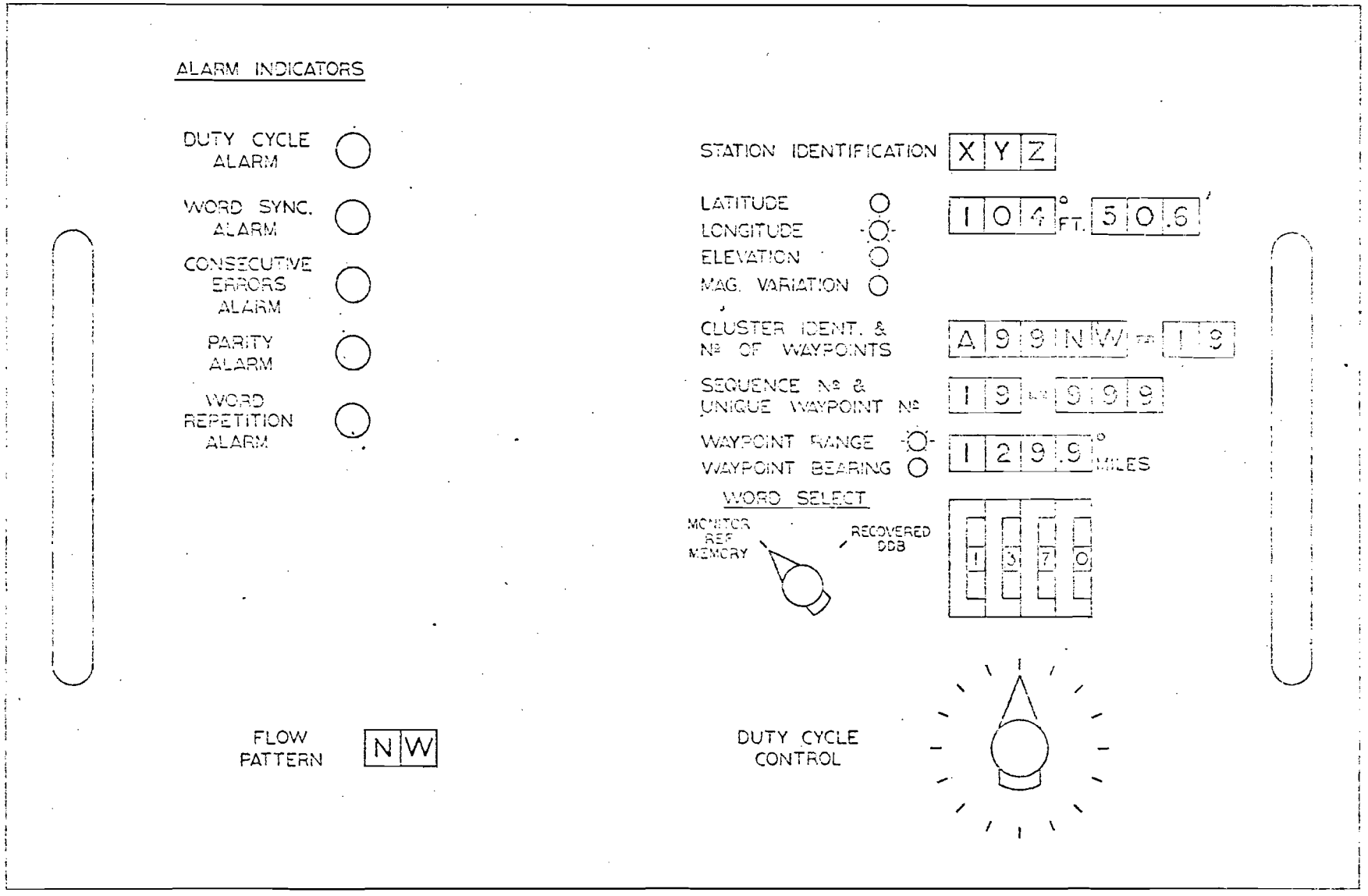


FIG. 4-9
DDB DATA GENERATOR/MONITOR FRONT PANEL LAYOUT

lamps identify errors such as word sync errors, consecutive word errors and "no data" errors.

The Data Generator/Monitor unit will be housed in an upright cabinet rack of welded frame, steel construction. The cabinet shall have a four point base attachment, as specified by the Government. Individual drawers will consist of EIA height hard aluminum front panels and attached aluminum chassis. Access to the equipment drawer will be from the front using full travel ball bearing quick-disconnect locking slides. Rear access to cabling and cable termination will be through a hinged rear door.

Cable retractors will be provided to allow withdrawal and repositioning of chassis without interference from or damage to cabling. External interconnecting cables will exit through a NEMA standard 4 inch square duct located on the top cabinet surface, as specified. A temporary cover plate will be installed on the delivered equipment. A duplex convenience outlet will be provided at the bottom front and rear of the cabinet and wired to a separate 120 volt power source.