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CHANNEL-LOSS DETECTOR FOR LOW-TRAFFIC TELETYPE CIRCUITS

Charles Santora

MAY 1975

FINAL REPORT

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16. Abstract

This report describes a prototype device for application at international flight service stations to detect teletype channel loss by providing an idle signal in the absence of messages and activating alarms when continuity is disrupted or a failure occurs which disables teletypewriter communication. Two units, each comprised of send and receive channel-loss detectors and teletypewriter circuit interfaces and associated alarms, were developed and evaluated at the National Aviation Facilities Experimental Center in accordance with Systems Research and Development Service, Washington, requirements and were found to perform satisfactorily. As a digital device, the channel-loss detector may lend itself to other communication applications as needed.

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PREFACE

Acknowledgement is made to Mr. Louis P. Davis of ARD-222 who, in addition to being project manager, patiently discussed technical solutions as well as requirements.

Acknowledgement is also made to the performance of technician Mr. George Ker, ANA-330, who painstakingly applied effort to uncover shortcomings in components which deviated from their nominal characteristics.

Acknowledgement is finally made to Mr. Andrew Gemski, ANA-120, who contributed the wealth of his experience with various commercial components and provided basic circuit design to best meet performance requirements.

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INTRODUCTION

PURPOSE.

The purpose of this project was to design and produce a prototype device that provides circuit assurance for teletype circuits by detecting a loss in the ability to communicate between two points.

BACKGROUND.

There are international flight service stations (IFSS's) using point-to-point duplex (four-wire, which can simultaneously send and receive) systems on which activity is normally low (i.e., idle at least 60 percent of the time), and an absence or breakdown of contact would not be apparent. It is therefore desirable that such lines be continually and automatically monitored and that alarms be provided for operators so that they may know immediately when any failure occurs as manifested by an absence of a signal (both message and idle).

DISCUSSION

REQUIREMENTS

It is specified that in the absence of a message signal, the channel-loss detector (CLD) (or circuit-assurance device) should send an idle signal from each station teletypewriter transmitter distributor (TD). This idle signal should be an interruption of the normal mark condition for 13.5 milliseconds (ms), such that it comprises a letters-shift character. While the idle signal is being received at a teletypewriter station, the printer, however, shall receive a steady mark. When a message tape is inserted and run at the TD, it shall replace the idle signal, and no more than the first character of the message shall be garbled.

At each teletypewriter station employing this circuit-assurance (or CLD) feature, the device shall consist of a "send" unit, to generate the idle signal in the absence of a message signal, and a "receive" unit, to convert the idle signal to a mark for the printer or allow the message, when present, to be applied to the printer. At each of these units shall be an alarm (light/buzzer), to indicate the absence of both message and idle signals, starting when neither has existed for about 200 ms. In addition, it is specified that spikes or signal interruptions of short duration (less than 5 ms) be disregarded.

SYSTEM DESCRIPTION.

A system consisting of two stations, each with a TD, perforator, and printer, which are supplemented by two interfaces, two CLD's and associated power supply, is shown in a block diagram as figure 1. The letter designations are associated with the interfaces used which are described below. The use of bars over

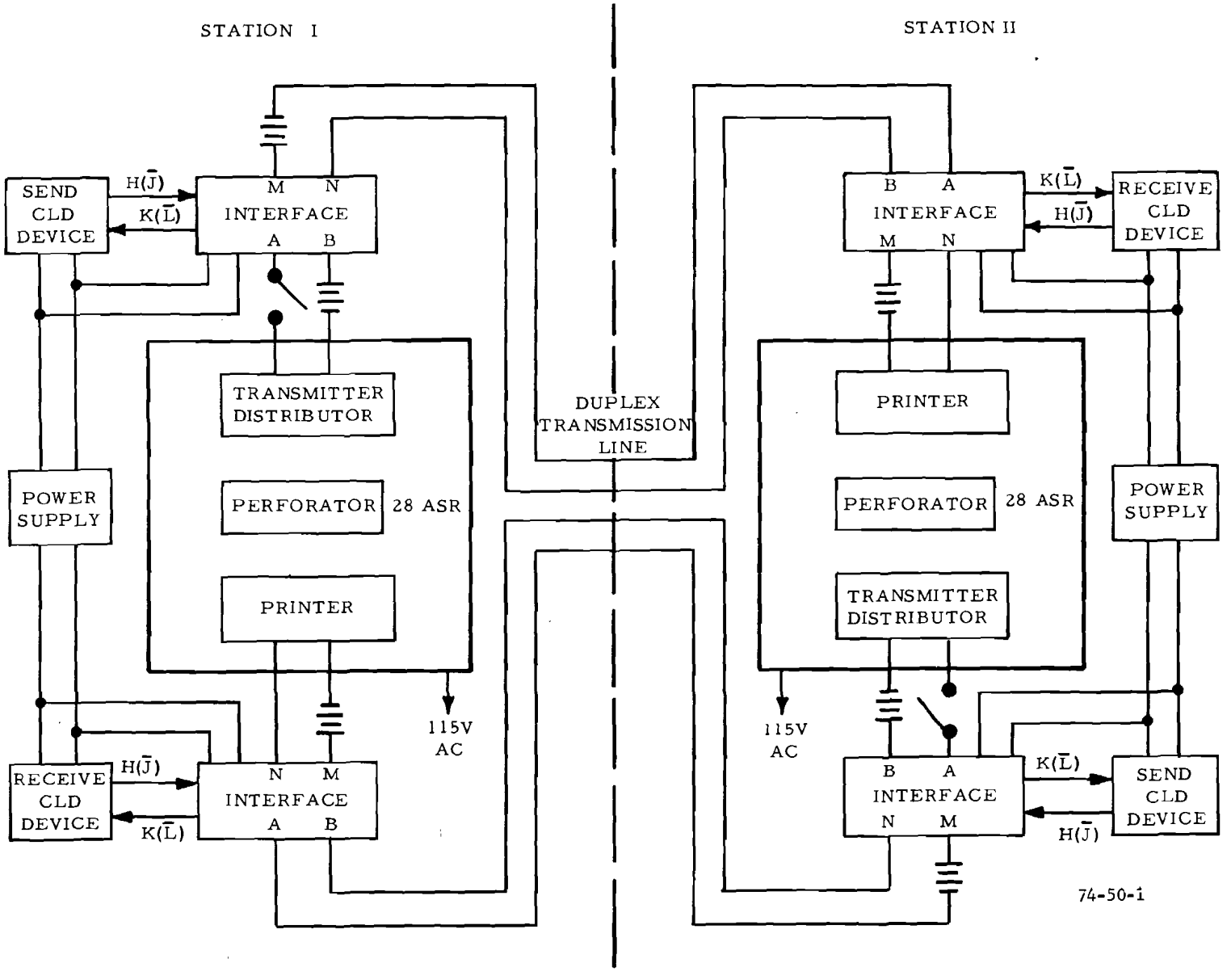


FIGURE 1. TWO-STATION DUPLEX-CONNECTED TELETYPE CONFIGURATION

letters is a logic designation such that when a given letter is zero, the same letter with a bar is 1 and vice versa. For example, K is the same as $\overline{L}$ since the actual terminal L is zero when K is 1 and vice versa. The signal power sources are direct current (d.c.) and are represented by the battery symbol. The essential characteristic is that 60 milliamps (mA) flow in each of the six circuits so powered.

The teletypewriter shown is a 28 ASR (Automatic Send/Receive) comprised primarily of a TD, printer, and perforator (the latter not used with a CLD). The assembly is shown in a block diagram (adapted from the literature) in figure 2. The 28 ASR operates at 5-level Baudot, and this code is given for reference in figure 3.

A Digital Sequence Detector unit (DSD) (model 454-1) was purchased from Pulse Communications (Pulsecom) (Falls Church, Virginia) by the Federal Aviation Administration (FAA), Washington Research Division to provide implicit components which might otherwise require time and effort to build. This DSD contained four "Signal Interface and Timer Module, No. C-100669-1" cards. Two of the signal interface unit portions of these cards are connected in each ASR station shown in figure 1. The circuitry for these identical interface units is shown in figure 4.

The interface provides a high (5 volts) at K when A and B are attached to a 60-mA source. L is then at ground potential. (A resistance of approximately 100 ohms was measured across A and B terminals when interface and power supply were disconnected, and hence the 100-ohm, 2-watt resistor provided by the interface was not needed and was switched out.) The operating voltage across AB measures approximately 3 volts. When loop current flows through the photodiode of the photo-optical coupler device (P), this diode emits light and thereby causes the phototransistor portion to conduct. This conduction places a low at the terminal input 9 of the integrated circuit (E chip), and output 8 (and K) will therefore be high. The external diode across P_1 serves to protect the photodiode from reverse potential. The E-section with terminals 3 and 4 inverts the signal for L.

The interface also provides 60-mA teletype current corresponding to a high at pin H (low at J). (A low at 6, either directly from J, or as a result of a high from H, will predominate over either, imposing a high at point 6.) A low at the E output terminal 6 will result in a mark condition at the output (M-N) of this interface. This is produced in the following fashion: a low at 6 is accompanied by a high at E2 which causes Q_{10} to conduct and the photodiode section to be nonconducting. The phototransistor section is then also not conducting, and transistor Q_6 will therefore conduct, due to the higher potential at its base. The successive transistors, Q_5 and Q_4, will also conduct and MN can conduct the 60 mA required for 28 ASR teletype operation. The vital interruptions of this current mark condition to comprise the signal pattern is accomplished by lows at H and an inverse set of conditions (highs at E6, lows at E2, conductions of Q_{10} and photodiode, conducitons of phototransistor, and nonconductions of Q_6, Q_5, and Q_4) which result in cutoffs of MN current (space conditions).

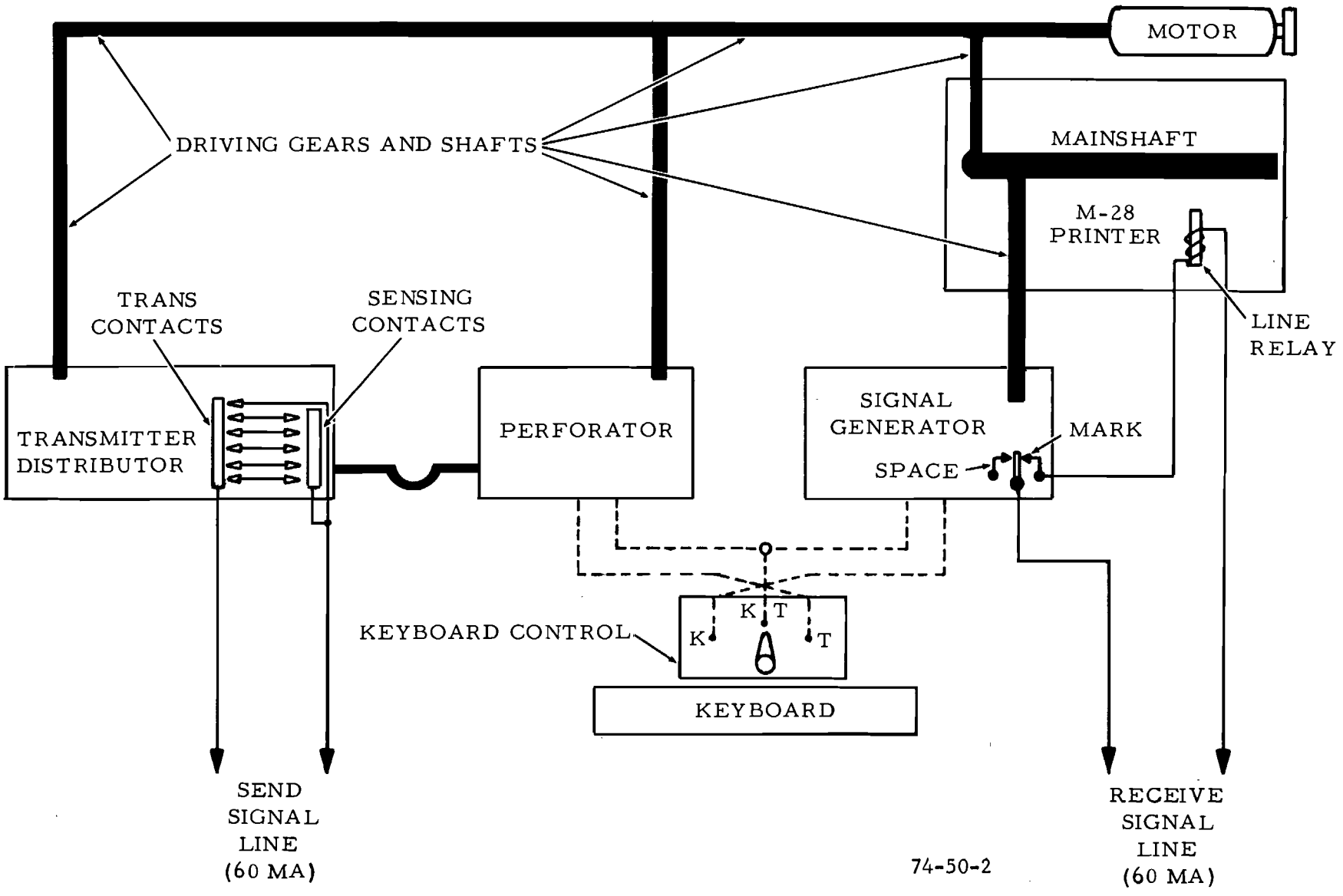
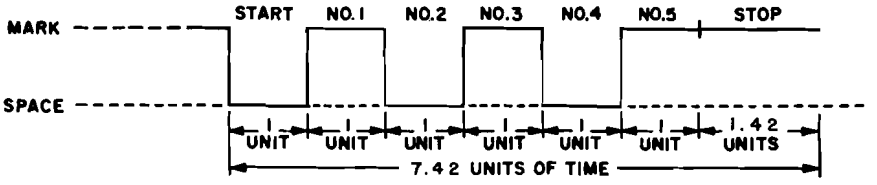


FIGURE 2. 28 ASR SET BLOCK DIAGRAM (DUPLEX CONNECTION)

FIGURES	–	5/8	WRU	$	3	1/4	&		8	'	1/2	3/4	.	7/8	9	0	1	4	BELL	5	7	3/8	2	/	6	"						
LETTERS	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z	BLANK	LETTERS	FIGURES	SPACE	CARRIAGE RETURN	LINE FEED
1	●	●		●	●	●				●	●						●		●		●		●	●	●	●		●	●			
2	●		●				●		●	●	●	●				●	●	●			●	●	●					●	●			●
3			●			●		●	●		●		●	●		●	●		●		●	●		●	●			●		●		
4		●	●	●		●	●			●	●		●	●	●			●				●		●				●	●		●	
5		●					●	●				●	●		●	●	●			●		●	●	●	●	●		●	●			

CHARACTER ARRANGEMENTS (FIVE LEVEL)



CURRENT WAVE FORM FOR LETTER "Y"

FIGURE 3. FIVE-LEVEL BAUDOT CODE

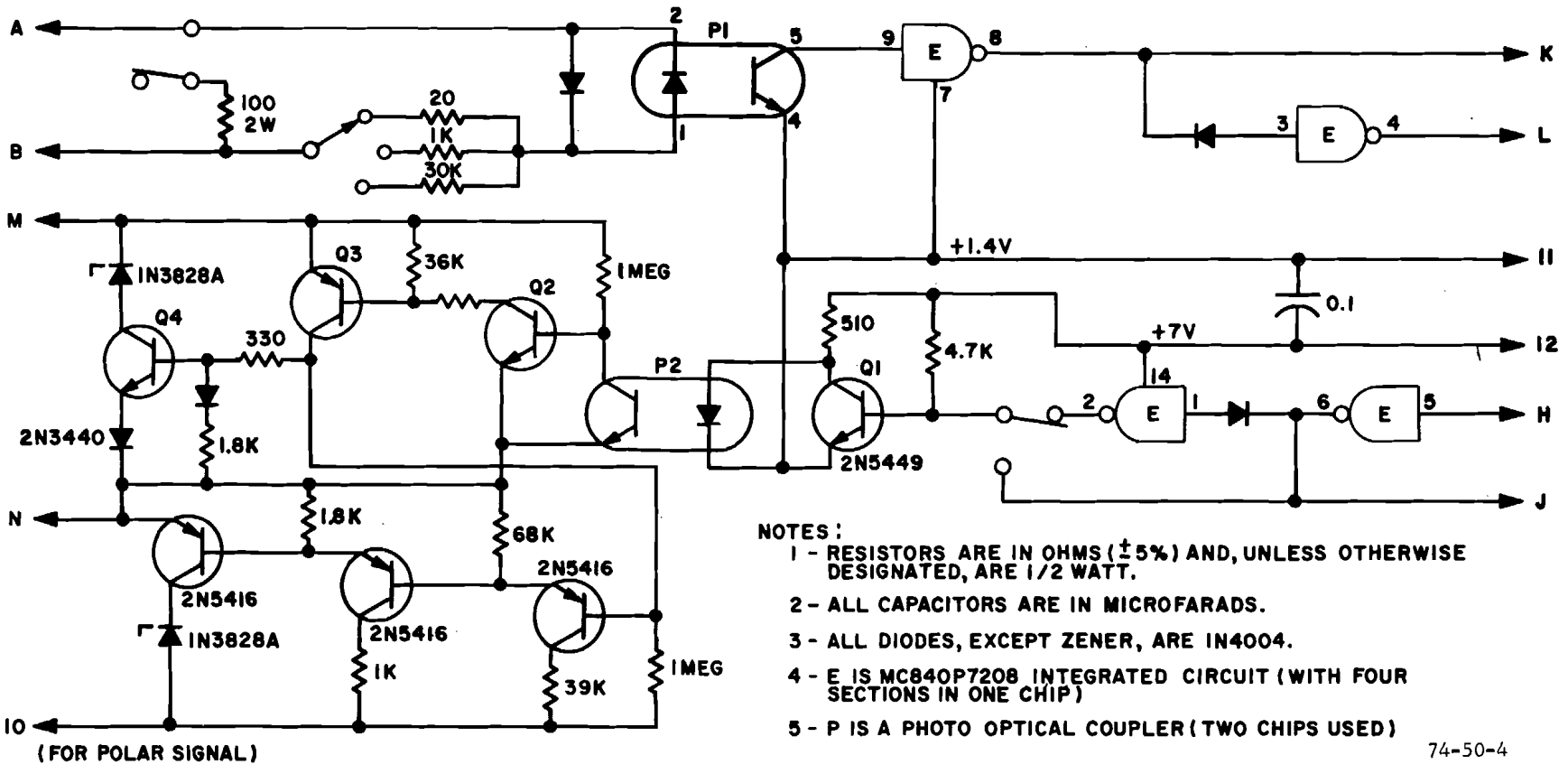


FIGURE 4. SIGNAL INTERFACE UNIT

In figure 4, output 10 (at lower left) is provided for a polar signal output requirement which was not employed in this undertaking. (The three transistors associated with terminals 10 and N act inversely to Q_6, Q_5, and Q_4.)

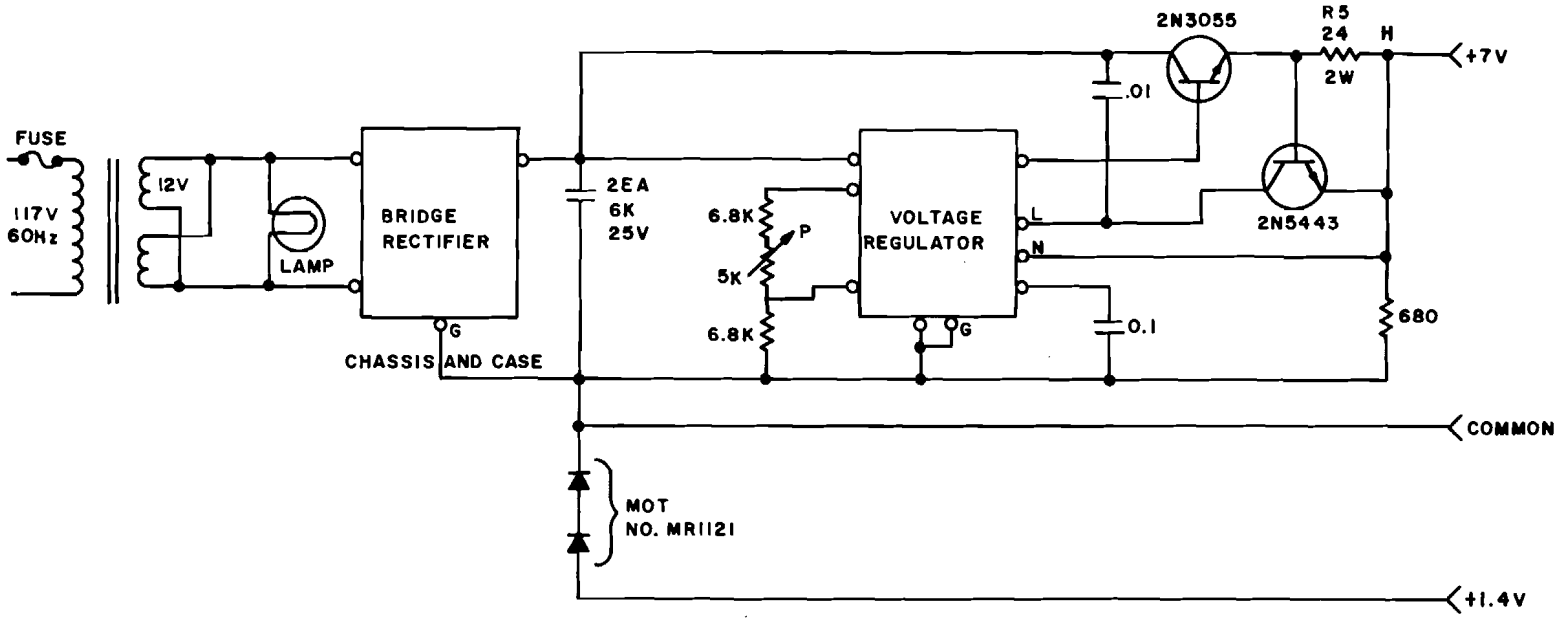
The power supply used for the interfaces, and the send and receive units which were designed and constructed for channel-loss detection, was also part of the pulsecom DSD. It is designated as model 5824-1, which provides +7 volts d.c. (up to 4 amperes) +1.4 volts d.c. (up to 5 amperes), and a nominal ground at zero potential. The circuit for this, which is adapted from the Pulsecom Instruction Manual, is shown as figure 5. (For simplification, one of two parallel +7 volts d.c. generators was omitted.) Two features to be noted are: (1) potentiometer (P) allows moderate adjustment of amplitude of the output voltage, and (2) the 2N5443 transistor acts as a current limiter by conducting when a high current flows through R_5, as when 7 volt d.c. output is shorted to ground, and there is decreasing potential at point L to the regulator to enable limiting (point N is the normal regulating input).

Because the output and ground situation are not straightforward, proper and clear use can better be understood by a simplified representation drawn in figure 6. Note that there is no 1.4 volts d.c. available unless a load is connected across terminals as shown with R load.

FUNCTIONAL DESIGN.

The functional requirements for the CLD should be looked at first in terms of the waveforms existing and needed at various significant points of the configuration shown in figure 1. These are provided in figure 7. Starting at the TD, there are three conditions which can exist there: (1) a steady mark condition (continuous current flow), (2) a message signal, and (3) an open condition (continuous no-current). The first two are the main ones and are shown side by side in figure 7. (The third condition will induce an alarm and is described below.)

Looking at figure 6 and the left half of figure 7, it is to be noted that "X" designates the 1.4 volts d.c. potential, which was used as ground (or common) for the CLD. A mark condition at the TD of station I will be accompanied by 60 mA into the interface and should appear out of the interface as a high (about 5.5 volts); the difference between K_1 (subscript referring to board 1) and X (1.4 volts d.c.) (V_{K_1X} in figure 7). The CLD unit should produce an idle signal corresponding to mark. This is shown as V_{H_1X} which is characterized by a periodic interruption, effectually the geometry of a letters-shift character. The teletypewriter operation is nominally 100 words per minute, which is specifically 74.2 bauds, the stop bit being 1.42 times the other bits (1 bit for start space and 5 for information). Looking at figure 3 and the makeup of a character for the 5-level code, 1 unit of time equals approximately 13.5 ms (1,000 ms divided by 74.2 bauds). The length of interruption used for the idle signal is therefore of this order, 13.5 ms.



NOTES:

1. RESISTORS ARE IN OHMS (±5%) AND UNLESS OTHERWISE INDICATED ARE 1/2 WATT
2. ALL CAPACITORES ARE IN MICROFARADS
3. G IS CONNECTION TO EQUIPMENT CASE/CHASSIS

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FIGURE 5. POWER SUPPLY (MODEL 5824-1) FOR SEND AND RECEIVE UNITS AND INTERFACES

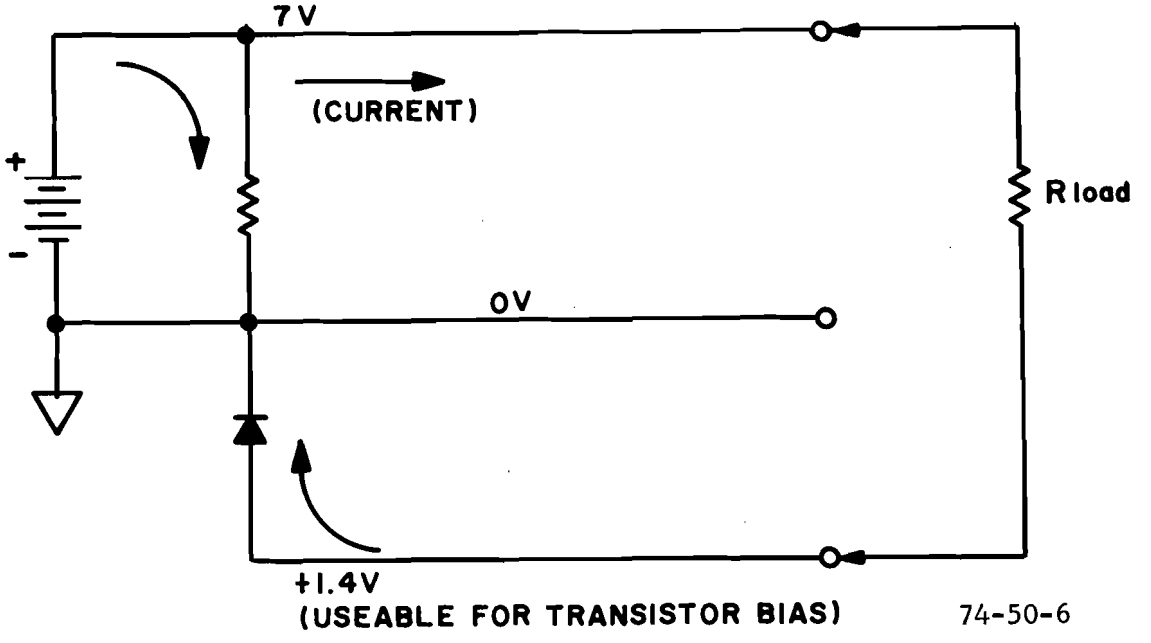
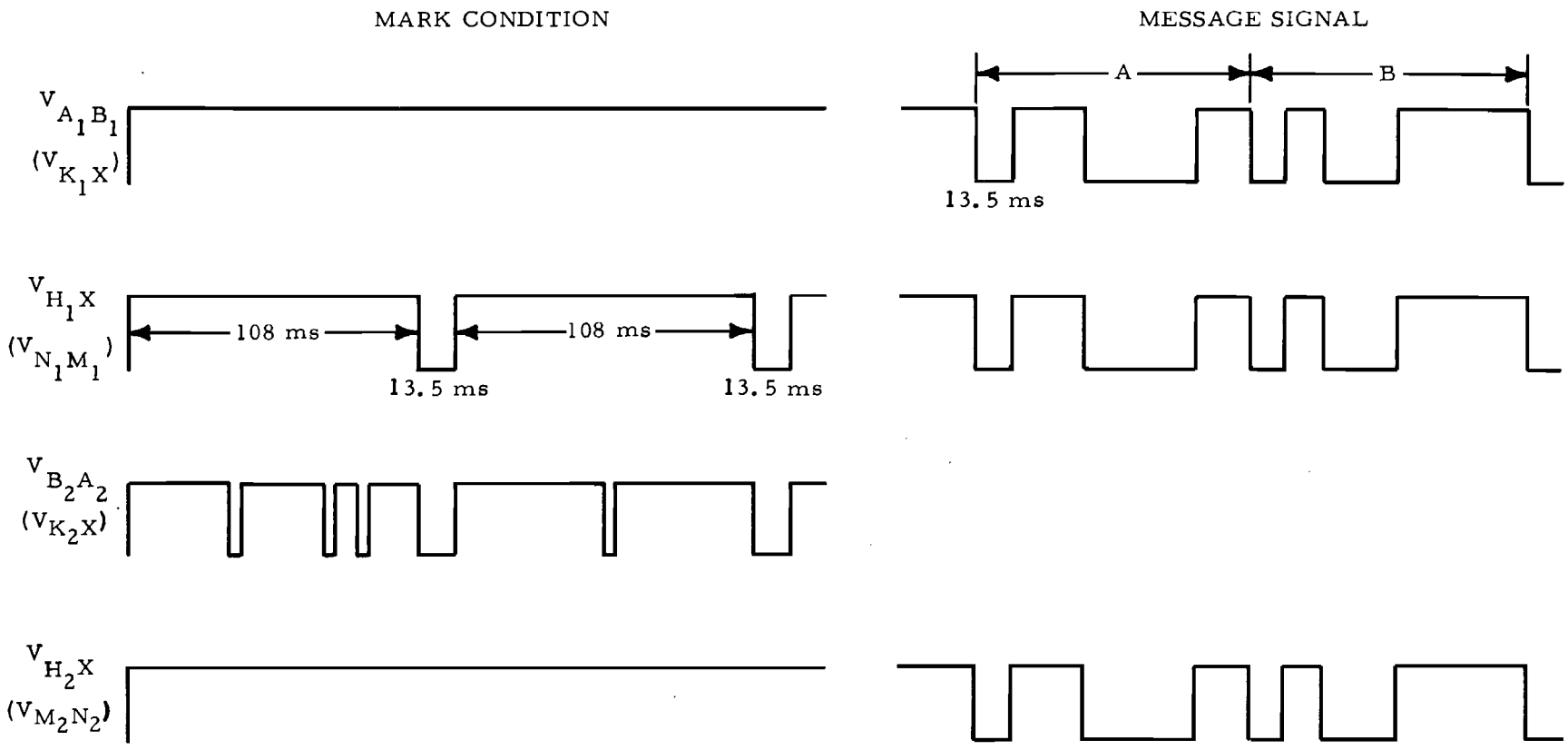


FIGURE 6. SIMPLIFIED POWER SUPPLY EQUIVALENT



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NOTE: NUMBERS 1 AND 2, SUBSCRIPTS WITH LETTERS, REFER TO STATION OF FIGURE 1.

X REFERS TO 1.4-VOLT COMMON

FIGURE 7. WAVEFORMS AT SIGNIFICANT POINTS OF FIGURE 1 CONFIGURATION

At $V_{B_2A_2}$, the waveform is shown with interruptions of brief durations, assumed to be introduced in transit, which the CLD receive device eliminates along with the deliberate 13.5-ms spaces in order to deliver a continuous mark at H_2X for the printer to avoid continuous mechanical motion corresponding to letter shift.

On the right-hand half of figure 7 is shown an interjection of characters A and B of a message signal. If a first character starts anywhere in time, such that its start space is initiated during the 108-ms mark period corresponding to V_{H_1X}, the 13.5-ms interruption will not occur, and the character will appear exactly at V_{H_1X}. The waveform at V_{H_2X} should therefore be the message signal which will also appear at $V_{M_2N_2}$ for the printer.

In employing an idle signal as described here, a steady mark or open condition corresponds to a malfunction. An alarm system is therefore to be included such that a mark condition longer than that of the idle signal (108 ms) or an open condition for longer than that of a blank character (6 times 13.5 ms, or 81 ms) will trigger a visual and/or audio warning signal. This is not critical, and a period of about 200 ms for each condition is completely suitable, and there will be no likelihood of false alarms.

IMPLEMENTATION.

SEND CLD. As shown in figures 1 and 7, the send CLD device when receiving a continuous mark should produce what is tantamount to a letters-shift character and otherwise deliver the message signal when present.

Time was spent designing and building breadboards employing commercial monolithic timer and retriggerable monostable multivibrator chips (integrated circuits) which, unfortunately, proved erratic and troublesome in this application for both this and the receive CLD.

The circuit finally adopted for the send CLD, without the alarms, is shown in figure 8. Waveforms at significant points are shown in figure 9.

The 4011 consists of four positive logic "NAND" units, two of which are employed as negative logic "NOR" as shown in figure 8.

To analyze the operation of this circuit, K_1 will first be assumed low. Therefore, the 5-volt B+ is conducting through the 30K resistor, and a net low exists at input 2 of the CD4011AE. Hence, 3 is high and C_1 is charged. Therefore, 5 and 12 are high, and 4 and 11 are low. Since 4 is low, the input to the 2N3646 amplifier is also low, it is therefore nonconducting, and pin 1 (to the 7408 "AND" unit) is high and also pin 1 of the CD4011AE. Since K_1 is low and also applied to pin 2 of the 7408 "AND", H_1 will be low also. This condition, corresponding to the first time segment shown for V_{K_1X} on the left half of figure 9, is illustrated for the successive significant points of this CLD send circuit.

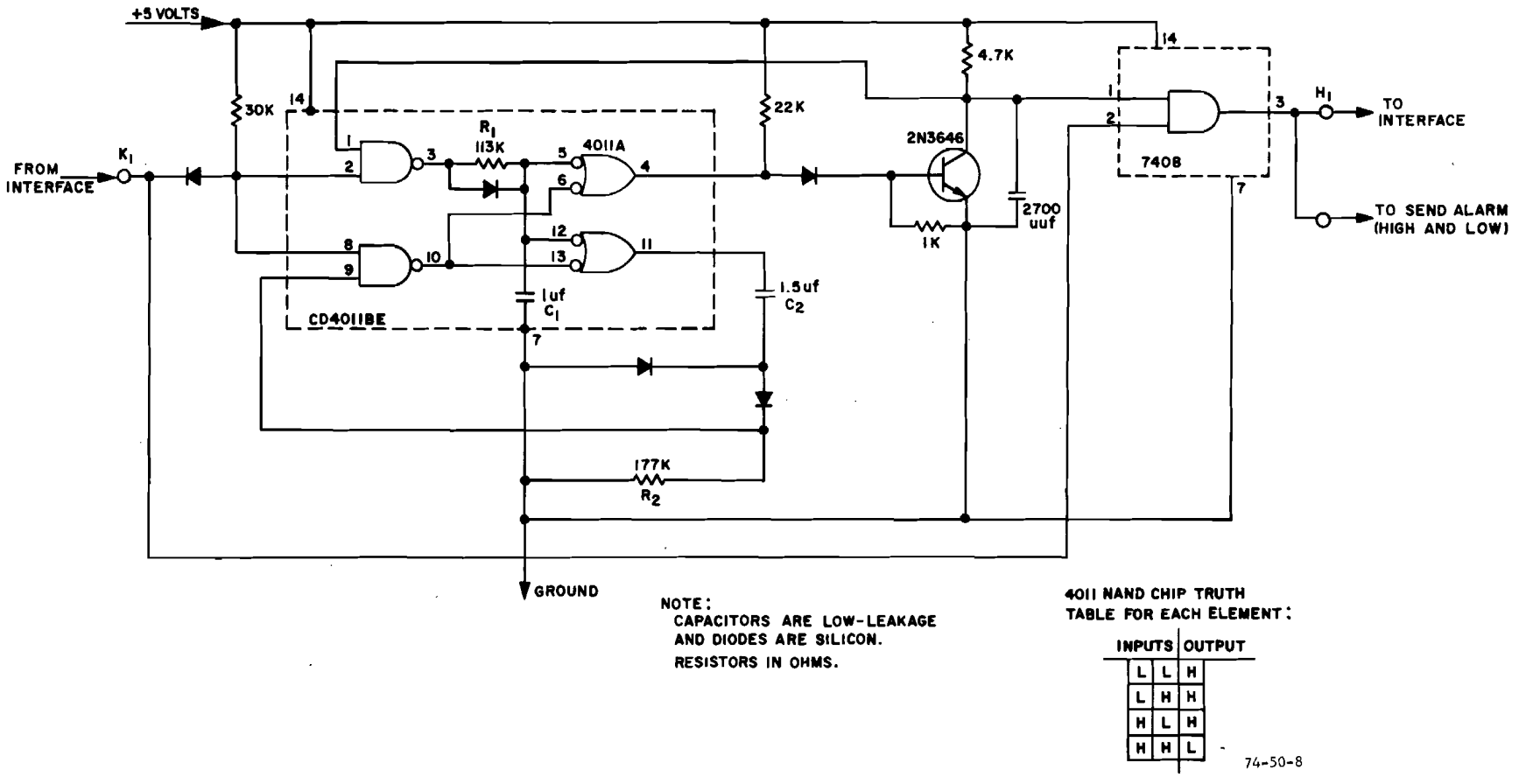

FIGURE 8. CLD SEND CIRCUIT WITHOUT ALARMS (STATION 1)

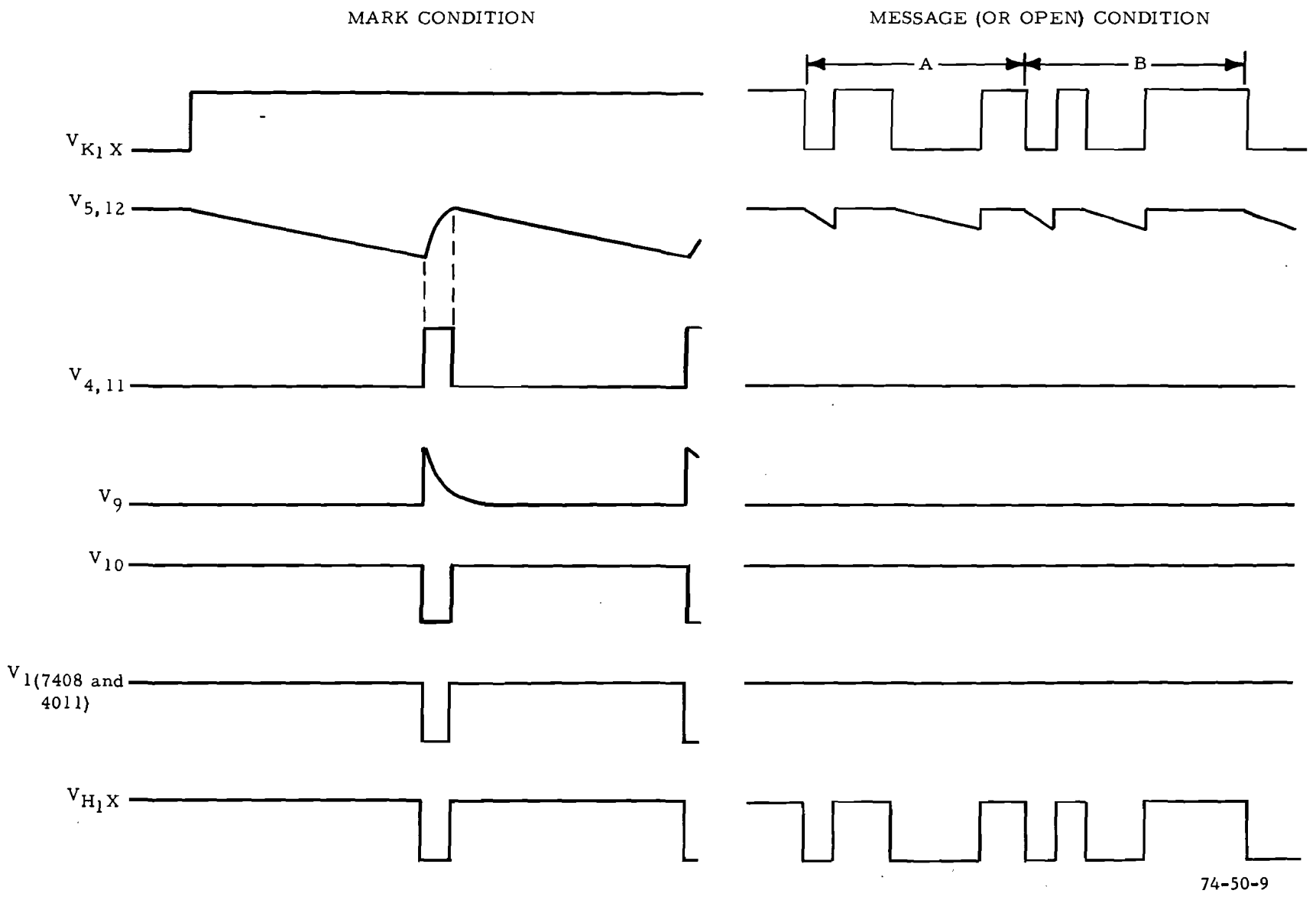

FIGURE 9. WAVEFORMS AT SIGNIFICANT POINTS OF SEND CLD CIRCUIT

When K_1 goes high to a mark condition as shown in figure 9 (left side), then pin 3 will become low and so will 5 and 12. It is to be noted, however, that time is taken for 5 and 12 to become sufficiently low, which is determined by the time constant R_1C_1. The components chosen correspond to an interval of 108 ms. If K_1 should become low, such as for a message, before 108 ms elapsed, then 5 remains high, 4 low, and pin 1 of the 7408 high. The output H_1 therefore corresponds to whatever is at K_1. However, should K_1 remain high for more than 108 ms, such as for a continuous mark (no message) condition, then 5 and 12 become sufficiently low, and 4 and 11 high (since 13 and 6 are normally low). Pin 4 high causes conduction of the 2N3646 and thereby renders pin 1 of the 7408 "AND" low. Hence, H_1 will become low. The high appearing at pin 11 will start to charge C_2 and place a high on "NAND" input 9 which will drop back to a low after an interval determined by product R_2C_2 which has been chosen for 13.5 ms. At the end of this interval, when pin 9 is low again, pin 10 will again be high, 4 low, 7408 "AND" 1 high, and for the continuous mark condition at K_1, 7408 "AND" 2 also high. Hence, H_1 will resume a high. The output of the send CLD unit for a continuous mark input will be a high interrupted at 108-ms intervals by a 13.5-ms low, which provides an effectual letters-shift character as an idle signal.

RECEIVE CLD. The circuit adopted for the receive CLD is shown in figure 10. Waveforms at significant points are shown in figure 11. Looking first at the left half of the latter figure, it is noted that V_{L_2X} is low when V_{K_2X} is high, corresponding to a mark line condition at A_2B_2. (The subscript "2" referring to the second station). The brief unwanted interruptions are shown here as spikes. These are eliminated by the action of the SN7408N.

The method employed to eliminate the spikes constitutes a basic technique used elsewhere in this CLD and for the alarms and is described below. The SN7408N contains four "AND" units, one of which is shown in use in figure 10. When a pulse is applied to the input of receive CLD at point L_2, it is also simultaneously applied to input 2 of the 7408 "AND" unit. This input is also applied to input 1 of the "AND" unit through a resistor (15k in this case) at its junction with a capacitor (3 microfarads (μF) to ground. Since a high output at 3 of the "AND" requires highs simultaneously at both the 1 and 2 inputs there will be no output until point 1 becomes sufficiently high. This will occur at some time interval after the high occurs at L_2, a time which is determined by the product of resistance and capacitance values when the capacitor has become sufficiently charged. In this case, input 1 will take approximately 4 ms to become high. (The 15k resistor is shunted by a diode to enable discharge of the capacitor when L returns to low.) Therefore, pulses of less than 4 ms will be eliminated since, when input 1 has become high, input 2 will have dropped to a low. Their elimination is shown for V_3 of figure 11. It should be noticed, however, that the normal 13.5-ms pulse will be narrowed by 4 ms, as shown, but this has no effect on the message signal which is applied to the "OR" output unit (SN7416) directly from K_2 (which is $\bar{L}_2$).

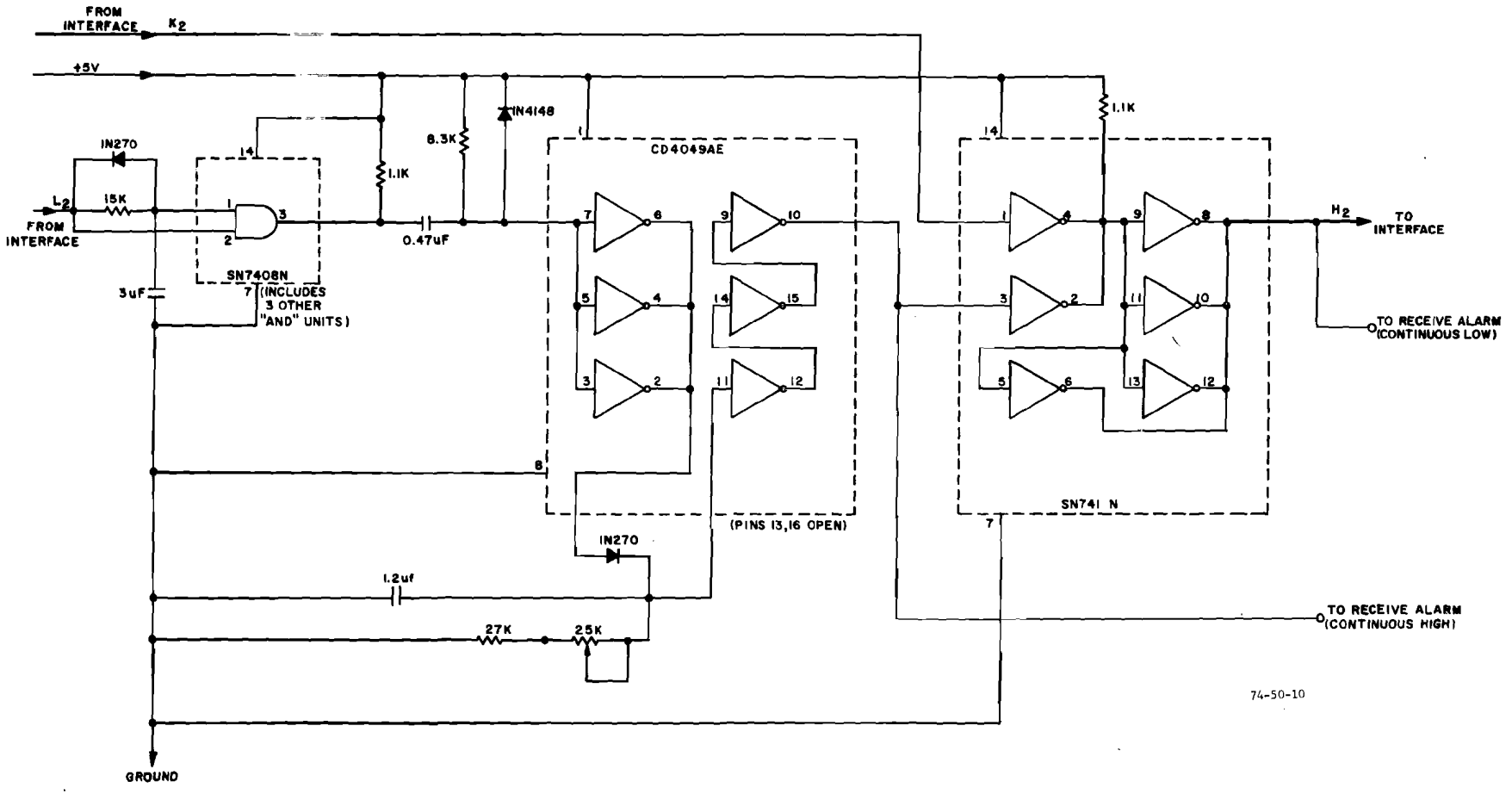

FIGURE 10. CLD RECEIVE CIRCUIT WITHOUT ALARMS (STATION 2)

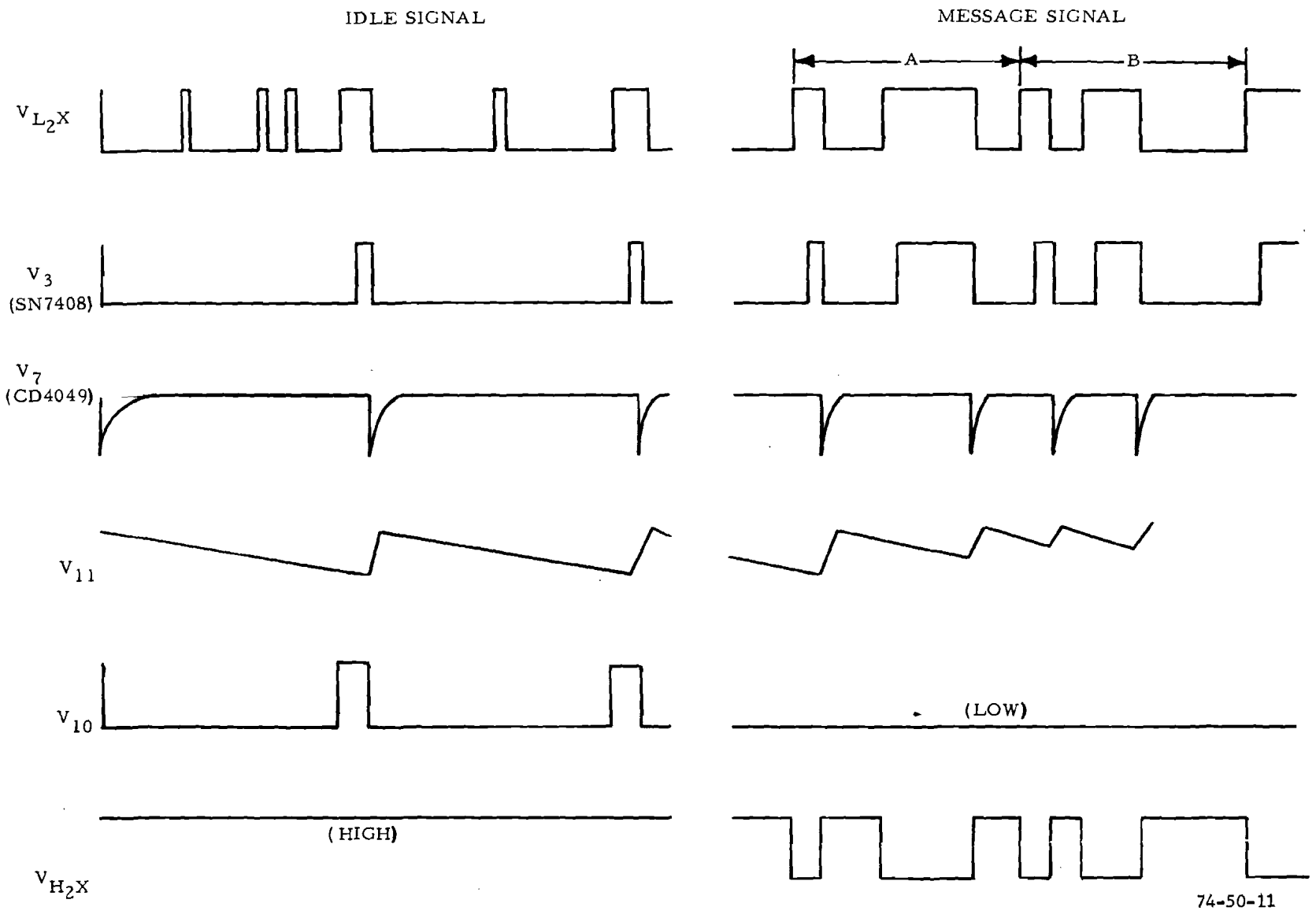

FIGURE 11. WAVEFORMS AT SIGNIFICANT POINTS OF RECEIVE CLD CIRCUIT

The output 3 of the SN7408 is applied to an amplifier (CD4049AE) through a coupling capacitor (0.47 μF) such that the net voltage to the amplifier is low when 3 is high and instantaneously becomes minus when 3 becomes low, but is restored to low when the 0.47-μF capacitor is discharged. This is shown as V_7 in figure 11.

The CD4049 amplifier units are connected as shown, the first three are in parallel to provide sufficient current to charge the 1.2 μF output capacitor. This voltage buildup occurs within the interval of a positive spike corresponding to V_7 (not shown), and the capacitor then discharges as shown for V_{11} in figure 11.

The sawtooth into 11 of the CD4049 amplifier causes conduction and a low output from 12 which is cut off at a point where the sawtooth voltage amplitude becomes too low to support conduction. This results in a square pulse which is amplified by the next two stages and is shown as V_{10} in figure 11.

The output of V_{10} is applied to an input of an SN7416N used as an OR followed by four shunted amplifiers. These positive pulses correspond to the negative pulses of $K_2(\overline{L_2})$ and the output at H_2 stays high. Therefore, an idle signal to the receive board maintains a high at H_2 and a mark condition for the printer as specified. (The four shunted amplifiers accommodate the comparatively low impedance of H_2.)

When a message arrives, pulses are always spaced closer together than the idle pulses. As shown for V_{11}, the sawtooth is initiated more frequently, and the capacitor (1.2 μF) never discharges sufficiently to be at a voltage level low enough to cut off the amplifier. Hence, the V_{10} output is a constant low, and the message signal waveform, appearing at K_2, will be the only signal at H_2. The waveform at H_2 will be identical to that at K_2 (since two amplifier stages comprise a double inversion). A low at K_2 causes the four shunted amplifiers to conduct and thereby drops the voltage at H_2 to the extent of its source impedance, compared to the combined amplifier impedance.

ALARMS. Since in normal operation there will be either a message or idle signal, a continuous high or low out of certain stages of the send and receive CLD's indicates a faulty condition in the CLD's or elsewhere.

For the send CLD, either a continuous low or high at H_1 comprises a faulty condition. H_1, being the output of the send board, is preferable over other send CLD points since malfunctions within any part of this unit will be encompassed.

For the receive CLD, a continuous low or high at K_2 comprises a faulty condition. However, K_2 is at the entry of the CLD and does not reflect the condition of the CLD. A continuous low at H_2 is a faulty condition, and the low alarm is taken from here. However, the continuous high-fault condition cannot be

taken at this point since that is normal for the idle signal condition. This, therefore, is taken at the output of the 4049 amplifier (pin 10 of figure 10) which is the input to the OR (of the SN7416N) and should be either continuously low or periodically pulsed for idle signal.

The alarms circuit is shown in figure 12. This unit employs an alarm for a steady high and one for a steady low. This particular device employs a light-emitting diode (LED) for each condition. One unit will be incorporated with the CLD send and one with the CLD receive unit.

Operation can be described by examining the steady high alarm shown in the upper portion of figure 12. Using the method described above, a high condition applied to input pin 1 of 4011 will not appear on input pin 2 until it persists for approximately 200 ms, a time which is determined by the product R_1C_1. For the steady high condition, therefore, the output 3 of this AND input device will go low. Thereafter, successive amplifiers in the 4011, 4049, and 7417 and inversion in the first two will provide a low at the output (pin 2 of the 7417) which can deliver the 30 mA needed to light the LED.

The lower circuit, for the steady low condition, is identical except that it has an extra amplifier stage (input 14 of the 4049) to invert the low. Therefore, when the LED glows it corresponds to a steady low input condition.

SYSTEM EMPLOYED. During the course of designing, developing, and testing the CLD, only one teletypewriter was available. The signal was therefore sent from the TD to the printer of the same unit. Figure 13 is a photograph of the setup. Only one alarm, labeled "send alarm," is shown. This was also used with the receive board when desired. The alarm unit in each case is identical, and in practice, the CLD send and receive would each have its own alarms as an integral part of each unit.

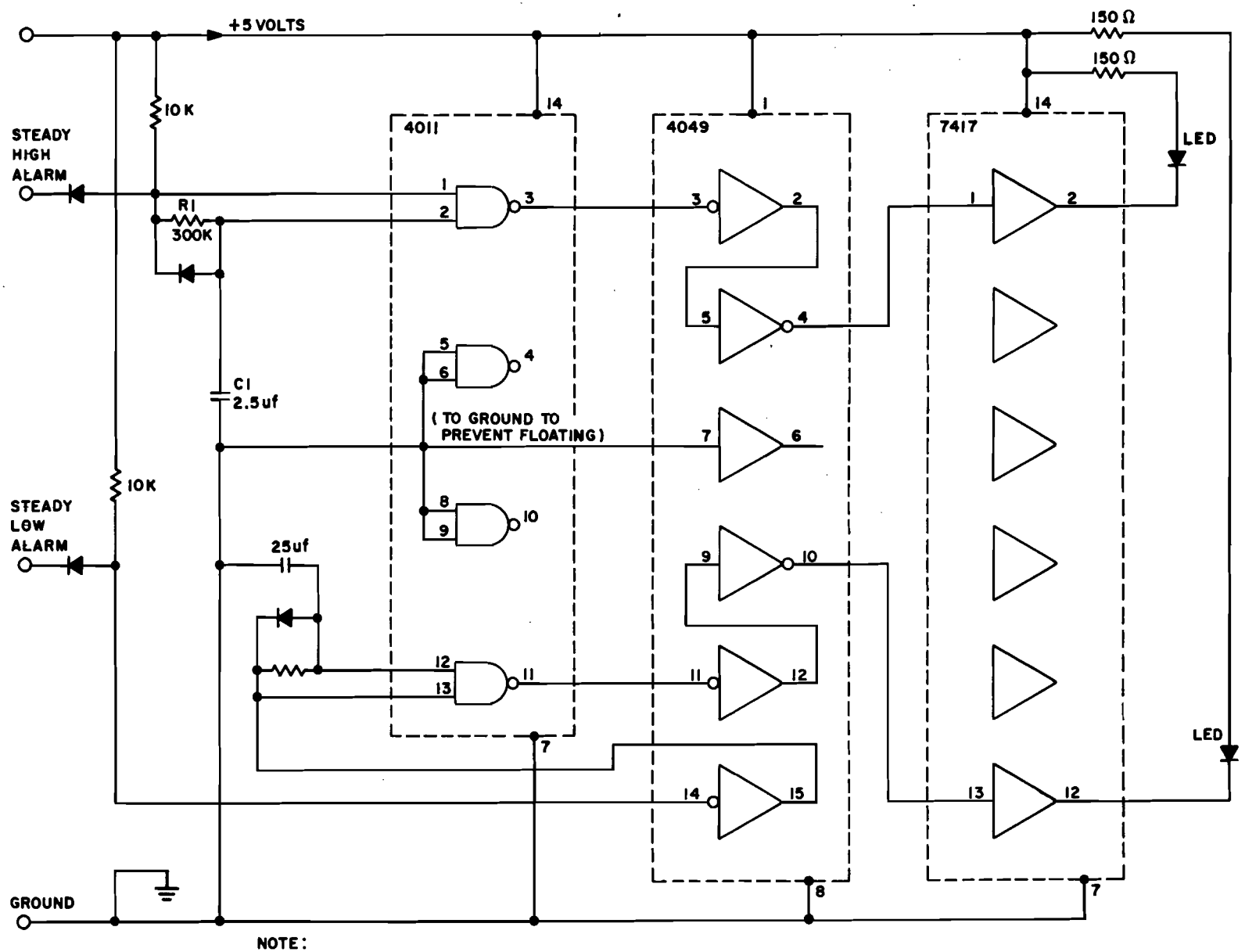

FIGURE 12. ALARM UNIT FOR SEND OR RECEIVE CLD

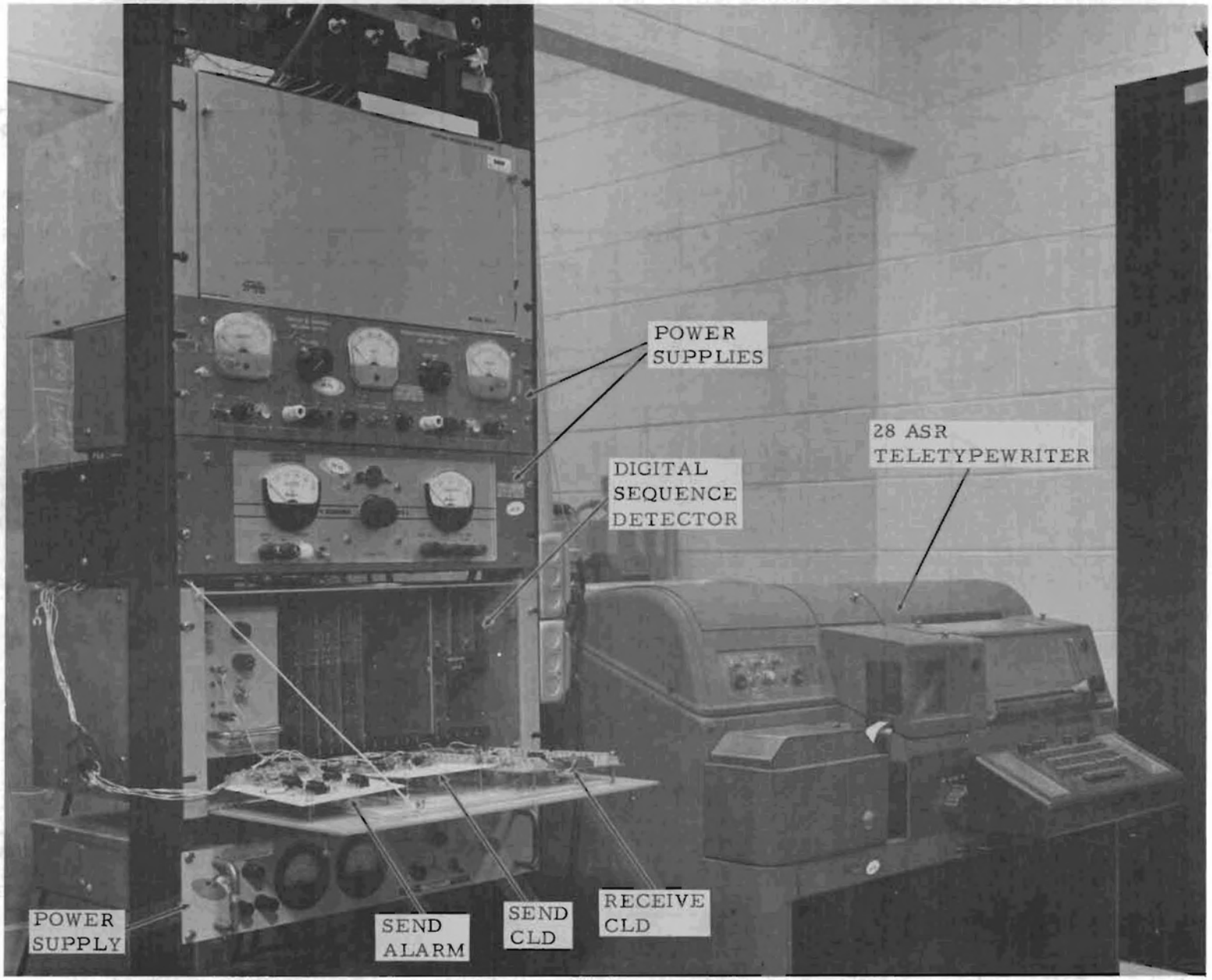

FIGURE 13. INITIAL ONE-STATION BREADBOARD SETUP

RESULTS

The CLD performed as described for its design. A continuous mark at the TD resulted in a mark condition at the receive printer, as it should.

An open at the TD results in the steady low alarm LED for the send unit lighting. This condition or an open line between interfaces results in the steady high alarm associated with the receive unit lighting. This alarm also responds to a steady mark condition into the receive unit.

The other two alarms, steady high at send output and steady low at receive output, respond to other malfunctions; for example, the send steady high alarm light if 4011 is removed (thereby incapacitating idle signal generation).

When the start bit of the first character of a transmitted message coincidentally begins during the bit of the idle signal, the first character transmitted out of the CLD send unit can be other than the one from the TD. The space of the idle signal will act as a start bit, and the start bit of the signal will act as the first level, etc. For example, an A character is conprised of marks in the first two levels, but may now become that character having marks in the 2nd and 3rd levels, namely I. B can become an L. If this takes place when the beginning of the character start space occurs at least halfway after the idle space started, then the theoretical probability of this occurring is approximately only 1 out of 18 starts. (This is calculated by relating the approximately half-bit range, when it can occur, to the total idle signal range of a 108-ms mark interval plus the one space interval.)

Tapes were run which had each character repeated three times, with separations between the different character sets as blanks. The three identical characters were invariably reproduced, but an extra character was added before and/or after the character set for about 20 percent of the total of set beginning and end positions. However, this can be reduced, and there is no reason why the idle signal pulses shouldn't be separated further (and the time to trigger alarms made longer if necessary). A much more satisfactory value found was 180-ms separation between idle pulses, which is accomplished by appropriate circuit change of R_1/C_1 in figure 8.

However, a local FSS responded to inquiry that the practice is to use three successive letter shifts before each message and four letter "N's" followed by a line feed and two carriage returns after the message. A check with New York IFSS indicated that that practice is standard, the same as domestic. This practice would isolate the message itself from these effects. The "range finder" (which determines the angular position at which the cam-clutch stops with respect to the selecting levers) on the printer was varied and the range of 15 to 100 was found uniformly free of introduced printing distortion.

The unit, as developed at NAFEC, is a breadboard device which demonstrates feasibility. Actual field test could assure that the functional performance is that actually required. Based on parts employed, and considering needed refinements such as printed circuitry and labor, it is estimated that the cost of mass-producing the CLD for each station (including power supply and interfaces) would be a few hundred dollars.

CONCLUSIONS

It is concluded that:

1. The model channel-loss detector (CLD) described here satisfactorily meets all the basic functional requirements set forth.

2. The CLD (which should include interfaces and power supply all in one physical unit) as designed and developed should be reliable, small in size (total not more than 200 cubic inches), and can be installed externally.

RECOMMENDATIONS

It is recommended that:

1. The power supply should provide +5.5 and +1.5 volts, with a ground common to both of them.

2. CLD prototype units should be checked in the field prior to writing of production specification and quantity procurement.