COPY 3 Report No. FAA-RD-76-224

WIDE APERTURE (DIGITAL) VOR

Girt C. Kundzins
Albert S. Palatnick

AIL, a division of CUTLER-HAMMER
Deer Park, New York 11729

NAFEC
LIBRARY
MAR 21 '77

Final Report
August 1976

Document is available to the public through the
National Technical Information Service,
Springfield, Virginia 22161

Prepared for

U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINSTRATION
Systems Research & Development Service
Washington, D.C. 20590

NOTICE

This document is disseminated under the sponsorship of the Department of Transportation in the interest of information exchange. The United States Government assumes no liability for its contents or use thereof.

Technical Report Documentation Page

1. Report No. FAA-RD-76-224	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle WIDE APERTURE (DIGITAL) VOR SYSTEM		5. Report Date SEPTEMBER, 1976
		6. Performing Organization Code
7. Author(s) GIRT C. KUNDZINS / ALBERT S. PALATNICK		8. Performing Organization Report No. A414-F
9. Performing Organization Name and Address AIL, A DIVISION OF CUTLER-HAMMER DEER PARK, LONG ISLAND, NEW YORK 11729		10. Work Unit No. (TRAIS)
		11. Contract or Grant No. DOT-FA73WA-3169
12. Sponsoring Agency Name and Address DEPARTMENT OF TRANSPORTATION FEDERAL AVIATION ADMINISTRATION 800 INDEPENDENCE AVENUE, S.W. WASHINGTON, D.C. 20590		13. Type of Report and Period Covered PHASE I FINAL REPORT
		14. Sponsoring Agency Code ARD-331
15. Supplementary Notes		

16. Abstract

THIS REPORT COVERS THE DESIGN, DEVELOPMENT, AND FIELD TESTING OF A WIDE APERTURE DIGITAL VOR SYSTEM. THE VOR GROUND STATION IS IN THE FORM OF 8 CROSSED BASELINE PAIRS OF INTERFEROMETERS. EACH OF THE INTERFEROMETERS PAIRS IS ENERGIZED SUCCESSIVELY BY A SET OF PULSES AND PHASE SHIFTS. THE AIRBORNE RECEIVER DECODES THE SIGNALS FROM EACH OF THE INTERFEROMETERS. THIS SET OF MEASUREMENTS ON EACH AXIS PERMITS COMPLETE RESOLUTION OF AMBIGUITIES AND THE PRECISE CALCULATION OF THE ANGLE WITH RESPECT TO THE STATION.

THE OBJECTIVE OF THIS WORK WAS THE DEVELOPMENT OF A SYSTEM THAT WOULD SIGNIFICANTLY REDUCE MAGNITUDE OF SITING ERRORS, PROVIDE GREATER ACCURACY AND UTILIZE DIGITAL TECHNIQUES TO SIMPLIFY PROCESSING. FIELD TESTS OF THE FEASIBILITY MODEL INDICATE IT IS A HIGH PERFORMANCE SYSTEM CAPABLE OF ACHIEVING AN ORDER OF MAGNITUDE IMPROVEMENT IN BOTH SITE ERROR REDUCTION AND IN ACCURACY COMPARED TO PRESENT VOR SYSTEMS. THE MEASURED ACCURACIES WERE 0.11° STANDARD DEVIATION.

17. Key Words Air Navigation VOR Systems Digital VOR Wide-aperature VOR Precision VOR	18. Distribution Statement Document is available to the public through the National Technical Information Service, Springfield, Virginia 22161.

19. Security Classif. (of this report) UNCLASSIFIED	20. Security Classif. (of this page) UNCLASSIFIED	21. No. of Pages 100	22. Price

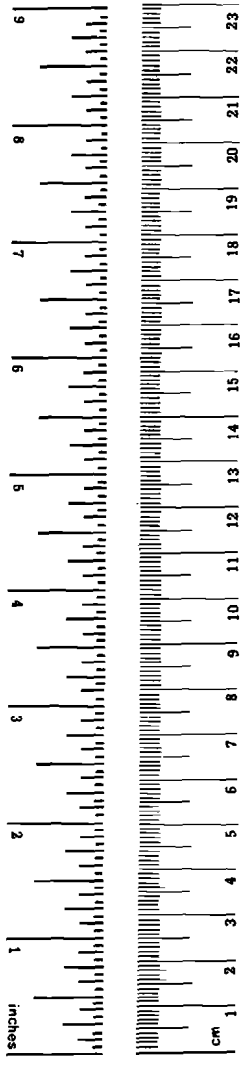
Form DOT F 1700.7 (8-72) Reproduction of completed page authorized

METRIC CONVERSION FACTORS

Approximate Conversions to Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
in	inches	*2.5	centimeters	cm
ft	feet	30	centimeters	cm
yd	yards	0.9	meters	m
mi	miles	1.6	kilometers	km
		AREA		
in^2	square inches	6.5	square centimeters	cm^2
ft^2	square feet	0.09	square meters	m^2
yd^2	square yards	0.8	square meters	m^2
mi^2	square miles	2.6	square kilometers	km^2
	acres	0.4	hectares	ha
		MASS (weight)		
oz	ounces	28	grams	g
lb	pounds	0.45	kilograms	kg
	short tons (2000 lb)	0.9	tonnes	t
		VOLUME		
tsp	teaspoons	5	milliliters	ml
Tbsp	tablespoons	15	milliliters	ml
fl oz	fluid ounces	30	milliliters	ml
c	cups	0.24	liters	l
pt	pints	0.47	liters	l
qt	quarts	0.95	liters	l
gal	gallons	3.8	liters	l
ft^3	cubic feet	0.03	cubic meters	m^3
yd^3	cubic yards	0.76	cubic meters	m^3
		TEMPERATURE (exact)		
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

*1 in = 2.54 (exactly). For other exact conversions and more detailed tables, see NBS Misc. Publ. 286, Units of Weights and Measures, Price $2.25, SD Catalog No. C13.10:286.



Approximate Conversions from Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
		LENGTH		
mm	millimeters	0.04	inches	in
cm	centimeters	0.4	inches	in
m	meters	3.3	feet	ft
m	meters	1.1	yards	yd
km	kilometers	0.6	miles	mi
		AREA		
cm^2	square centimeters	0.16	square inches	in^2
m^2	square meters	1.2	square yards	yd^2
km^2	square kilometers	0.4	square miles	mi^2
ha	hectares (10,000 m^2)	2.5	acres	
		MASS (weight)		
g	grams	0.035	ounces	oz
kg	kilograms	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	
		VOLUME		
ml	milliliters	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
l	liters	0.26	gallons	gal
m^3	cubic meters	35	cubic feet	ft^3
m^3	cubic meters	1.3	cubic yards	yd^3
		TEMPERATURE (exact)		
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F

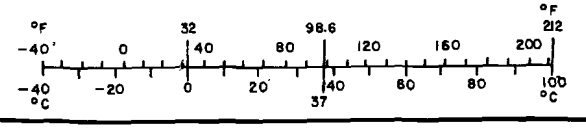


TABLE OF CONTENTS

SECTION	TITLE	PAGE
1.0	INTRODUCTION	1-1
	1.1 PROGRAM SUMMARY	1-3
	1.2 BASIC PRINCIPLES OF OPERATION	1-5
2.0	HARDWARE DEVELOPMENT	2-1
	2.1 TRANSMITTING ANTENNA ARRAY	2-4
	2.2 GROUND STATION RF UNIT	2-5
	2.3 GROUND STATION CONTROL UNIT	2-7
	2.4 AIRBORNE EQUIPMENT	2-13
3.0	FIELD TEST PROGRAM	
	3.1 INSTALLATION AND PRELIMINARY CHECKS	2-1
	3.2 DATA PROCESSING AND TEST INSTRUMENTATION	3-2
	3.3 TEST RESULTS	3-3
	3.4 TEST ANALYSIS	3-5
4.0	CONCLUSIONS AND RECOMMENDATIONS	4-1

LIST OF ILLUSTRATIONS

FIGURE NO.	TITLE
1-1	BASIC THREE ELEMENT INTERFEROMETER
1-2	RECEIVED CODING WAVEFORMS
1-3	TRANSMITTER WAVEFORMS
2-1	GROUND STATION GENERAL BLOCK DIAGRAM
2-2	GROUND STATION EQUIPMENT FAMILY TREE
2-3	RF UNIT
2-4	CONTROL UNIT
2-5	AIRBORNE UNITS WITH COVERS REMOVED
2-6	AIRBORNE EQUIPMENT BLOCK DIAGRAM
2-7	AIRBORNE EQUIPMENT FAMILY TREE
2-8	DIGITAL VOR ANTENNA BASE LAYOUT
2-9	RF UNIT BLOCK DIAGRAM
2-10	GROUND CONTROL UNIT BLOCK DIAGRAM
2-11	COUNT CONTROL AND DECODER BLOCK DIAGRAM
2-12	COUNT CONTROL AND DECODER PC BOARD NO. 1
2-13	COUNT CONTROL AND DECODER PC BOARD NO. 2
2-14	BUILT IN TEST GENERATOR BLOCK DIAGRAM
2-15	BUILT IN TEST GENERATOR PC BOARD
2-16	PULSE COUNT MONITOR BLOCK DIAGRAM
2-17	SWITCH MONITOR BLOCK DIAGRAM
2-18	SWITCH MONITOR PC BOARD
2-19	AIRBORNE PROCESSOR BLOCK DIAGRAM
2-20	PULSE DECODER BOARD
2-21	AMBIGUITY RESOLVER BOARD
2-22	CALCULATOR BOARD
2-23	BEARING BOARD
2-24	DEVIATION BOARD
2-25	INTERFACE BOARD
2-26	TIMING AND CONTROL BOARD
2-27	PULSE DECODER BLOCK DIAGRAM
2-28	PULSE DECODER SIGNAL WAVEFORMS
2-29	DATA AVERAGER - AMBIGUITY RESOLVER BLOCK DIAGRAM
2-30	BEARING CALCULATION BLOCK DIAGRAM
2-31	BEARING ANGLE "A" AS A FUNCTION OF γ
2-32	DEVIATION COMPUTATION BLOCK DIAGRAM

LIST OF ILLUSTRATIONS (CONT)

FIGURE NO.	TITLE
3-1	GROUND STATION
3-2	TRANSMITTING ANTENNA
3-3	TYPICAL COMPUTER PRINT OUT
3-4	12 MILE ORBIT ERROR CURVE
3-5	6 MILE ORBIT ERROR CURVE
3-6	RADIAL ERROR CURVE
3-7	60/66 AZIMUTH SECTOR ERROR CURVE
3-8	178/184 AZIMUTH SECTOR ERROR CURVE
3-9	222/229 AZIMUTH SECTOR ERROR CURVE

1.0 INTRODUCTION

Several types of VOR have been developed during the last thirty years; (1) the conventional VOR; (2) the Doppler VOR; (3) the precision multilobe VOR; and (4) the precision Doppler VOR. VOR receivers, now in aircraft, receive the signals from all of the four kinds of VOR facilities. However, to gain the maximum benefits from the precision multilobe VOR and the precision Doppler VOR, special signal processing must be performed that is beyond the capabilities of the present day VOR receivers. Also, in order to use the present VOR bearing information, digital airborne equipment require an analogue to digital conversion.

The purpose of the VOR, described in this report, was the development of a system greatly superior to any so far developed. The objectives were to reduce siting errors by an order of 1/10th of those in present use, provide about 10 times more accuracy, and utilize digital techniques to simplify signal processing.

Phase I work has led to the development of a feasibility model Wide Aperture Digital VOR system that was flight tested to determine its basic performance characteristics. The results of these tests has demonstrated it is a high performance system capable of achieving a 10 fold improvement in both accuracy and site error reductions as compared to previously developed VOR systems. These tests indicated that the overall system accuracy, including ground station and receiver errors as well as error contributions by the data acquisition, data reduction and EAIR tracking system is 0.11 degrees standard deviation. Therefore, the basic objective of this program to develop a VOR greatly superior to any so far developed has been achieved.

Development of the ground station electronics and the airborne decoders followed an approach based on the crossed pair interferometer principle. This is the most efficient way to use a given size aperture while requiring a minimum number of elements. Eight crossed pair interferometers are energized successively by a set of pulses

and phase shifts. The time multiplexed signal detected by the airborne receiver is processed in a form, whereby a simple digital computer performs the calculations necessary to define angular coordinates. An entire Wide Aperture Digital VOR system was installed and flight tested at NAFEC, Atlantic City, New Jersey.

This report describes the principles of the system, it summarizes the equipment design and includes block diagrams and photographs of all boards and ground station and aircraft equipment; and discusses and analyzes the performance data gathered during the field testing.

1.1 PROGRAM SUMMARY

The flight tests of the Feasibility Model of the Wide Aperture Digital VOR system showed it is greatly superior to any VOR so far developed. Its improvement is brought about by the combination of using an antenna aperture of 275 feet with digital techniques. The large aperture has increased accuracy by 10 times, while the digital generation of transmitted signals and consequent digital signal processing results in a simpler and inherently more stable receiver.

Although siting error tests were not included in this test phase, it follows that the increased aperture will reduce effects of siting errors by an order of magnitude. The usual errors associated with VOR systems due to receiver cross modulation, Doppler shifted carrier and counter poise modulation do not exist.

The pertinent characteristics of the feasibility equipment of the Wide Aperture Digital VOR are summarized.

(1) Measured Accuracy (includes the ground station, receiver, EAIR tracking radar and data reduction errors).

Mean 0.04°

Standard Deviation 0.11°

(2) Ground Station

RF Unit	10-1/2" high x 19" wide x 19" deep
Control Unit	10-1/2" high x 19" wide x 19" deep
Transmitting Antennas	17 Alford Loops
Aperture	275 feet

(3) Airborne Equipment

Conventional VOR Receiver (Collins 51R-3)

Processor Unit

Power Supply Unit

The Wide Aperture Digital VOR can be phased into operational use in a logical evolutionary development. Since it is compatible, it can be colocated with and made part of present VOR systems, sharing the same RF carrier. Since the precision information can be extracted from the audio detected at the IF output of any conventional VOR receiver, it retains full compatibility with existing receivers. No modifications are required to existing receiver circuitry, only an additional unit is needed.

Hence, the implementation of the Wide Aperture Digital VOR system can be phased into service gradually on an as-needed basis without affecting present day VOR usage.

1.2 BASIC PRINCIPLES OF OPERATION

The Digital VOR developed by AIL is based on a system of crossed wide-baseline interferometers; that measure directly the angles between the line of sight and each of the two baselines. The accuracy of an interferometer, neglecting instrumentation errors, but in the presence of some multipath reflection is directly related to the baseline separating the sources. However, if the baseline exceeds one wavelength, ambiguities exist. These are resolved through the use of additional interferometers, including one with a baseline of less than one wavelength. In principle, and if there are no multipath reflections, an interferometer of less than one wavelength baseline can resolve the ambiguities for any size aperture. Since the presence of some multipath was assumed, the resolution of ambiguities is done in steps of 4 to 1. The ground station uses a set of four interferometers on each axis with spacings of $\lambda/2$, 2λ, 8λ, and 32λ. An antenna located at the center radiates the station carrier.

The geometry of a pair of crossed interferometers does not have radial symmetry. The output is first derived as trigonometric functions of angles related to each of the baselines. The raw data is then processed by digital techniques to perform the calculations to extract the required angular coordinates.

The modulation method is similar in principle to that utilized successfully in CONSOLAN, an interferometer system with a long and successful record. Each of the eight interferometers is energized successively by a set of pulse and phase shifts. The set of four measurements on each axis permits complete resolution of ambiguities and the precise calculation of the angle with respect to the station.

The station carrier is modulated with a pulse train, a nominal 3.84KHz repetition rate during the interferometer transmission period and a 12.5KHz sinusoiadal signal during the "dead" time. The RF pulses are taken from a suppressed carrier modulator and applied to the elements of the interferometers in turn. The center element is energized with reference carrier only during the outer element excitation and with reference carrier modulated by a 12.5KHz sine wave during outer element "dead" times.

The relative phase of the outer elements of each of the interferometers is varied cyclically and in opposite directions. The receiver receives a series of positive (or negative) pulses followed by a series of negative (or positive) pulses. The main purpose of the pulse is to create the detectable dissymmetry that allows discrimination between positive (narrow) and negative (wide) pulses. The transition point between the two types of pulses is a function of the receiver's angular position (equal numbers of positive and negative pulses corresponds to a position where the signals from both elements of the interferometer are in phase). Each cycle of phase change has a specific number of pulses so that the angle measurement is made by pulse count.

As mentioned previously, the Digital VOR does not measure azimuth angle directly, but requires some computation to obtain true azimuth. Here we examine the geometry involved and show the nature of the computations that must be made. Assume that the antennas are disposed along two orthagonal baselines, one running in a north-south direction and one in an east-west direction. Let us denote the spherical coordinates by R, A, and E where R is slant range, A is the azimuth measured clockwise from north, and E is the elevation above the horizon. We have the relation:

$$X = R \text{ SIN } A \text{ COS } E$$

$$Y = R \text{ COS } A \text{ COS } E$$

$$Z = R \text{ SIN } E$$

Let us further denote the direction cosines

$$l = X/R = \text{COS } \alpha$$

$$m = Y/R = \text{COS } \beta$$

$$n = Z/R = \text{COS } \gamma$$

where α and β are the angles between the lines of sight and each of the two baselines, while $\gamma = \frac{\pi}{2} - E$ is the angle between the line of sight and the vertical. l and m are the quantities that are measured by the Digital VOR

system. A is obtained as follows:

$$\text{TAN } A = \frac{X}{Y} = \frac{R \times 1}{R \times m} = \frac{1}{m} = \frac{\text{COS } \alpha}{\text{COS } \beta}$$

so that

$$A = \text{TAN}^{-1} \frac{1}{m}$$

Consider a station consisting of three radiating elements equally spaced on a straight line as shown in Figure 1-1. Assume that the center element radiates a constant frequency carrier wave while the outer two elements radiate a series of pulses at the same frequency. Let the RF phase of the signal applied to the righthand element be advanced by an amount ϕ and let the phase of the signal applied to the lefthand element be retarded by the same amount. Also, assume that the receiver is located at a distance that is large compared to the baseline dimensions. The angle between the line of sight and the righthand extension of the baseline is defined as α. At the receiver then the signal from the righthand element will be advanced an amount

$$\Theta = (2\pi d/\lambda) \cos\alpha$$

due to the geometry of the situation and further advanced an amount ϕ due to the electrical phasing. The phase of the signal from the lefthand element will be equal and opposite. The total signal received is then:

$$E_R(t) = E_o \left\{ 1+M(t)[\exp j(\theta+\phi)+\exp -j(\theta+\phi)] \right\}$$
$$= E_o \left\{ 1+2M(t)\text{COS}(\theta+\phi) \right\}$$

where M(t), the modulating function, is a string of pulses.

It will be noted that if $\theta + \phi$ lies in the range between -90° and +90° so that the cosine is positive, the envelope will be modulated by a series of positive pulses. On the other hand, if the sum $\theta + \phi$ lies in the range between 90° and 270°, the envelope will be modulated by a series of negative pulses. If the parameters of the modulating pulse train are chosen appropriately, the positive pulses can be heard as a string of Morse code dots and the negative pulses can be heard as a string of Morse code dashes. If ϕ is fixed, there will be zones where dashes are heard and zones where dots are heard. Separating these zones will be rather sharply defined regions where the modulation vanishes and only unmodulated carrier is heard.

Suppose now that ϕ is slowly varied from zero to π radains. Depending on the value of θ we may hear a series of dashes followed by a series of dots or a series of dots followed by a series of dashes. For certain particular values of θ we may hear only dots or only dashes. Suppose that we hear dots first and then dashes as in Figure 1-2(a). At the instant when the dots vanish and the dashes have not yet commenced, we know that the sum $\theta + \phi$ is very nearly 90° plus or minus some multiple of 360°. Similarly, if we start with dashes and finish with dots as in Figure 1-2(b), we know that at the instant the modulation vanishes the sum $\theta + \phi$ is 270° plus or minus some multiple of 360°. If we know ϕ as a function of time then we can determine θ with a possible ambiguity of some multiple of 360°. If ϕ varies at a uniform rate and if the pulses also occur at a uniform rate, the measurement can be made by merely counting the number of dots and dashes and noting which are heard first.

Essentially, the Digital VOR coding system is that described above, with the phase ϕ varying from $-\frac{\pi}{2}$ through $\frac{\pi}{2}$. Although based on the same principles as CONSOLAN, the Digital VOR has significantly expanded capabilities. Two crossed baselines provide the requisite data which is generated at a much higher rate. The counting is done electronically and the ambiguity resolution is done automatically.

For the demonstration of Digital VOR system feasibility, as noted earlier, the element spacings are 1/2 wavelengths for the coarse pair, 2 wavelengths for the medium (intermediate) pair and 8 wavelengths for the fine pair, and 32 wavelengths for the superfine pair.

128 pulses at a repetition rate of 3.84KHz are generated for each complete rotation of $\emptyset$ through 2π radians, or 64 pulses for a $\emptyset$ change of π radians. Figure 1-3 shows the relative goniometer waveforms and transmission periods associated with each of the interferometers. The resolution is then 1 part in 64 for the direction cosine associated with each baseline. The actual scale factor is dependent on the angle, and has a maximum sensitivity at $\alpha = 90°$ (when $\cos \alpha = 0$). The superfine interferometer pair enables the system to achieve a scaling sensitivity of about 100 electrical degrees for an azimuth angle change of 0.01°.

2.0 HARDWARE DEVELOPMENT

In this section, the implementation of the Digital VOR is outlined. Simplified block diagrams are described and the required major assemblies and modules to implement the system are listed in associated Equipment Family Trees.

The ground station provides the aircraft with space angular information relative to each baseline; that is processed in the aircraft in terms of an azimuth angle relative to the ground station.

The ground station consists of three major sections:

- Transmitting Antenna Array
- RF Generation Unit
- Control Unit

Figure 2-1 shows the station block diagram and Figure 2-2 shows the associated Equipment Family Tree. The equipment units, (see Figures 2-3 and 2-4) are housed in rack mountable packages with identical outside dimensions of 10-1/2 inches high, 19 inches wide and 19 inches deep. During field tests, the units are mounted in a standard 19 inch equipment rack.

The Digital VOR signals are generated by the transmitter module and split via the power splitter into two lines - the carrier and sideband. The carrier is passed through a phaser unit and fed directly to the center (carrier) antenna. The phaser provides for field adjustment to phase match the carrier with the sideband signals.

The sideband signal feeds the goniometer which performs the required phase shifting when rotated. The goniometer is driven at a constant speed by the synchronous motor although its exact RPM is not critical as in the VOR or ILS. The goniometer outputs are at 90° relative phase at the bridge input to each other and are combined in a hybrid

bridge. Since one of the bridge legs contain an additional 180° phase shift, the bridge outputs are the sideband signals that rotate in phase opposition. The sideband signals are routed to the Control Unit which contains the RF switches. These switches, under direction by the Control Unit, perform a dual function. They route the RF signals to the appropriate antenna pair and provide the requisite pulse modulation of the RF signal.

The encoder generates the basic timing signals that are processed to provide the switch control and pulse modulation signals in the ground station.

The encoder provides basically two signals - a continuous pulse train of 128 pulses per revolution and a reference pulse generated once a revolution. The control logic processes the increment pulses to provide the control gates to step the switches in the proper sequence with the correct spacing between each step and complete frame scans. The reference pulse is utilized to both monitor the control logic and to provide the frame reset for every scan.

The control unit also contains modules for the purpose of monitoring the integrity of the station output signals; and to simplify routine troubleshooting and fault isolation.

The aircraft Digital VOR equipment processes the series of single cycle pulse modulates sinewaves to obtain the azimuth angular positions of the aircraft relative to the ground station.

The airborne units, see Figure 2-5, consists of four major sections:

- VOR Receiver
- Processor Unit
- Display Unit
- Power Supply

Figure 2-6 shows the aircraft equipment block diagram and Figure 2-7 shows the associated equipment family tree.

The conventional VOR audio output feeds the pulse decoder portion of the processor which determines the presence of pulses and their sign (width) - either positive (narrow) or negative (wide). The decoded pulses are routed to the appropriate registers corresponding to the specific transmitting interferometer pair and process the counts to resolve ambiguities. Next, the arithmetic unit calculates the aircraft azimuth bearing angle and provides the bearing direction information. The display unit visually shows the results of the arithmetic computation.

Additionally, for test monitoring and evaluation purposes, built-in monitor circuits are also provided. These are used not only to monitor equipment operation, but also provide data for the establishment of alarm and flag level criteria and a measurement of detailed system performance. The power supply unit consists of four commercial DC power supplies mounted on a common chassis.

2.1 TRANSMITTING ANTENNA ARRAY

Figure 2-8 shows the layout of the Digital VOR station which provides precision VOR service to suitably equipped aircraft. The precision VOR is based on the use of crossed baseline interferometers requiring 17 antenna elements. Four sets of interferometers on each baseline are used in addition to the center carrier antenna. The precise value of the distance between each antenna pair is set to be 0.5 λ for the inner pair, 2 λ for the next pair, 8 λ for the third pair and 32 λ for the outermost pair. The small (4 to 1) ration of baseline spacings ensures the integrity of the ambiguity resolution.

Each interferometer pair consists of two Alford loop antennas mounted on four foot pedestals and fed by two identical coaxial lines. The interferometers on one baseline must be fed $\lambda/2$ out of phase with respect to the interferometers on the other baseline. This is necessitated by the fact that the goniometer audio phase lags by 180 degrees during every second interferometer transmission (see Figure 1-3).

In order to minimize mutual coupling near the center of the array, the center antenna is raised 15-3/8 inches above the top of the sideband antennas. This height difference is also standard for the 5 loop VOR Alford Array. During the flight check phase of the program, it was noted that the orientation of the innermost sideband antennas did have an affect upon the induced currents in the nonradiating pair. For this reason, the antenna orientations were adjusted for minimum induced currents, which meant that the transmission line section of all loops, except for the inner North-South loops, pointed along the magnetic 315 degree radial. The inner North-South antennas were rotated by 90 degrees from this common position.

2.2 GROUND STATION RF UNIT

Figure 2-9 shows the RF unit block diagram and Figure 2-3 shows a photograph of the unit.

The VOR RF signals are generated by a standard AIL localizer transmitter module tuned to the VOR operating frequency. The unit is all solid state and provides a minimum of 20 watts power. In between sideband transmissions, modulated signals are obtained by the use of electronic keying of a tone oscillator. The tone on the RF carrier is obtained by amplitude modulating the transmitter during the "dead-time" between sideband transmissions. A Colpitts oscillator provides a 12.5KHz tone. It is gated by the same control pulses that set the state of the two 9 position antenna selector switches in the control unit. When these switches are in their "dummy load" position, the oscillator output is gated and amplified to modulate the RF transmitter output. The oscillator, gate control logic and audio power amplifier, are mounted on a single board assembled into the chassis of the RF unit.

The RF generated by the transmitter module is passed through a low pass filter into a power divider that consists of a coaxial TEE and a hybrid bridge. By varying the length of the coaxial lines feeding the bridge, it is possible to obtain the desired division of carrier to sideband power. The carrier is passed through a wattmeter element and a phaser unit before being fed to the center (carrier) antenna. The phaser provides for field adjustment to phase match the carrier with the sideband signals.

The sideband signal is routed through an isolator to the goniometer. Isolation of the sideband and carrier signals is required due to the mismatch that exists at the goniometer input. Without the isolator, this mismatch would cause a low level 30 hertz modulation of the carrier signal, which would introduce distortion at the receiver and affect system accuracy. The goniometer is driven at a constant speed by a synchronous motor although its exact RPM is not critical as in the VOR or ILS. The goniometer outputs are the sine and cosine functions varying at a 30 hertz rate. These are at 90° relative phase

at the bridge input due to an extra $\lambda/4$ line length in the sine function output leg. Since one of the bridge legs contains an additional 180° phase shift, the bridge outputs are the sideband signals that rotate in phase opposition. The sideband signals are fed to wattmeter elements after which they are routed to the Control Unit for switching.

The encoder, driven by the same synchronous motor as the goniometer, generates the basic timing signals that are processed to provide the switch control and pulse modulation signals in the ground station. This unit is a compact optical rotary incremental encoder that generates 256 continuous pulses per shaft revolution on one output and one pulse (zero reference) per shaft revolution on a second output. All encoder output pulses are TTL compatible. The encoder operates off a +5VDC supply located in the Control Unit.

The RF unit front panel contains a meter for monitoring the +28VDC supply and one common wattmeter for measuring either carrier, sideband I or sideband II powers. On ON/OFF circuit breaker controls, the application of 115VAC to the goniometer motor and the power supplies in both the RF and Control Units.

2.3 GROUND STATION CONTROL UNIT

Figure 2-10 shows a block diagram of the Control Unit and Figure 2-4 shows a photograph of the unit.

The encoder output is routed to the Count Control logic section which controls the status of the two 9 position Antenna Selector Switches, the two position RF Phase Control Switches, and the Pulse Count Monitor. The Decoder logic sequentically, via the Count Control, steps the antenna selector switch position and routes the sideband RF energy to the appropriate pair of antennas. For routine maintenance and initial installation adjustments, the antenna selector switch position is indicated by the illumination of associated lamps on the Control Unit front panel. Additionally, proper operation of the switch control logic is continuously vertified by the switch drive monitor. In the event of malfunction, the alarm lamp is illuminated. The Pulse Count Monitor counts and verifies that the correct number of pulses are produced for each complete transmission cycle. A positive indication is provided with the front panel indicator flashing on momentarily and then extinguishing at the start of the following cycle.

The two goniometer outputs are routed to the positive and negative sideband antennas through the phase control switches. During the pulse duration, the antennas are excited by an inphase RF signal. During the time between pulses, the Phase Control switches route the out-of-phase RF signal to the antennas. Each output port of the antenna control switch is passed through an RF detector. The detector output feeds a bank of test points on the front panel so that the signal to any one antenna can be visually monitored via an oscilloscope.

The Control Unit front panel is shown in Figure 2-4. The power ON/OFF switch turns on the local power supplies and also energizes the shaft encoder in the RF Generator Unit. Under normal operation, the BIT (Built-In-Test) switch deactivates the test generator. In the test mode, the encoder outputs are blocked and the Built-In-Test generator supplies simulated encoder pulses in its place so that troubleshooting can be accomplished independently of the RF Generator Unit.

The Mode switch sets the operational status of the station. In NORMAL, the antennas are automatically energized sequentially. In MANUAL, the specific antenna pair dialed by the associated switch will be continuously energized. The switch cycle lamps indicate the particular antenna pair being energized at all times regardless of mode.

The test meter and associated selector switch are used to indicate internal supply voltages. Critical internal test signals are brought out to the panel test points so that performance and operation can be checked without opening the unit.

For routine maintenance, a SCAN PERIOD switch is used to set in the number of pulses generated per complete frame period. The switch would normally be set to 1663, one less than 1664 which is the number of pulses in a frame. The difference occurs because the first pulse presets the counters and is not included in the total count. In conjunction with the built-in-test generator, this switch is used to gate a specific number of pulses through the control circuitry for help in troubleshooting procedures.

The two alarm indicator lights are located at the top of the panel. The Count Alarm Monitor counts the number of encoder pulses in the frame and compares it to the number dialed on the "SCAN PERIOD" switch. If the count is equal, the light will momentarily blink indicating normal operation. Since there are approximately 3 complete frame scans per second, the light will blink at a similar rate. If pulses are missing, the steady blinking rate will be absent.

The SWITCH ALARM light is unlit when the antenna switch drivers are operating correctly. If there are extra or missing switch control pulses in any period, the light is illuminated and stays on until manually reset by the RESET control button located beneath the lamp.

2.3.1 COUNT CONTROL AND DECODER LOGIC DETAILED DISCUSSION

Figure 2-11 draws the block diagram of the count control and decoder sections of the Control Unit. This circuitry is located on boards A1 and A2 in the Control Unit chassis. Photographs of these boards are shown in Figure 2-12 and 2-13 respectively.

The detailed operation of the count control and decoder logic follows. An optical shaft encoder is driven in synchronization with the goniometer. The encoder A channel provides 256 incremental pulses for each revolution while the B channel provides 1 reference pulse per revolution. The incremental pulses are routed to a divide by two counter in order to obtain the desired 128 pulses per revolution. Next the pulses are shaped in a one-shot multivibrator to a 1/3 duty cycle so that negative and positive pulses may be recognized. The multivibrator output is routed through an OR gate to a counter and an AND gate. The other input to the OR gate is from a Built-In-Test Generator module that simulates the normal encoder signals. The Control Units can, therefore, be checked out and maintained independent of the RF Unit.

The incremental counter essentially provides three outputs; one every 64 counts corresponding to the length of a space between transmissions, one every 128 counts corresponding to the length of a transmission, and one every 192 counts corresponding to the length of a space between a complete set (8) of transmissions. The eight position antenna selector switches are governed by a 4 bit binary to 16 line decoder, whose odd numbered output lines (8 in total) select a particular switch position when in a high state. The even numbered output lines do not activate the antenna selector switches and represent the spaces between transmissions.

In order to obtain the correct control sequence for the antenna selector switches, the decoder is stepped by an antenna selector counter via an OR gate. The antenna selector counter receives its input from a 3 input NAND gate whose output goes high at the completion of either a space (64 pulses), a transmission (128 pulses), or a long space (192 pulses). This is accomplished by taking the

64, 128, and 192 count outputs from the incremental counter and feeding them separately to 2-input NAND gates where they are combined with appropriate NAND outputs fed by the decoder. Thus, for the "space", the 64 count output from the incremental counter is combined with the output from the 7 input NAND gate representing the 7 even lines in the decoder output. With any one of the decoder 7 even lines low, the input to the 2 input NAND gate will go high and stay high until the 64 count output from the incremental counter goes high. At this point, the antenna selection counter will receive a pulse by the way of the 3 input NAND gate, which in effect, steps the decoder to an odd output line. In a similar fashion, the 128 counts from the incremental counter are combined with the odd line outputs of the decoder by the way of an 8 input NAND gate to signal the end of an antenna transmission and advance the decoder to an even output line. Finally, the 192 count output from the AND gate is combined with the last line of the decoder (#16) via an inverter to signify the end of a "long space".

The antenna selection counter is reset each 13 revolutions by the revolution counter which feeds off the encoder reference pulse channel. There again, as in the case of the incremental pulses, the circuit may be checked out in the absense of an encoder by the built-in-test generator, which generates its own reference pulses via an OR gate.

To activate the tone generator in the transmitter module during the sideband antenna "dead" times, it is necessary to provide a composite signal representing the times between transmissions. This is done by adding the 7 input NAND gate output (64 count spaces) to the decoder #16 output (192 count space) in a NAND gate with appropriate inverter gates at the inputs and outputs.

The control for the two-position phase reversal switches is derived from the incremental pulses. During the antenna transmission cycles, one switch output is activated by the incremental pulses high state and the other output by the pulses zero state. An AND gate, fed by the identical signal going to the transmitter tone-keyer and the incremental pulses provides this required signal.

The antenna selector switches may also be controlled manually through a front panel digital switch allowing any one of the 16 decoder output lines to be chosen. This is made possible because an OR gate feeding the decoder inputs accepts an input from either the antenna selection counter or from the front panel mounted binary switch depending on the position of the AUTOMATIC/MANUAL switch.

2.3.2 BUILT-IN-TEST GENERATOR

Figure 2-14 shows the block diagram of the Built-In-Test Generator. The major portion of the generator circuitry is located on Control Unit Board A4, shown in Figure 2-15.

A unijunction relaxation oscillator generates the 3.84KHz square wave. Two potentiometers near the top of the board allow for adjustment of pulse width and frequency. The oscillator stage is followed by a transistor amplifier stage that drives a one-shot multivibrator which gives the pulses a 1/3 duty cycle. The output of the one-shot provides the incremental test pulses while a divide by 128 counter provides the reference test pulses.

2.3.3 PULSE COUNT MONITOR

Figure 2-16 shows a block diagram of the Pulse Count Monitor. Components associated with this circuitry are mounted on Board A2 shown in Figure 2-12.

This monitor accepts as an input the incremental pulses provided by either the encoder or the test generator. The pulses are fed into a presettable down counter. A manual front panel binary switch selects the number of pulses that the counter will be preset to (1663 for a four speed system). The actual presetting of the counter is done by the reference pulses coming from either the encoder or the test generator. If the correct number of pulses have been counted down in one frame period, the terminal count output of the counter momentarily changes the flip-flop output to a high state. The succeeding one-shot stage stretches the pulse to about 200 Ms

width so it may be observed visually on the LED display. Hence, during normal operation of the ground station, the pulse count monitor LED lamp produces a steady blinking light as long as the correct number of pulses are counted.

2.3.4 SWITCH MONITOR

Figure 2-17 shows the block diagram for the switch monitor. The major portion of this circuitry is located on Board A3 shown in Figure 2-18.

This card monitors the control signals to the antenna selector switches during each transmission cycle and illuminates a front panel LED if the signals are not normal.

Each of the eight control signals used to drive the two antenna switches feed individual D-type flip-flops. The outputs of the eight flip-flops drive an eight input NAND gate which in turn feeds a counter. By feeding the counter outputs through appropriate decoding NAND gates, a one-shot is activated whenever the total count within a frame deviates from the number eight. The flip-flops are reset by the inverse of the control signal. A manual clear front panel button allows resetting of the one-shot and LED after an alarm condition.

2.4 AIRBORNE EQUIPMENT

The aircraft Digital VOR equipment processes the series of single cycle pulse modulated sine waves to obtain the azimuth and elevation angular positions of the aircraft relative to the ground station.

The feasibility model aircraft unit consists of two major sections -- a processor unit and the power supply unit.

The processor unit also contains the control display panel mounted on the chassis. A removeable plate on the front panel allows access to internal test points, and control functions necessary for routine maintenance, performance monitoring and adjustments. The power supply unit contains commercial power supplies that convert the aircraft A.C. power into regulated D.C. voltages required by the airborne equipment.

The Digital VOR equipments are mounted on a common pallet fitted with shock mounts to minimize shock and vibration effects. Figure 2-5 shows photographs of the processor (left) and power supply (right) units without covers.

See Figure 2-19 for a block diagram of the airborne processor. The conventional VOR audio output feeds the pulse decoder directly. The pulse decoder board, see Figure 2-20, examines the input and determines the presence or absence of pulses by time discrimination techniques. Since the pulse width of the desired signals are known, 87 usec for a narrow pulse and 174 usec for a wide pulse, discrimination circuitry is set to extract only pulses with these nominal widths. Rather than depend on the absence of a valid signal to signify the "dead-time" between sideband transmissions, a pilot tone, not harmonically related to the basic pulse rate, is transmitted during this period. It is detected in the receiver and inhibits the pulse detection function thereby eliminating the generation of false data pulses in the "dead-time" period. At very low RF levels, where the pilot itself is not detected, the signal/noise ratio is so low that the processor is correctly rejecting all data as invalid and providing a flag indication.

In addition, the pulse decoder module provides gate signals indicating the pulse type (narrow or wide) received first, when data is being received and the field and frame mark signals between antenna transmissions and the end of a complete transmission cycle.

The pulse decoder feeds the ambiguity resolver board, see Figure 2-21, which counts the number of positive and negative pulses individually. In practice, an equal number of positive and negative counts can be expected to be "lost". Therefore, provided that the number of positive and negative pulses are nominally equal and an acceptable total number of pulses have been received, an "averaging" process will correct and add in the missing counts. The VOR processor has the capability to set in various threshold levels so that system performance, during the flight test program, can be analyzed. After the averaging process, the counts are temporarily stored in a RAM (Random Access Memory).

Upon completion of a frame period, the total number of field transmissions are noted. A ground station with four interferometer antennas per baseline will generate eight field transmissions and a three speed system will generate six fields. Depending on the number of fields, the ambiguity resolver will accordingly extract the temporarily stored counts and process them to obtain the direction cosines with the correct scaling for each of the baselines. The degree of correlation between adjacent interferometer pairs are examined in the abmiguity resolver to verify the quality of the data. In an ideal error free situation, there is an exact relationship between the pulse counts associated with each interferometer pair. The magnitude of the variation from the ideal is monitored against a threshold level. As before, the threshold is adjustable so that operation of performance under various conditions can be analyzed.

The direction cosines are fed into the bearing computation circuitry made up of two modules -- Bearing and Calculator units. The calculator module, see Figure 2-22, contains standard calculator chips that perform the arithmetic operation of division to obtain the tangent of the azimuth angle. The Bearing module (see Figure 2-23)

contains the logic that manipulates the information for transfers to and from the interface module, calculator module and the deviation module.

The deviation module, see Figure 2-24, performs the arithmetic operations to obtain the difference between the OBS command and the actual bearing and feeds the result to the interface module. The interface module, see Figure 2-25, provides the necessary operations to tie in the display/control panel and convert the digital data to analog format for normal VOR display.

The timing and control module, see Figure 2-26, is the control which generates the basic control signals for transfer and computation cycles in the processor unit.

The Digital VOR processor control/display panel is shown in Figure 2-5. The two microammeters indicate the normal VOR outputs of deviation and AGC currents. The aircraft angular postions in azimuth are presented as direct numeric readouts. The TO/FROM bearing direction is indicated by the illuminated LED indicator.

The OBS is directly set by the three decimal digit switch. The MANUAL/AUTO toggle switch control is placed in the MANUAL position for normal VOR operation; and the deviation is directly related to the difference between the OBS setting and the bearing. This is quite sufficient for flight tests along radial paths.

For test flights involving orbits around the station, it is desireable to provide an OBS input that would continually step in the orbit direction. This would reduce the maximum deviation indication and permit a more meaningful analysis of system performance to be made. The AUTO position does this. In this mode, the deivation is continuously monitored, and when it exceeds a given value, the internal OBS command is incremented to a new angle ahead of the receiver bearing. Therefore, the recorded deviation output will display a "saw-tooth" shape and vary between two relatively small values. This permits a fine grain evaluation and determination of course bends and system accuracies.

The Digital VOR processor alarm threshold controls are not required for unit operation. Therefore, they are recessed and covered by the removable plate mounted on the lower part of the front panel.

2.4.1 PULSE DECODER

The function of the Pulse Decoder is to analyze the incoming detected audio produced by the conventional VOR receiver. Amplitude, pulse width discrimination and pulse correlation techniques are used to extract only valid signals and reject noise. When valid inputs are detected, the pulse decoder provides normalized logic level pulses and gates to the digital processor section; that, in turn, performs the ambiguity resolution, the computation of bearing and elevation angles, and also provides a deviation indication relative to an OBS input bearing.

The general block diagram of the pulse decoder is shown in Figure 2-27. The conventional VOR receiver output at the final IF stage is detected and routed to the Pulse Deocder input. Since the detected audio is at a D.C. level due to the receiver's internal bias network, the pulse decoder input amplifier is capacitively coupled. After amplification, the pulse amplitude modulated sine wave feeds a comparator. The comparator reference input is at ground, therefore, the comparator output switches states as the input passes through zero volts. The Figure 2-28 shows the typical input signals, both narrow and wide, and the associated comparator outputs. Hysteresis is incorporated in the comparator to reject noise signals.

The pilot tone modulation for the transmitter during the dead-time between sideband transmissions requires a filter, amplifier, and inhibit gate generator for proper processing. A high pass 6 pole Butterworth filter rejects the fundamental pulse frequency and noise below 12 KHz. Additionally, the notch filter ensures that the low order harmonics of the pulse rate are rejected. The amplifier produces an output sine wave only when the pilot tone is transmitted. As the amplifier output goes through zero at the start of the positive half cycle, it triggers the

comparator, that in turn triggers a Retriggerable Multivibrator. The normal period of the multivibrator is slightly greater than the pilot tone period so that as long as the pilot is present, the multi is enabled providing the requisite inhibit gate.

In order to determine the presence of a valid input pulse, both edges - leading and trailing - of the pulse must be detected. Essentially, the leading edge of the pulse causes a narrow delayed window, centered around the expected time of the trailing edge, to be generated. If the trailing edge does fall in this window, then a valid pulse is indicated. Two such windows would be generated, one for the narrow and another for the wide pulse. If noise, that may be present on the pulse, causes the leading edge to jitter and fall below the amplitude threshold momentarily, the time delay circuitry is reset. This ensures that the window will only be generated after a valid pulse leading edge. See Figure 2-28 for the timing relationships.

Referring to Figure 2-27, we see that gate G1 provides the delayed window for the narrow pulse extraction, and similarly gate G2 provides the window for the wide pulse extraction. Note that for the wide pulse case, gate G1 is generated too, but no output is produced, since the pulse's trailing edge does not fall within this window.

When the comparator output is high, the counter is enabled and triggers G1 just prior to the time of the trailing edge of a narrow pulse. If the comparator output remains high, G1 times out without producing an output. Just prior to the time of a trailing edge of a wide pulse, G2 is enabled. If the comparator output drops during the G2 window, an output indicating the presence of a wide pulse is produced. Again, if the comparator output remains high, G2 times out. The time delay counter some time later automatically resets and locks up its zero state. It should be noted that at any time the comparator output drops to zero, the time delay counter is reset. The time delay sequence is only enabled when the comparator changes from its low to a high output state.

Gates G1 and G2 establish Flip-Flop 1 state accordingly to provide a gate that indicates whether a

narrow or wide pulse has been detected. Also, their outputs are routed through an OR gate to provide a single count pulse source that is further processed before being fed to the digital processor section.

To eliminate the unlikely but possible erroneous detection of the start of a count cycle due to a transient, that may have a pulse shape characteristic similar to a valid input pulse, either narrow or wide, the initial detected pulses are further processed to verify their validity. The first two pulses received must meet basic preselection criteria before being further processed. If their characteristics are not satisfactory, they are rejected.

After the initial amplitude and pulse width discrimination filtering, the spacing between the pulses is examined. Since the desired input signal characteristics are well defined, both pulse width and repetition frequency, the delay of the second pulse after the first is known. If a second pulse is not present when expected, the first pulse is rejected, and no output is provided to the digital processor. When the first two pulses do satisfy the basic criteria of amplitude, pulse width and pulse spacing, then and only then is it determined that a valid signal has been received. However, further monitoring to verify that the correct number of pulses are received, that there are equal narrow and wide pulses, etc., is still continuously performed to assure integrity of the final processed data.

Due to this correlation process of the first two pulses, the first pulse would not be counted. This is compensated by a counter in the digital processor starting at a count of one rather than zero when counting the number of pulses received.

The count pulse feeds the correlator circuitry. It enables time delay counter 2 which, in turn, opens gate 3 at the time the following pulse is expected. If the initial pulse was due to a transient that had the nominal characteristics of a valid input signal, a second pulse will not be present. Therefore, gate 3 does not produce an output signal to the digital processor.

However, when valid inputs are received, the second pulse is routed through gate 3 and sets flip-flop 2. When set, the flip-flop generates a valid data present gate, DPG, that triggers the digital processor section to initiate its functions. The data present signal also gates the normalized count pulse, DPV, via gate 4 to the ambiguity resolver in the digital processor and flip-flop 3 to indicate whether a narrow or wide pulse occurred first. As mentioned earlier, note that the first pulse sent to the digital section is actually the second valid pulse received.

Each DPV also resets time delay counter 3 used to generate field and frame pulses fed to the digital processor. After field transmission, signified by no valid input to the receiver, time delay counter 3 produces a field pulse, FLD. It occurs 7 milliseconds after the last DPV pulse. After a complete frame, the time delay counter 3 produces a frame pulse, FRA, about 30 milliseconds after the last field transmission. Since the spacing between successive fields within a frame is 16.7 milliseconds, the FRA is only provided during the 50 millisecond spacing between frames.

2.4.2 DATA AVERAGER-AMBIGUITY RESOLVER

Each data field transmitted by the ground station defines a location relative to the specific antenna pair on one of the interferometer baselines. The proper combination of data fields defines a unique bearing.

The data field is demodulated within the standard VOR receiver and the pulse decoder board of the processor as a series of wide and narrow pulses. The ground station transmitting characteristics are such that theoretically, the total number of wide pulses and the total number of narrow pulses within any single data field should be 64. Depending on the receiver location, the demodulated data field will produce one of the following sequences of wide/narrow data pulses:

a) 64 wide pulses followed by 64 narrow pulses

b) "a" wide pulses followed by 64 narrow pulses followed by "b" wide pulses where a + b = 64.

c) 64 narrow pulses followed by 64 wide pulses.

d) "a" narrow pulses followed by 64 wide pulses followed by "b" narrow pulses where a + b = 64.

Thus, each data field consists of a combination of 128 wide and narrow pulses.

As discussed in the previous section, the following signals are generated in the pulse decoder section:

a) DPV (a "string" of pulses ($\approx$128) for the duration of the data field).

b) NPG (a "1" for narrow data pulses).

c) NPF (a "1" when the first pulse in a field is narrow).

d) DPG (a "1" during the data field).

e) FLD (a 200 usec pulse delayed 6.4 msec from the end of each data field).

f) FRA (a 200 usec pulse delayed 32 msec from the end of a date frame).

See Figure 2-29 for a block diagram of the Data Averager-Ambiguity Resolver.

The input data gate circuitry routes the DPV data pulses to either an up or down counter whenever the data present signal (DPG) is high. In parallel with this, the count control circuitry synchronizes the DPG, DPV, NPG, NPF, FLD, and FRA signals from the pulse decoder to internal phase clocks and generates control gates for the counters, adder and RAM (random access memory).

The counter controls consist of signals that first preset the down counter to 63 and the up counter to 0 during each field mark and then enable the down counter at the start of the DPG signal. The counter enabling signal is subsequently removed from the down counter when the NPG signal changes state and the equivalent of 64 data pulses are allowed to pass before the up counter is enabled by another change in the NPG state. Disabling of the up counter is accomplished when the DPG_1 gate goes low. In this fashion, we have counted the number $b^1 = (63 - a)$ into the down counter and the number $b + 1$ into the up counter. Since $63 - a = b$, we are compensating for lost pulses near the pulse decoder zero crossings when we add the two counter outputs in the full adder that follows and take the output as $\frac{(63 - a) + b}{2}$.

The narrow pulse first (NPF) signal causes an extra 64 to be added to the adder output. This corresponds to a total count range of 0 to 127 with 0 to 64 representing cases where the data field starts out with wide pulses first and 65 to 127 representing cases with narrow pulses first. With this technique, we have uniquely identified any combination of narrow/wide pulses within a complete data field.

The averaged data from the adder output is stored in a random access memory whose read/write commands are controlled by the count control circuitry. The data is "written" into the RAM in the order from coarse to superfine each time a field mark comes along. Depending on the number of antennas used in the ground station either 8, 6, or 4 fields will be stored.

The ambiguity resolver uses the finer resolution data associated with a particular antenna baseline to correct the coarser data. Thus, in a four speed system the superfine data corrects the fine data, the fine data corrects the medium data and the medium data corrects the coarse data. Depending on the number of fields of data transmitted, a cycle number is established in the count control circuitry. This cycle number by the way of the RAM address control determines the data readout commands to the RAM.

The data from the RAM is transferred in parallel to the ambiguity resolution algorithm circuitry. The superfine data is transferred directly into the 13 bit shift registers used for temporary storage. A multiplexer through a command from the N-S, E-W resolution control enters this data into an adder. Next, the fine data from the RAM multiplied by 4 is entered into the other input ports of the adder. The output of the adder is obtained as $\frac{4f_{FINE} - f_{SUPERFINE}}{128}$ by taking the 1's compliment of $f_{SUPERFINE}$ and adding 1 to give a binary number equal to $-f_{SUPERFINE}$. In order to round off the adder output to the nearest whole bit, we feed the sum back to the adder input where we add 1/2 to it and then take the 3 most significant bits and store them into the "FINE" and one half of the "MEDIUM" shift register. At this point we have the corrected fine data available in the shift registers. Carrying on the algorithm of $\frac{4fn - fn-1}{128}$ on the next set of coarser data; medium, and then finally the coarse data we will end up with the complete resolved data for one baseline in the shift registers. After loading this data into the cos α output register, the resolver is ready to perform similar operations on the data obtained from the other baseline (N-S). The resolved data for the N-S baseline is then also entered into the cos α register after its previous contents has been shifted into the cos β register by appropriate commands from the N-S, E-W resolution control section. Data resolving in 2 and 3 speed systems proceed in a similar manner with the RAM address control automatically making adjustments in its read/write address to compensate for "missing" data fields.

Two operations are performed on the data in the cosine registers. First, the data is serially shifted to the right 2 bits for a 3 cycle (6 data fields) transmission, or 4 bits for a 2 cycle (4 data fields) transmission. Second, the two direction cosines (N-S and E-W) are compared in magnitude. This is done by an end around shifting of the data to the right by 16 bits. In this manner, the data bits are compared from most significant bit to least significant bit. When an inequality is detected, the relative mangitudes are established and the

comparison stopped. By being shifted 16 bits, the data is returned to its original location in the register.

The output multiplexer selects the larger direction cosine to be read out first to the tangent computation circuitry. The larger direction cosine goes in the denominator so that the tangent computation is performed over a 0 to 45 degree sector where the numbers involved are finite.

2.4.3 BEARING COMPUTATION

See Figure 2-30 for a block diagram of the bearing calculation circuitry. The direction cosine data from the ambiguity resolver are applied to one of the inputs of the direction cosine/octant address multiplexer. Prior to passing through the direction cosines this multiplexer selects the octant correction address. The reason for this is that the tangent computation is performed on 0 to 45 degree sectors. There are eight sectors and the appropriate sector is determined by the octant decoder. The octant decoder logic produces the octant address based on conditions placed on the coarse E-W and N-S data field narrow pulse first signal and the relative magnitudes of the E-W and N-S direction cosines. This is the address of the location in a programmable memory (PROM) which contains the binary number corresponding to the octant correction in degrees to be added to the 0 to 45 degree sector to give a bearing between 0 and 359.9 degrees.

The octant address is transferred to a binary counter by the way of the multiplexer, and stored in the memory address buffer. There, it addresses the PROM and the octant correction data is read out of the PROM and stored in the octant correction buffer storage.

After the octant correction has been stored, the direction cosines are transferred in parallel via the multiplexer into the binary counter. The binary counter is used to convert the binary direction cosine data into binary coded decimal (BCD) for operational use in the tangent calculator. This is accomplished by

counting the binary number down to zero as a BCD counter is counted up. The count pulses are generated in the Tan A, cos α , cos β BIN/BCD control circuitry.

The input to the TAN calculator is routed through the TAN calculator load register with the numerator entered first from most significant digit to least significant digit. Then the divide command, the denominator most significant digit to least significant digit, and finally the equal command. The control for data read in and read out of the TAN calculator are generated by the TAN calculator R/I-R/O control, which feeds the calculator input multiplexer. Two 4 bit serial shift registers wired as a ring counter determine the 8 states for controlling the tangent computation. The operation taking place during each state are listed below.

STATE	OPERATION
1	a) Reset TAN calculator.
	b) Parallel load numerator (cos α or cos β) into binary counter.
2	a) Convert binary direction cosine (α or β) into BCD.
	b) Parallel load calculator load register with BCD direction cosine (numerator).
3	a) Enter BCD direction cosine (numerator) into TAN calculator.
	b) Enter TAN calculator "divide" command.
	c) Parallel load denominator (cos α or cos β) into binary counter.

STATE	OPERATION
4	a) Convert binary direction cosine (α or β) into BCD.
	b) Parallel load calculator load register with BCD direction cosine (denominator).
5	a) Enter BCD direction cosine (denominator) into TAN calculator.
	b) Enter TAN calculator "equal" command.
6	a) Readout tan γ from TAN calculator into BCD counter.
7	a) Convert tan γ from BCD to binary.
8	a) Reset TAN calculator R/I-R/O controls.
	b) Load binary tan A into memory address buffer.

The TAN calculator consists of a 10-digit decimal arithmetic processor chip with external interface circuits. The processor chip is an MOS/LSI digital (building block designed to process numerical data) in BCD format. It performs the most commonly required arithmetic operations, and numbers up to ten digits can be processed in under 100 milliseconds. Functions that the processor will perform may be classified into three types; arithmetic, register, and internal control (housekeeping). The timing of the data entry and control is determined by the enable input in conjunction with the status outputs. Data entry is possible during the READY mode only. The processor will ignore inputs when performing an operation.

Data inputs are changed each time the processor goes from the READY to the BUSY state until the entire sequence is completed. The serial data input line requires its information in the form of a serial five-bit word. Four bits are used as data/instruction code and the fifth bit as control. The control determines whether the four-bit code is interpreted as data or as in instruction.

Part of the PROM fed by the memory address buffer is an Arc-tangent look-up table covering the sector of 0 to 45°. Tangent γ in binary notation addresses the PROM resulting in an output γ in binary form. Since covers only 0 to 45°, the ration $\frac{\cos \alpha}{\cos \beta}$ or $\frac{\cos \beta}{\cos \alpha}$ is set up so that the numerator is always the smaller number. This means the bearing subangle (with no octant correction) should be read out as either γ or 90- γ depending on whether cos α or cos β is in the numerator. Figure 2-31 and the accompanying table show the relationship between the bearing angle A and γ.

The binary number γ and the octant correction from the PROM are fed to an adder/subtractor whose output is (n-45 $\pm$ γ). The decision whether to add or subtract the subangle γ is determined by the octant location which is obtained from the octant decoder. The whole number part of the bearing angle A is in binary form, 9 bits;

2^0 - 2^8 while the fractional part of the angle has 6 bits;

2^{-1} - 2^{-6}. Only the bits 2^8 to 2^{-4} are loaded into the bearing binary counter.

2.4.4 DEVIATION COMPUTATION

See Figure 2-32 for a block diagram of the deviation computation circuitry. Deviation is computed between the time the binary bearing is output from the adder/subtractor of the bearing calculation circuitry and the time this binary bearing is converted to BCD. The deviation is the difference between the front panel OBS (Omni Bearing Selector) thumbwheel input and the computed bearing angle. This difference is obtained as follows.

The decimal OBS thumbwheel input is transferred as three BCD digits to the OBS update counter. The function of this counter is to permit the OBS input to be changed automatically so that the deviation does not exceed a preset limit if the front panel OBS control switch is set to the "automatic" position. With the OBS control switch in the "manual" position, the decimal OBS thumbwheel input passes through the update counter unaffected. From the OBS update counter, the OBS is transferred to the OBS BCD counter. As this counter is counted down to 0, the OBS Binary Counter is counted up. The clock pulses for the binary to BCD and BCD to binary conversions are generated in the Central Control Timing circuitry.

After the OBS data has been converted to binary in the OBS Binary Counter, it is compared against the binary bearing data. If they are not equal, a deviation exists. The magnitude of this deviation is determined by taking the difference between the bearing and the OBS. This is accomplished by counting down the OBS Binary Counter while the Deviation Display Counter is being counted either down or up until the comparator senses an equality between the OBS and the bearing. The Deviation Display Counter is first counted down from 0 to -90. At -90, a comparator causes the Deviation Counter to be counted up towards +90. At +90, a second comparator causes the counter to be counted down to zero. Deviation in the range of 0 $\pm 90°$ are represented as a "FROM" signals while 180° $\pm 90°$ deviations are represented as "TO" signals by way of independent front panel LED indicators. Logic gating generates an out of range deviation for the front panel meter whenever the deviation exceeds $15\frac{15°}{16}$ from 0 or 180°

For example, if the bearing should happen to be greater than the OBS, the OBS Binary Counter will count down to 0, reset to 359, and continue counting down until its output equals the bearing. At this point, the Deviation Display Counter stops counting and the whole number part of the deviation is transferred from this counter to the deviation buffer. The fractional part of the deviation ($2^{-1} - 2^{-4}$) comes directly from the PROMS of

the bearing calculation circuitry and are stored in the 4 least significant bits of the Deviation Buffer.

The Deviation Buffer drives a data converter to generate an analog voltage corresponding to the deviation. This analog deviation passes through a circuit with a variable time constant, and a second circuit with a variable gain before driving the deviation meter on the front panel.

The Bearing Display Blanking Circuitry determines if the change between successive bearings exceed a preset limit. This is done by counting the pulses to the BCD bearing counter in a separate threshold counter. For each bearing, the output of the deviation threshold counter is examined to see that it lies within a thumbwheel threshold. When the deviation threshold limit is exceeded, the bearing LED display is blanked and the bearing output buffer load is inhibited if S18 is in the down position. With S18 in the up position, all bearing readings are displayed.

2.4.5 FRONT PANEL

The front panel contains the displays, controls, and test points related to the Digital VOR. See Figure 2-25 for the VOR Processor Control Panel.

a) Deviation

A microammeter (M1) displays ± deviation with two possible sensitivities:

(1) 1 uamp = 1° deviation when S16 is in the X1 position (down). The maximum range is then =±15-15/16°.

(2) 1 uamp = 0.1° deviation when S16 is in the X10 position (up) the maximum range for this setting is ±1.6°.

The time constant of the signal to the deviation meter is controlled by switch S15 and potentiometer R1 for a given setting of S15. Rotating R1 changes the time constant between the indicated limits.

b) TO/FROM Indicators

The TO/FROM (DS1, DS2) lights indicate if the bearing deviation from the OBS setting is on course or 180° off course. Table illustrates this.

TABLE

	TO(DS1)	FROM(DS2)	DEVIATION(ua)
Bearing = OBS	OFF	ON	0
Bearing = OBS + 180°	ON	OFF	0
Bearing = OBS + 10°	OFF	ON	+10
Bearing = OBS - 10°	OFF	ON	-10
Bearing = OBS + 180° +10°	ON	OFF	-10
Bearing = OBS + 180° - 10°	ON	OFF	+10

c) Bearing

DS3 through DS6 presents a 3 digit + decimal fraction of Bearing angle from 0° north heading. If S18 is down, each bearing measured will be displayed. If S18 is up, only those bearings which differ by less than the threshold of S17 will be displayed. The display will be blanked for all others.

d) AGC

Meter M2 is a monitor of the receiver AGC voltage.

e) Flags

The flag display lights operate in conjunction with various thresholds established by thumbwheel switches. See Table.

TABLE

FLAG	DESIGNATION	THUMBWHEEL	CONDITIONS FOR FLAG
Data	DS9	-	Data not present.
Count	DS10	-	Light will be going on and off at a steady rate whenever receiver is processing data.
Up/ Down	DS11	S12	Difference between number of wide pulses and number of narrow pulses is greater than thumbwheel setting.
Resolution	DS12	S7	Ambiguity resolution correction greater than thumbwheel setting.
Deviation	DS13	S17**	Change in successive bearings is greater than thumbwheel setting.
System	DS14		Any previous flan ON.

** S17

CYCLE	MINIMUM RESOLUTION	MAXIMUM RANGE
4	0.2°	3.0°
3	0.4°	6.0°
2	0.8°	12.0°

e) OBS

Thumbwheel switches S1, S2, and S3 enter the OBS data. The OBS is compared with the bearing to generate deviation. The OBS update switch (S4) in the MANUAL position means that the deviation is based on the OBS set into the thumbwheel. With the OBS update switch (S4) in the AUTO position, the OBS is automatically updated (by 2° if S14 is down or 4° if S14 is up) if the deviation exceeds 1° or 2° that the deviation is maintained less than or equal to ±1° or ±2° correspondingly.

3.0 FIELD TEST PROGRAM

3.1 INSTALLATION AND PRELIMINARY CHECKS

The Wide Aperture Digital VOR system equipment was delivered to NAFEC, Atlantic City, New Jersey in August 1975. The ground station, shown in Figure 3-1, was installed at the old MOPTAR site, which is a flat 300 foot diameter asphalt surface with a centrally located equipment pit. The terrain beyond the asphalt surface is fairly level in the northern direction while it drops off sharply some 10 feet towards the south. Gently rolling terrain characterizes the airport property in general.

As shown in Figure 2-8, an equipment pit, about 4 feet deep, 3 feet wide and 10 feet long is located on the 90° radial with respect to North. Because the East medium antenna would "fall" over the pit, if the baselines were positioned in the conventional North/South - East/West directions, the axes were rotated 45 degrees. Accordingly, the receiver was programmed to compute the bearing for this orientation.

The transmitting antennas, shown in Figure 3-2, standard Alford VOR Loop antennas, were mounted on four foot aluminum pedestals. These were attached to square concrete filled wood forms that rested directly on the asphalt. All antenna cables were routed to the ground station equipment pit.

After completion of the ground station installation, the receiving equipment was installed in a van with a telescoping antenna. Ground checks and phasing adjustments were made at a minimum of 1000 feet from the station. The system performance was checked at surveyed points around the transmitting site. Concurrently, the NAFEC data interface and recording system was installed and checked out.

Preliminary flight checks were held in December 1975 to qualitatively verify overall ground-airborne system operation and to completely check out the data recording system. This recording system provided a synchronous record of key internal aircraft receiver processor signals, VOR bearing output and data from the NAFEC EAIR radar tracking facility.

Analysis of early flight check data indicated the receiver provided erratic bearing readout information at certain angular sectors (primarily around 135 and 315 degrees). The great majority of these were directly traceable to the inner (coarse) sideband antenna transmissions by analysis of the "antenna count" data. During the antenna installation, the positioning of the antennas were made by measuring from the physical center of each of the antennas, which is not necessarily equivalant to the electrical spacing. Indeed, the data showed that the electrical spacing between antennas was greater than the physical dimensions would indicate. Other contributions to the problem were induced parasitic currents due to the very tight spacing of the coarse antenna cluster. Subsequent adjustments of antenna phase, inner antenna spacings, and antenna orientations to each other corrected the earlier problems of erratic readings. The remaining antennas were not touched after their initial installation.

It should be noted that no averaging or filtering of the raw data was performed in the computations. Each bearing readout calculation is based on just one complete ground station cycle. In other words, the bearing computations are completely independent of each other. This was purposely done so that basic performance characteristics of the system, on a independent cycle to cycle basis, would be obtained, without masking of any raw data anomalies.

3.2 DATA PROCESSING AND TEST INSTRUMENTATION

Figure 3-3 shows a typical computer print out page. The NAFEC clock time representing the specific time of recording the data is shown in the lefthand column. Miscellaneous analog outputs representing deviation and receiver AGC are under IAN0 and IAN1. The primary raw data of pulse counts from each antenna pair are listed under AC1 through AC8. AC1, AC3, AC5, and AC7 represent the superfine, fine, medium, and coarse antenna pairs along the East/West axis (N-E axis, see Figure 2-8). Similarly AC2, AC4, AC6, and AC8 represent the corresponding pulse counts from the antenna pairs along the North/South axis.

The resultant ambiguity resolution computation is shown in the cos 1 and cos 2 columns; where cos 1 is the result of the computations from the data of AC2, AC4, AC6, and AC8 and cos 2 is the result of the computation from the data of AC1, AC3, AC5, and AC7. Because of the serial transfer and timing of the receiver data to the data acquisition system, the receiver bearing output data associated with the cos 1, cos 2 data is printed on the following line. The associated merged EAIR data, translated to the Digital VOR axis, representing aircraft slant range, azimuth and elevation are also listed in the computer print out.

3.3 TEST RESULTS

The quantitative test data presented herein were collected from orbital test flights on July 12, 1976 and an earlier radial, for which merged EAIR data was available, flight flown on May 5, 1976. The orbits were at 6 and 12 slant mile range, and at about 5800 feet altitude. The data shows that the system errors were about 0.11 degrees standard deviation under all tests.

The azimuth error was computed directly by taking the difference between the VOR bearing output and the corresponding EAIR reference bearing. As noted earlier, no filtering or averaging of the results was performed. The results for the tests are summarized below:

TEST	MEAN	STANDARD DEVIATION
6 mile orbit	.047	0.11
12 mile orbit	.035	0.11
Radial	.04	0.10

The 360 degree error plots for the orbit tests are shown in Figures 3-4, 3-5 and the radial test in Figure 3-6.

Unfortunately, a direct plot of the data was not available. Consequently, quite arbitrarily the 360° azimuth error plots were generated by sampling the last line of data on each computer print out page. The validity of this statistical sample was verified by taking a second set of samples from a line in the middle of each page and comparing the statistics of the two samples. This second set had a mean of 0.30° and standard deviation of 0.091° which compares very closely with the mean of 0.035° and standard deviation of 0.11 for data presented.

Overall, the error plots over the 360° azimuth show a slight cycling tendency, and generally a random distribution each side of the mean. However, the spacing of these data samples will not uncover any higher frequency error components. Therefore, further analysis was made by examining the continuous output of the VOR over several small azimuth sectors.

The selected sectors are representative of the possible modes of system operation.

1. Crossing an antenna baseline (225° radial).

2. Crossing a 45 degree octant boundary (180° radial).

3. Remaining within an octant.

The typical computer print out page shown in Figure 3-3, describes a 25 second period of the 12 mile orbit covering the sector from 59.65 degrees through 66.05 degrees. Its error plot is shown in Figure 3-7. Here, it is readilly apparent that there is a high frequency error component with about a .23 degree peak to peak value. The mean value of the error in this sector is -0.04° with a standard deviation of 0.077°. The corresponding data for the 6 mile orbit is also shown. Its mean is 0.102 with a standard deviation of 0.077.

The radial flight, supposedly on a constant radial, actually deviated from the starting 182 degree radial and finished at the 180 degree radial. Consequently, a direct azimuth error plot as a function of range is misleading since the errors as a function of azimuth angle are significantly greater. Therefore, Figure 3-6 shows two plots; one for the combined error (due to both range and azimuth) and secondly, with the error due to the range alone. The latter curve is generated by taking the difference between the 12 mile orbit results and the radial at these angles. Essentially, it is the difference between the two curves shown in Figure 3-6 describing the errors in the 178/184 degree sector.

In this sector, the mean and standard deviations are:

TEST	MEAN	STANDARD DEVIATION
6 mile orbit	.13	.04
12 mile orbit	.10	.10
Radial	.04	.10

Finally, Figure 3-7 displays the 6 and 12 mile orbit performance in the 222/227 degree sector as the aircraft crosses an antenna baseline.

3.4 TEST ANALYSIS

Although the basic objectives of the flight tests have been accomplished, that is demonstrating that the Wide Aperture Digital VOR has provided the 10 times more accuracy, the fact that the error plots display notable cyclical components, indicates that system performance can be further improved. Generally, a cyclical characteristic is a strong indication that its source is due to some system equipment or configuration percularities that can usually be corrected.

As noted, system goals were achieved even with these cyclical errors. Thus, no attempt was made to modify the feasibility equipment to eliminate the systematic errors. However, an analysis of the system design points out several critical areas, discussed below, that could produce these types of errors.

The expanded error plots, about the 60/66 degree 178/184 degree and 222/229 degree sectors, show similar cyclical errors with a nominal 1.8 degree azimuth period and a peak-peak value of about 0.2 degrees. It has twice the frequency of the electrical cycle generated by the superfine interferommeter pair. This type of cyclical error arises when a bias exists in the time measurement circuitry.

The possibility of this kind of error was discussed in Quarterly Report A248-Q4. Because the pulse decoder input circuit uses a comparator referenced to ground, changes in the capacitively coupled detected audio output of the VOR receiver would change its effective threshold level. The changes may arise due to the assymetrical pulse modulation of the sine wave that varies with azimuth of the aircraft; and also, audio envelope distortion that can introduce an effective DC level shift.

Laboratory tests showed that an error of 0.084 degrees could be introduced. However, it was concluded that because the error was quite small, further design effort to eliminate this effect was not warranted. Even now, considering the operational accuracy already achieved, there does not appear to be a compelling reason to further reduce the system errors.

A factor contributing to the single cycle error may be a variation in electrical heights between the superfine antennas, as "seen" by the aircraft, as it moves around the ground station. The fundamental measurement made is the direction cosine defined by the angle made by the intersection of the axis joining the two antennas with a line from its midpoint to the aircraft. The axis must be parallel to the surface of the earth, otherwise an error will be introduced as the aircraft moves. Because the superfine antennas are located near the periphery

of the circular area, it is possible that the two antenna heights may appear to vary electrically at different azimuths and elevation. This results from the different and changing ground planes between each antenna and the aircraft as it changes position. Normally, the differences on ground planes are imperceptible, but again it should be noted that sources of extremely small errors (under 0.1°) are being explored. The magnitude of the height variations under consideration are found by observing that the superfine antennas are spaced 275 feet (32 λ) and a 3 inch difference in height might produce a $\pm$0.05 degree cyclical error.

Similarly, the initial positioning of the ground station antennas can be a source of error. The alignment of the antenna axis is within $\pm$0.03 degrees of nominal. Normally, an inconsequential error, but again significant in comparison to the measure results.

Another possible factor may be vertical polarization effects due to radiation from the vertical antenna supports.

Finally, the test instrumentation including the data acquisition and EAIR tracking radar effects must be taken into account. The EAIR has a 2 sigma tracking error of 0.088° azimuth and 0.05 degree elevation which are not an insignificant percentage of the observed errors in the test data.

The last test orbits described were made with the final configuration of the ground station antennas; and almost all erratic readings were eliminated. However, occassionally single readings due to some transient noise and obviously incorrect, displaying large bearing errors would occur. As has been stated, the calculation of the bearing is made on a cycle-by-cycle basis with no filtering or averaging. Therefore, an erroneous count, in any one of the 8 antenna count inputs, would produce an error, for the associated bearing calculation; with the magnitude of the error dependent on the particular antenna pair in error.

The erroneous indication can be easily prevented by a simple prediction or averaging circuit. The computer print out (Figure 3-3) for the antenna counts shows that successive antenna counts can be readilly predicted by its past history. Within limits, the next antenna count can be estimated by taking the difference between its present and the immediately preceding readings; and then adding the difference to the present reading. If the following reading is significantly different than expected, then the estimated value would be used in the calculations. If the differences consistently exceed the predetermined limit, an error flag would be generated. The flag would inhibit bearing readout and alert the operator that erroneous data is either being received or that an internal receiver failure has occurred. With the ready availability of microprocessors and peripheral memory IC chips, the circuitry to accomplish this is relatively trivial.

The possibility of "locking on" to a wrong bearing indication is totally eliminated by the ambiguity resolution process that is repeated independently for each transmission cycle. If noise, under low signal strength conditions, induces erroneous counts, the accumulated numbers from cycle to cycle would differ; and the error flag, described above, would be produced.

In summary, several system areas have been identified that could account, either individually or in some combination for the systematic errors that have been observed. The design modifications to further increase system accuracy are well within the state-of-the-art. However, as has been repeatedly mentioned, the magnitude of the errors are quite small; and they are apparently within the accuracy requirements needed by a new generation VOR to meet the needs for precision navigation for the 1980 period and beyond.

4.0 CONCLUSION AND RECOMMENDATIONS

The purpose of the work described by this report was to obtain a VOR that is greatly superior to any so far developed. The tests have proven the feasibility of the Wide Aperture Digital VOR in meeting this objective. In particular, an improvement in accuracy by approximately 10 times over present VOR's has been demonstrated with residual system errors of 0.11 degrees.

Therefore, as a result of this work, a new, reliable, and useful technique has been demonstrated. Further, the FAA should continue to work with the existing feasibility model to:

1. further delineate basic system performance

2. determine effects of siting factors such as size and orientation of reflecting objects

3. verify Wide Aperture Digital VOR compatibility with existing VOR systems by installing Wide Aperture Digital VOR ground station at existing VOR site and operating it on same VOR channel frequency

4. measure system performance with one-half the number of antennas. This would reduce the number of antennas from 17 to 9. E.g., the interferommeter pairs would each consist of one antenna plus the control carrier antenna

5. use available higher power VOR transmitter to increase range

6. integrate on R-NAV computer with the Digital VOR receiver and demonstrate operation over prescribed paths.

Concurrently or after additional data on system performance has been obtained:

1. investigate and modify equipment to correct the deficiencies noted earlier

2. add processing circuitry in receiver to provide filtering and short term averaging of raw data to enhance reliability and accuracy of the VOR bearing indication

3. Study monitoring methods.

Finally, the system should be installed and tested at a known poor site like Rikers Island, New York.

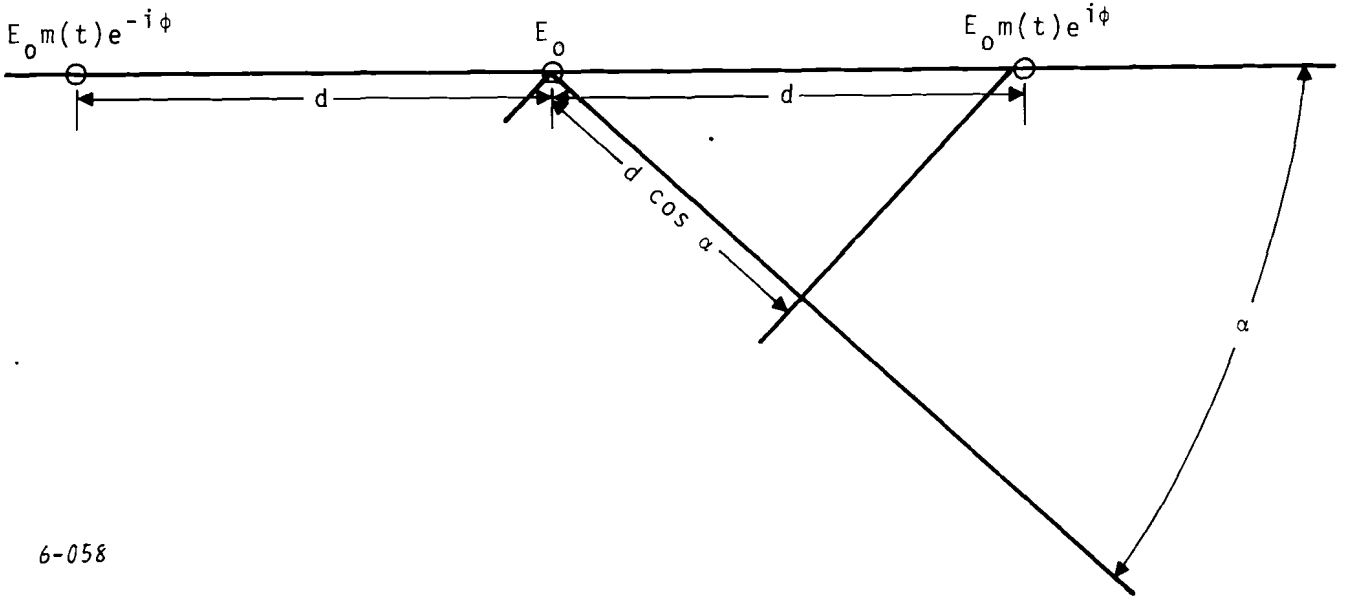
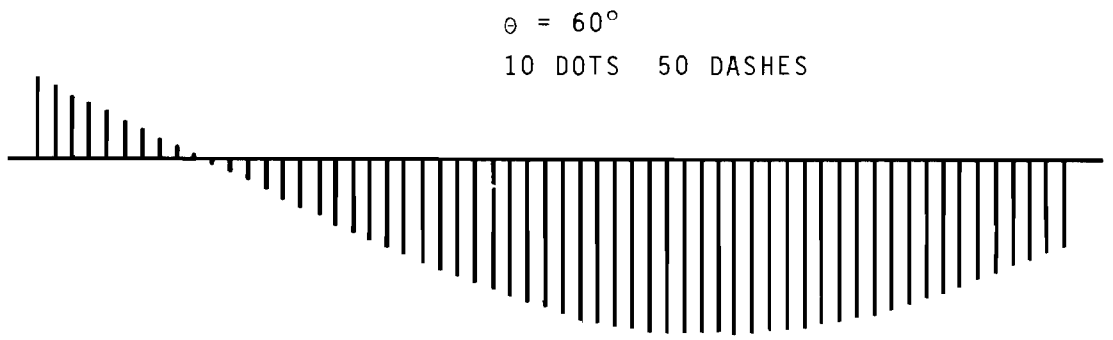
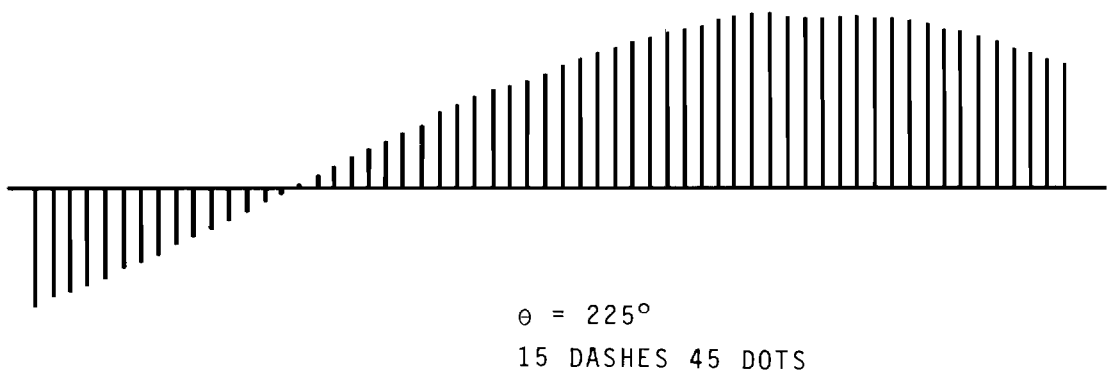


FIGURE 1-1. BASIC THREE ELEMENT INTERFEROMETER



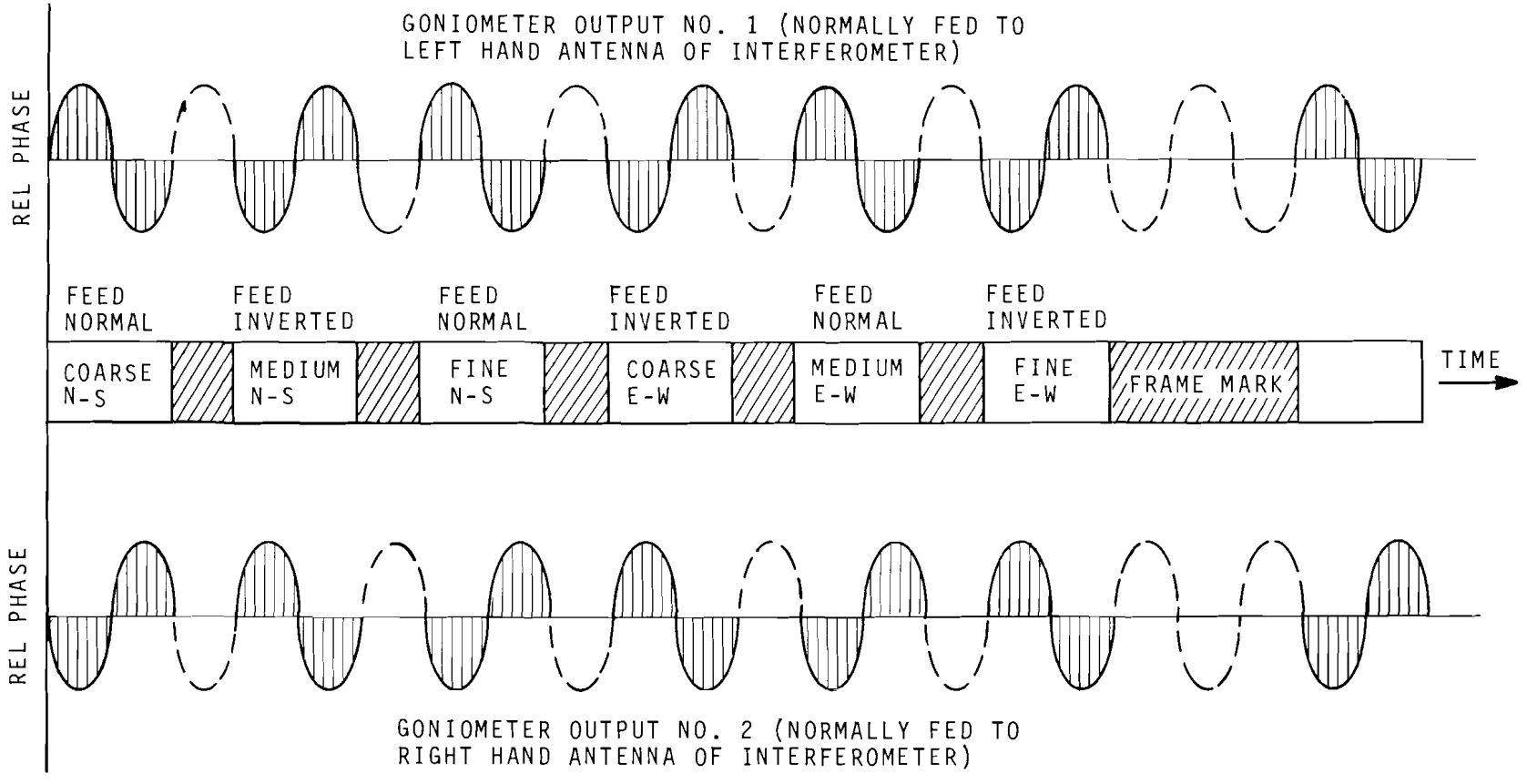
(a)



(b)

6-059

FIGURE 1-2. RECEIVED CODING WAVEFORMS



2-1253

FIGURE 1-3. TRANSMITTER WAVEFORMS

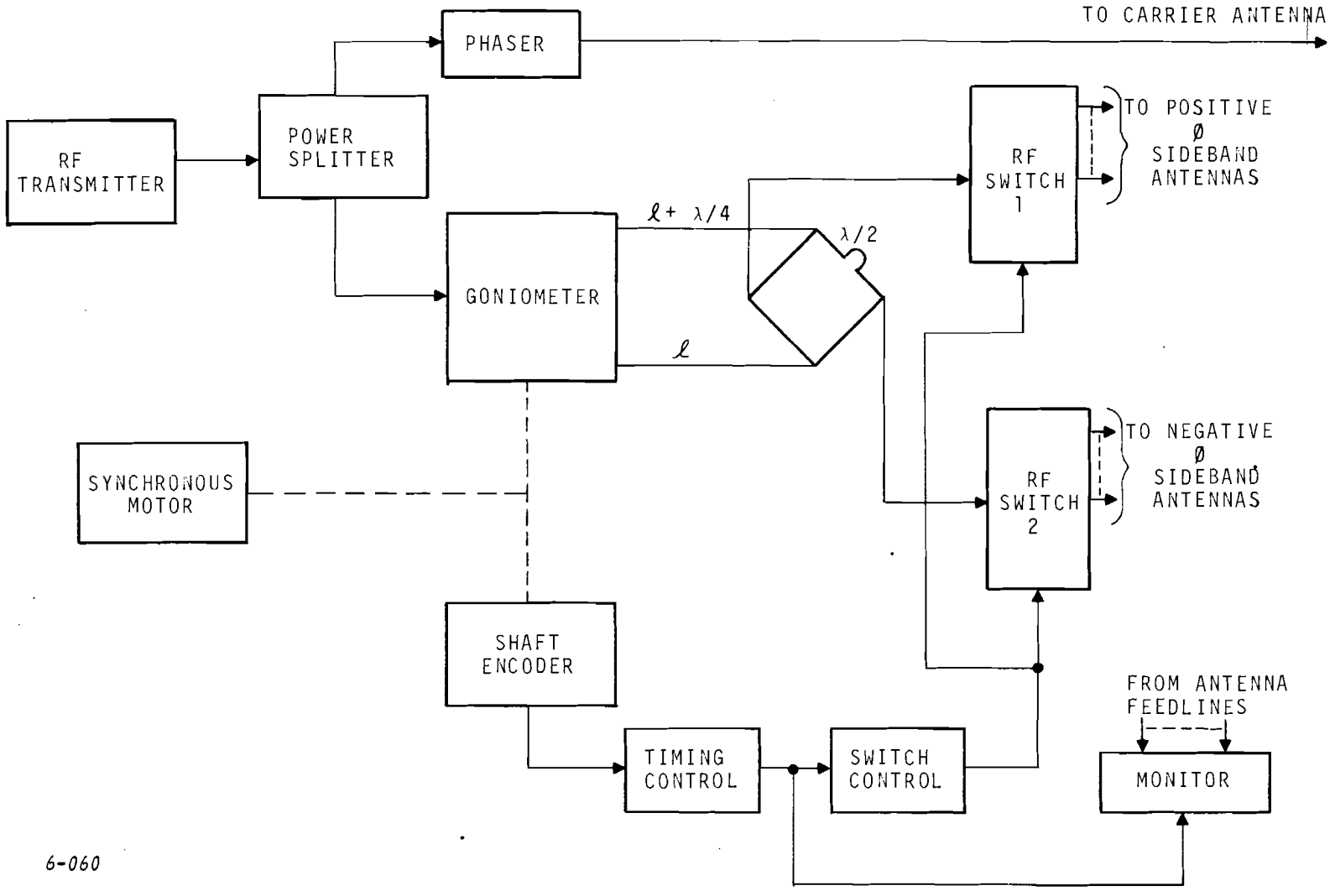


FIGURE 2-1. GROUND STATION GENERAL BLOCK DIAGRAM

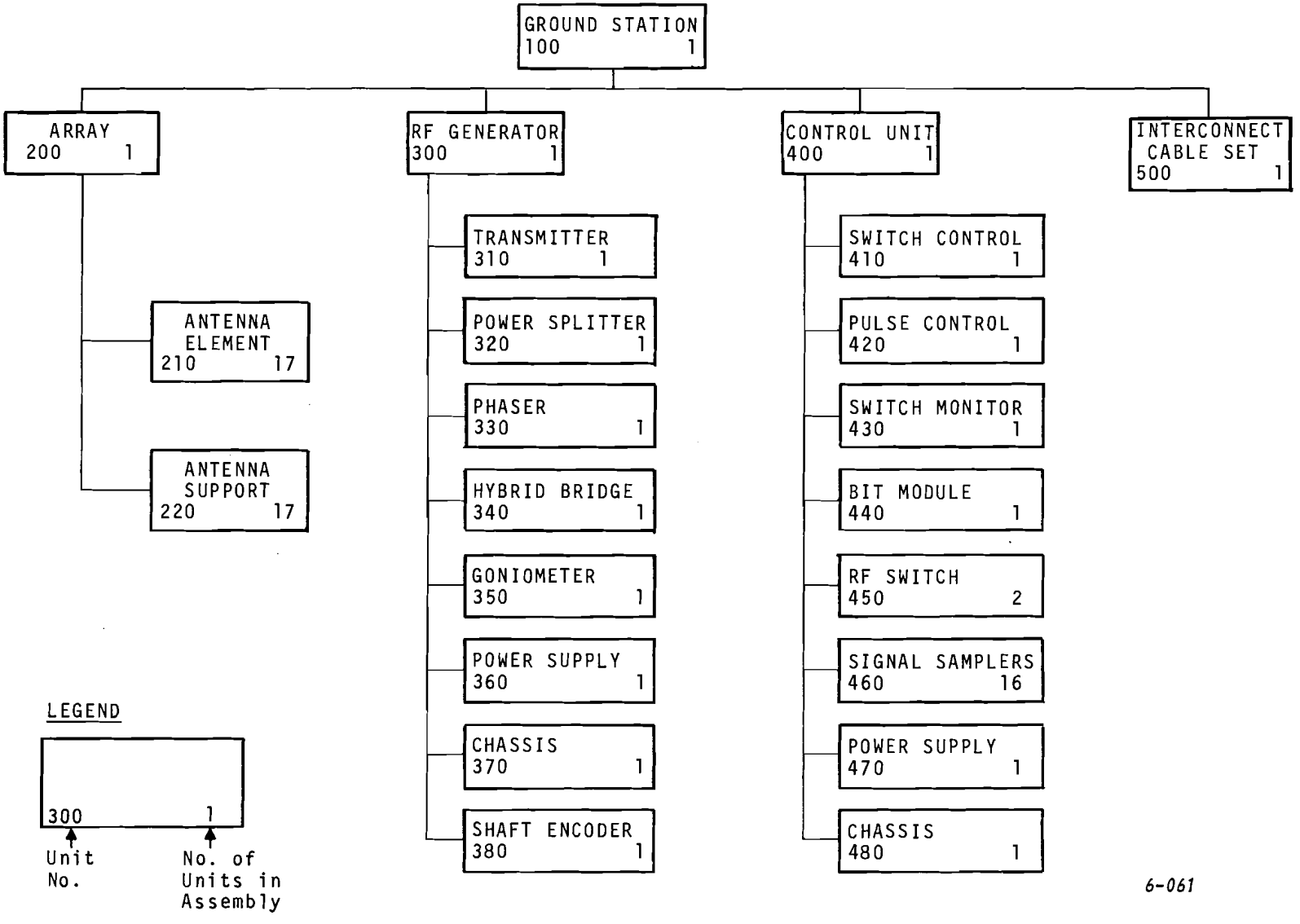
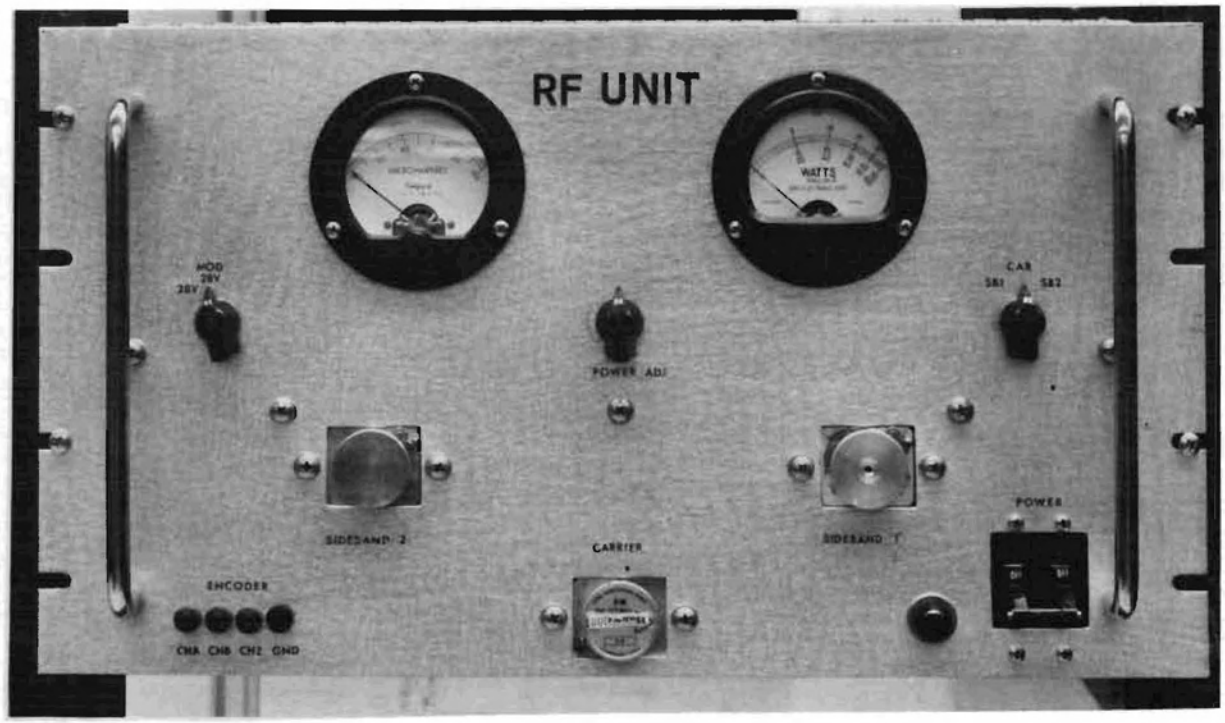
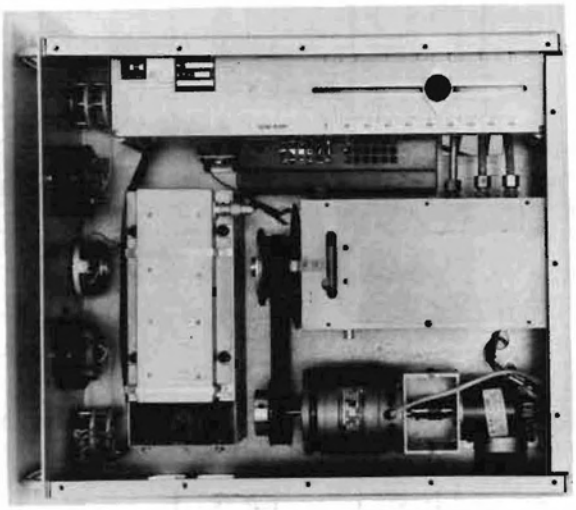


FIGURE 2-2. GROUND STATION EQUIPMENT FAMILY TREE



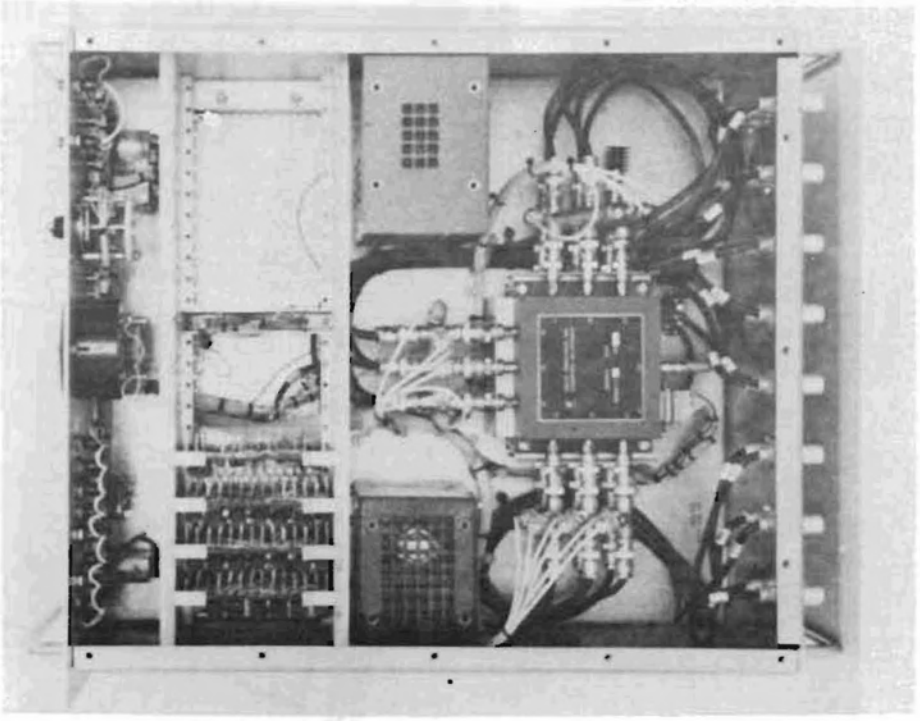
FRONT VIEW



TOP VIEW

FIGURE 2-3. RF UNIT

FRONT VIEW



TOP VIEW

FIGURE 2-4. CONTROL UNIT

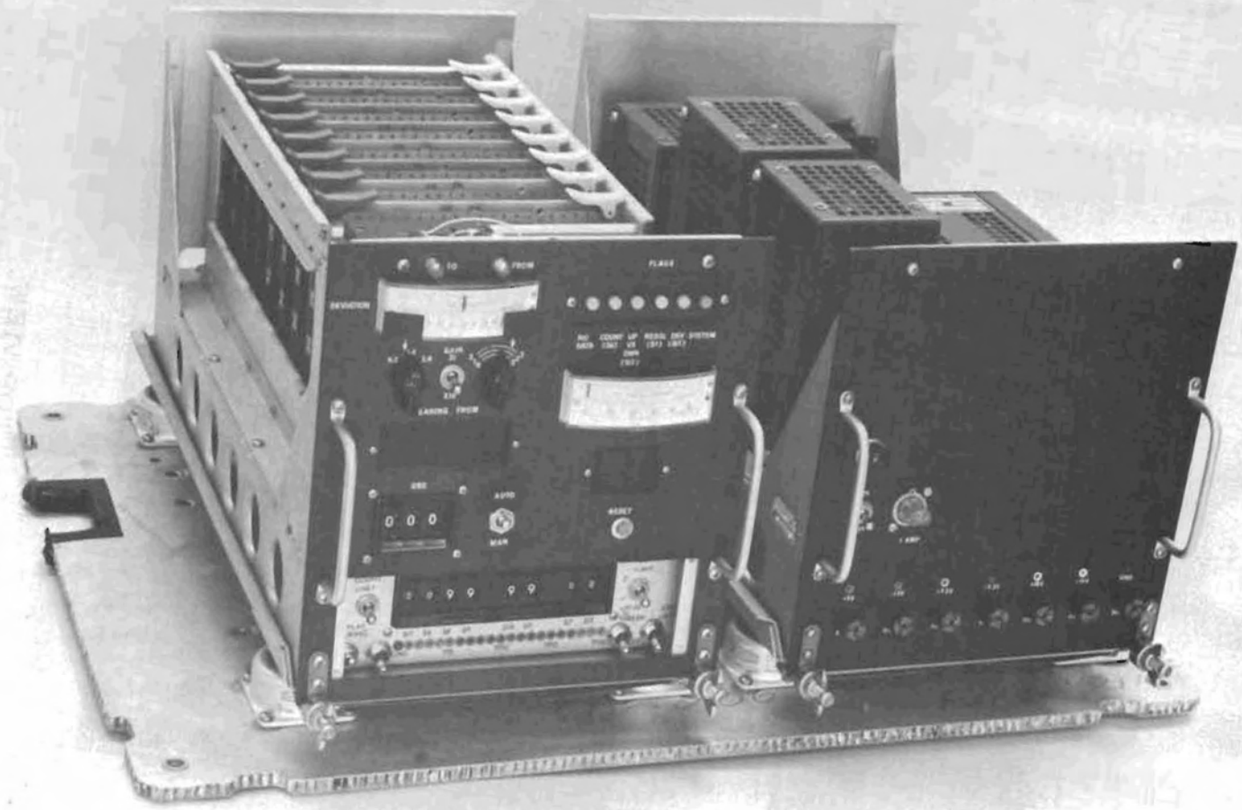


FIGURE 2-5. AIRBORNE UNITS WITH COVERS REMOVED

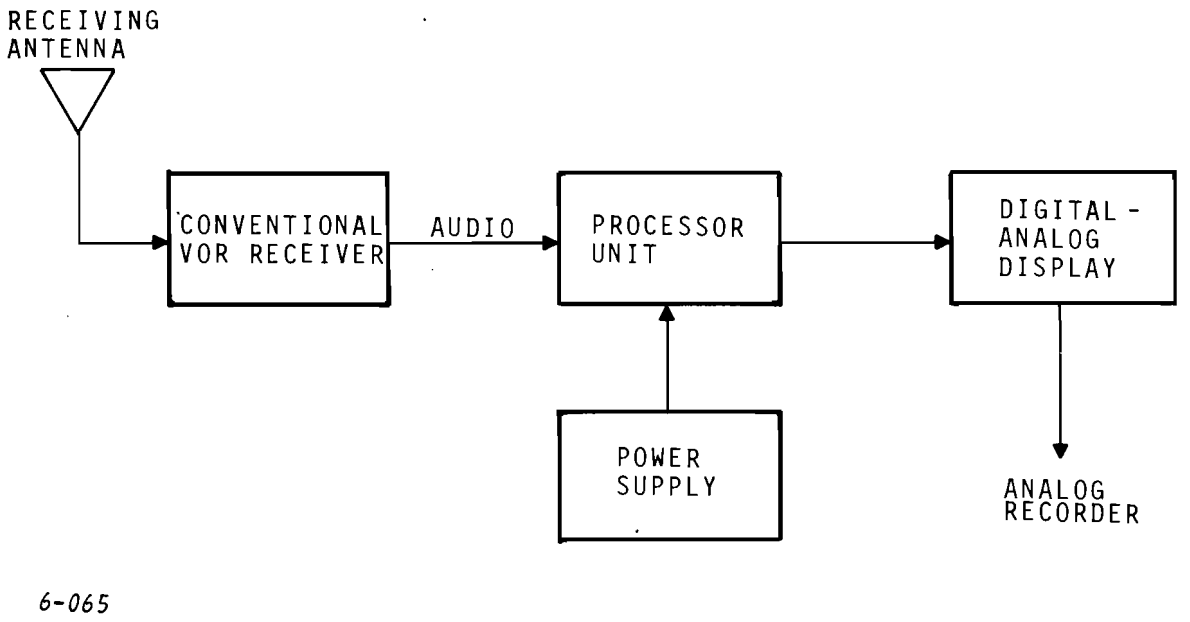


FIGURE 2-6. AIRBORNE EQUIPMENT BLOCK DIAGRAM

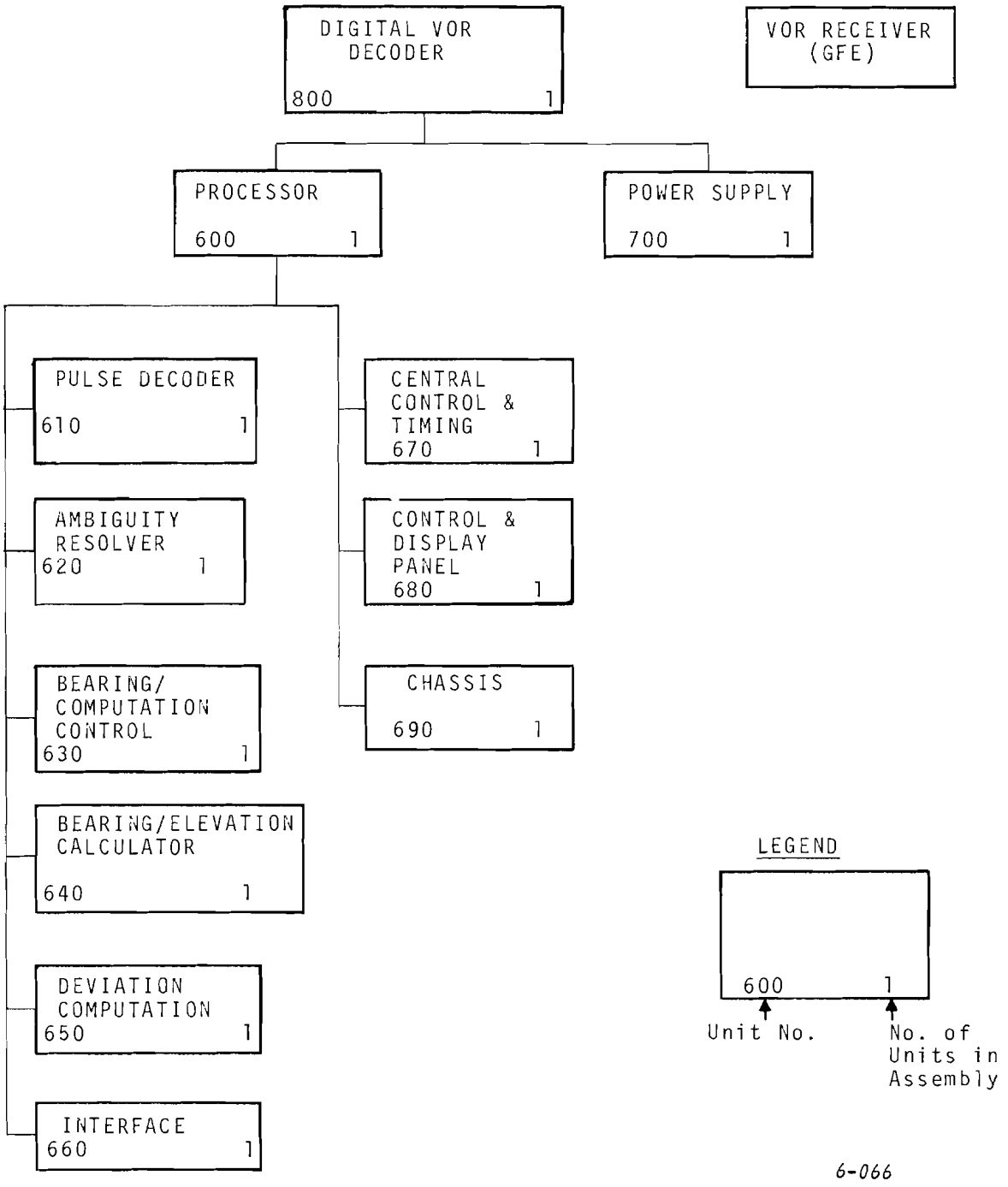


FIGURE 2-7. AIRBORNE EQUIPMENT FAMILY TREE

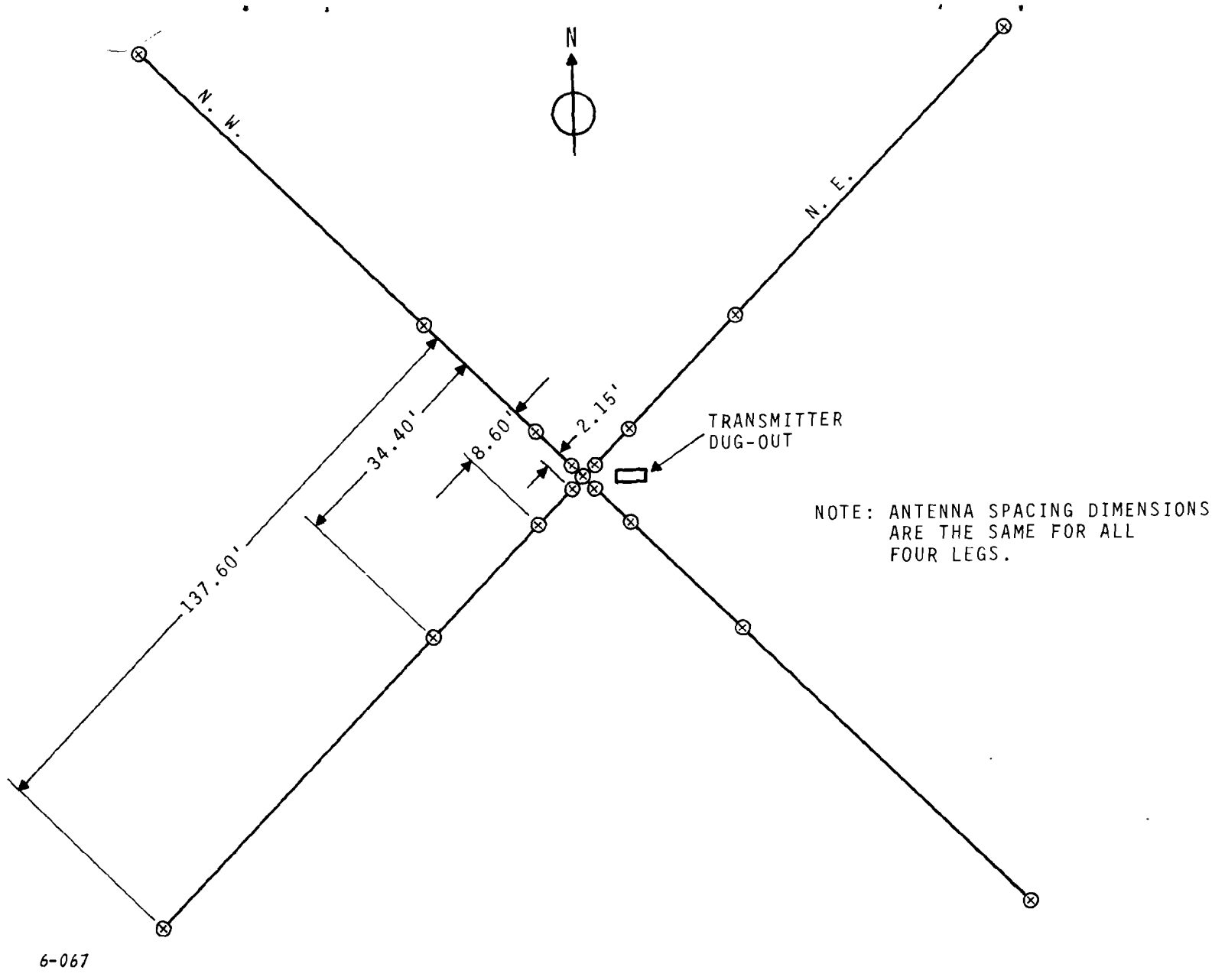


FIGURE 2-8. DIGITAL VOR ANTENNA BASE LAYOUT

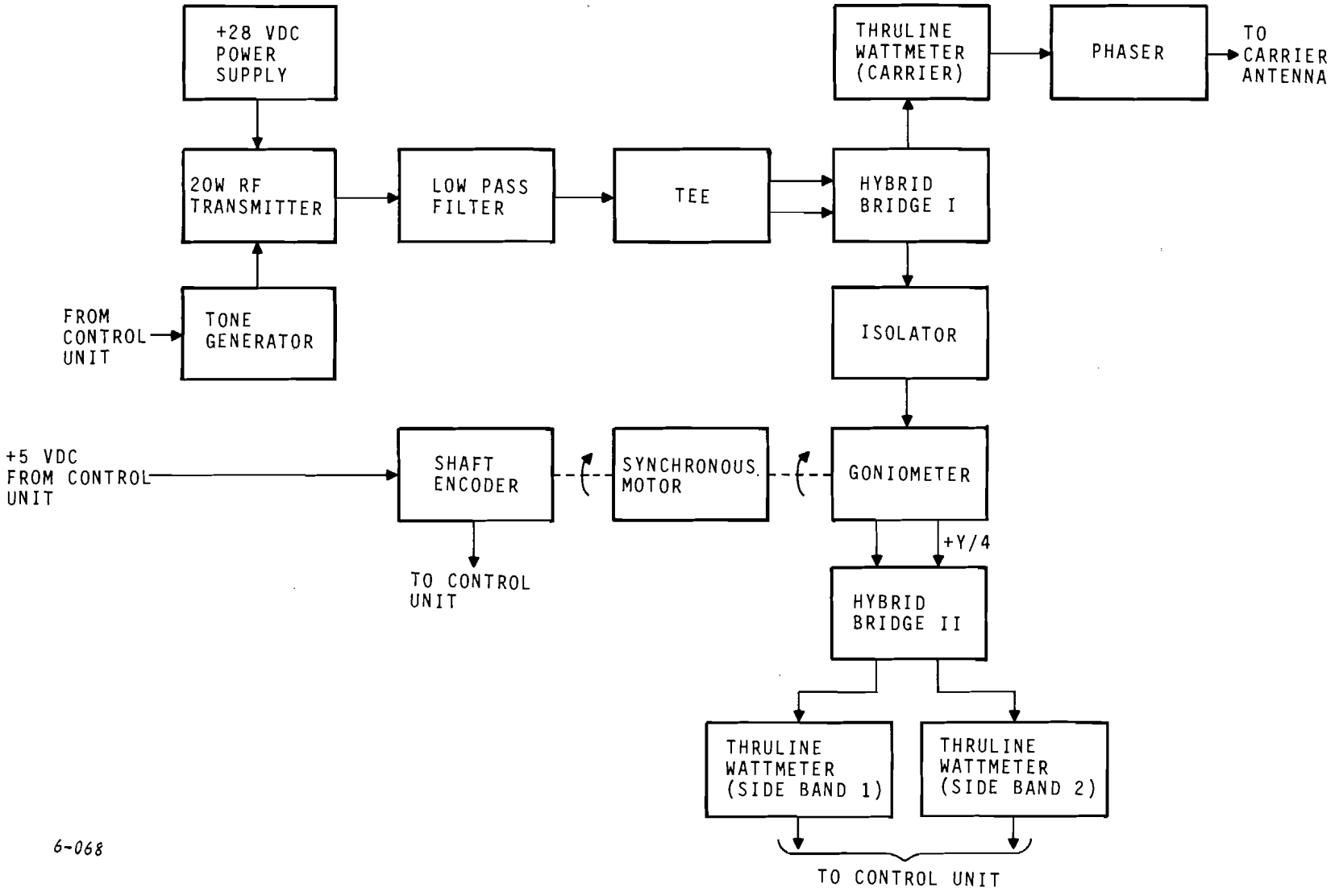


FIGURE 2-9. RF UNIT BLOCK DIAGRAM

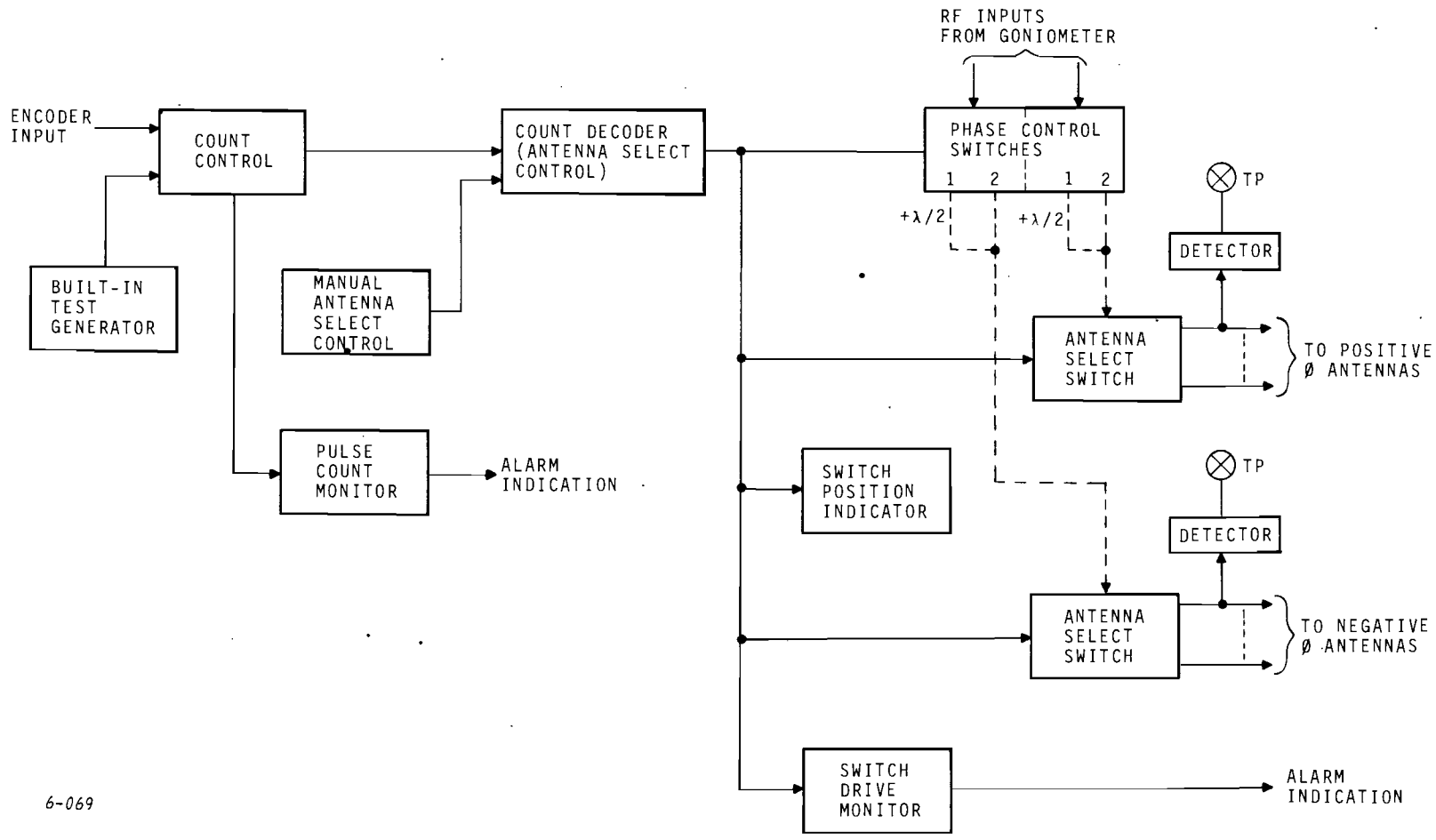


FIGURE 2-10. GROUND CONTROL UNIT BLOCK DIAGRAM

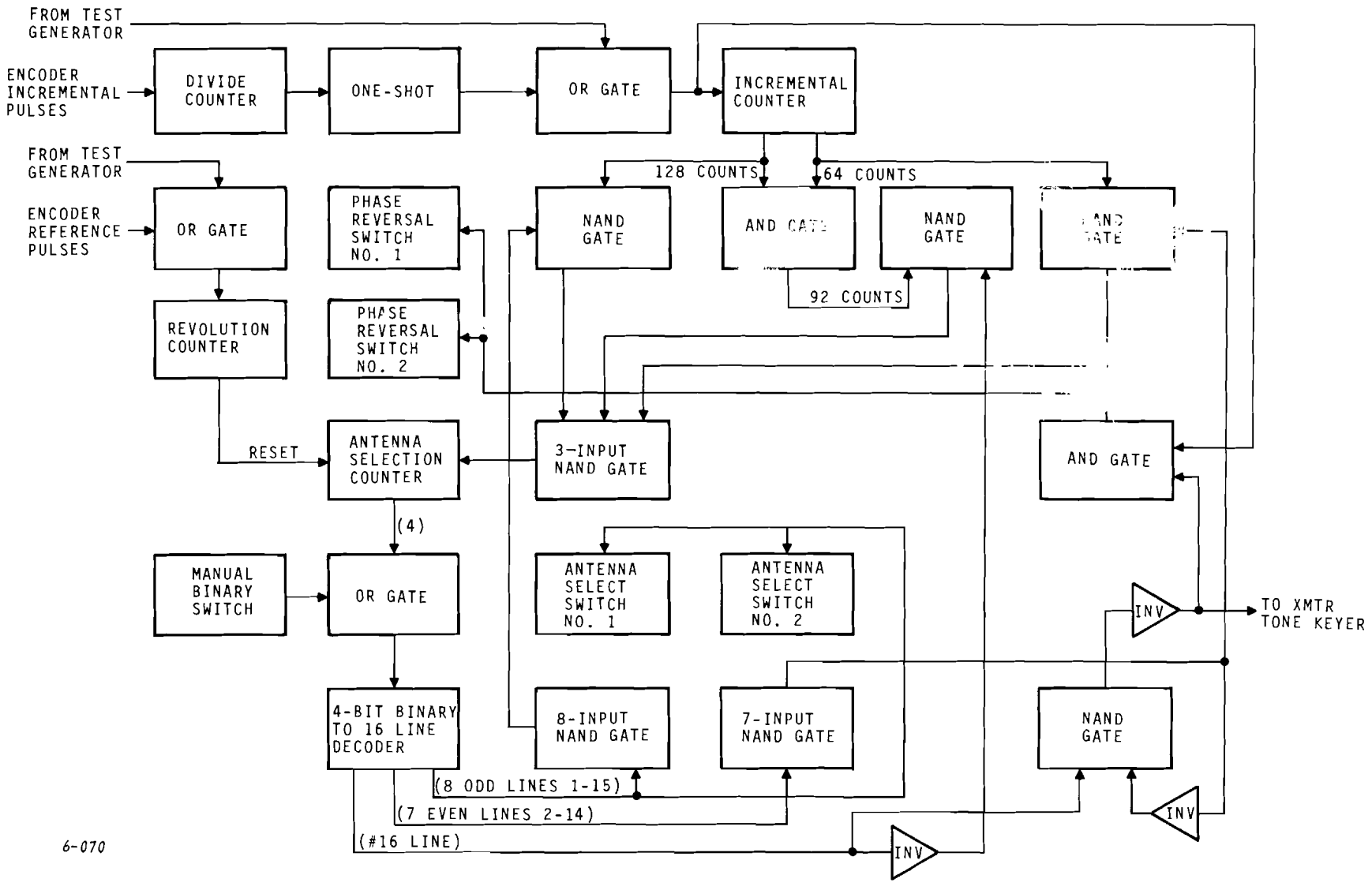


FIGURE 2-11. COUNT CONTROL AND DECODER BLOCK DIAGRAM

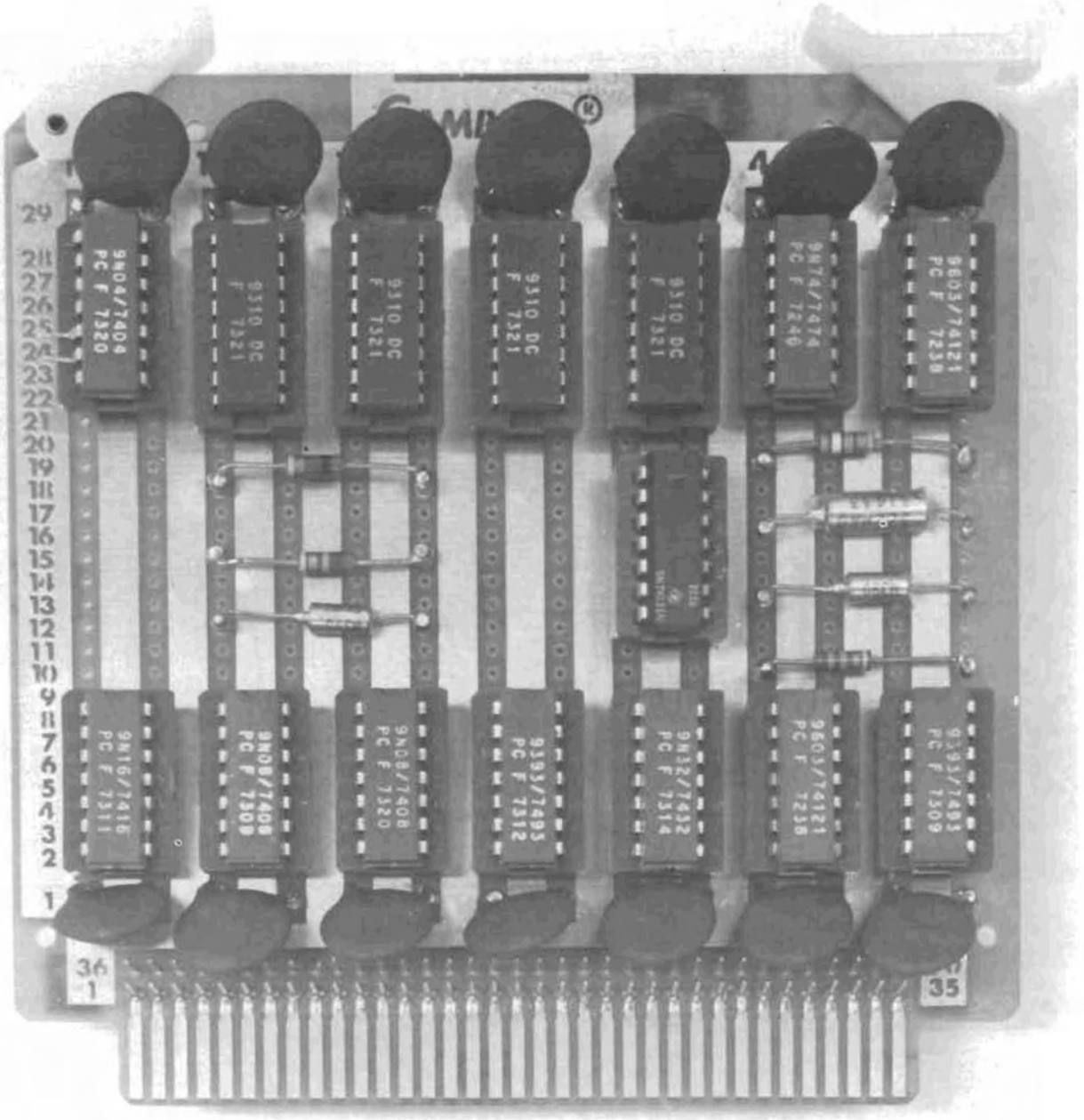


FIGURE 2-12. COUNT CONTROL AND DECODER PC BOARD NO. 1

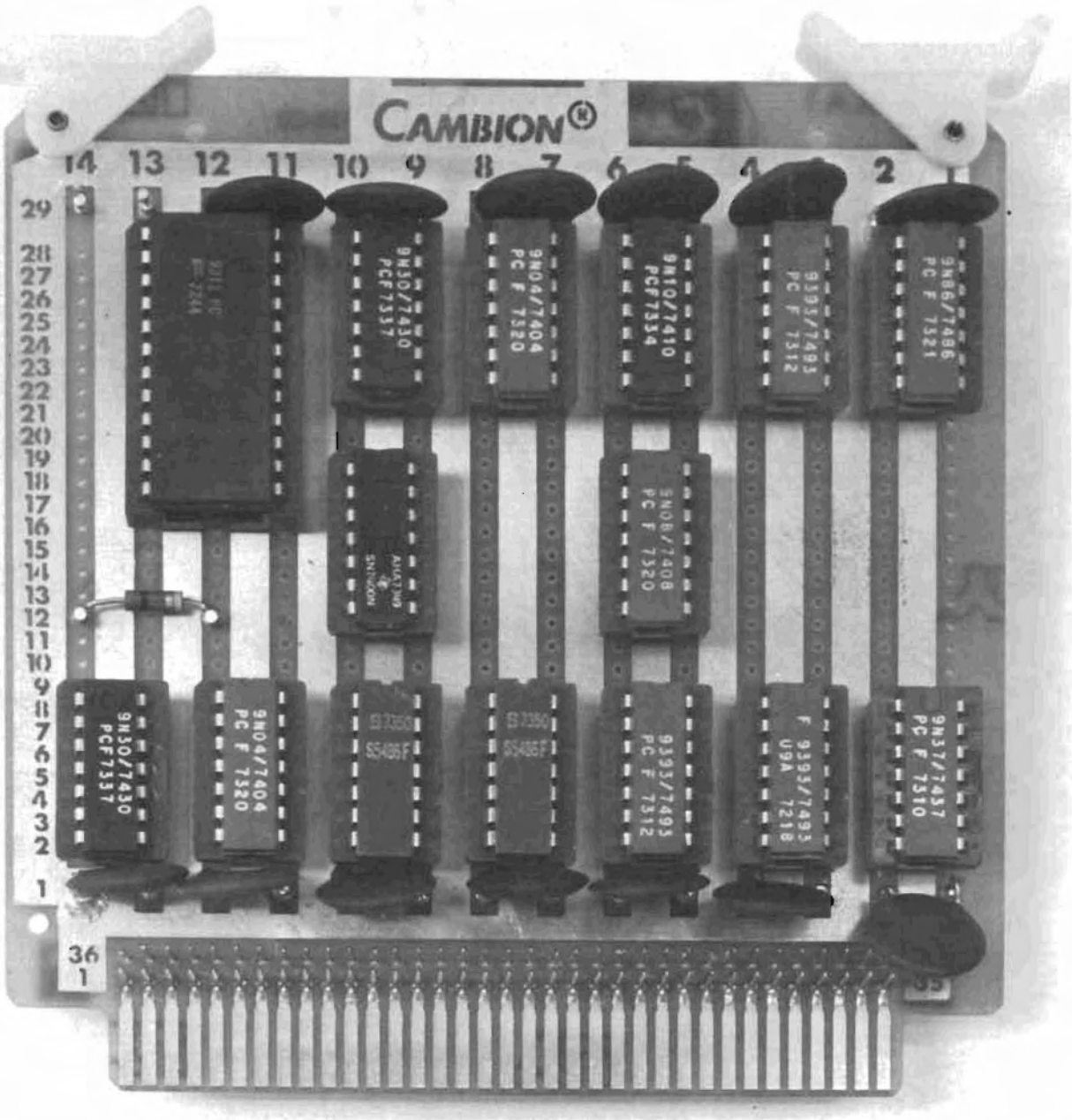
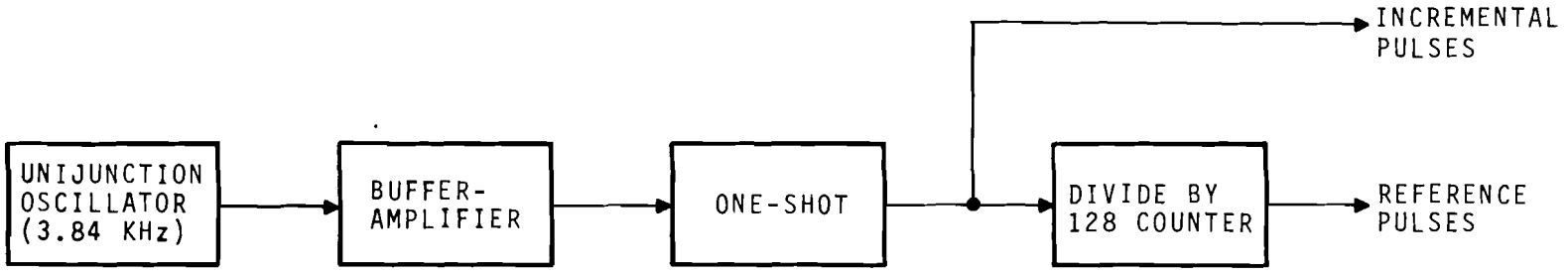


FIGURE 2-13. COUNT CONTROL AND DECODER PC BOARD NO. 2



6-2565

FIGURE 2-14. BUILT IN TEST GENERATOR BLOCK DIAGRAM

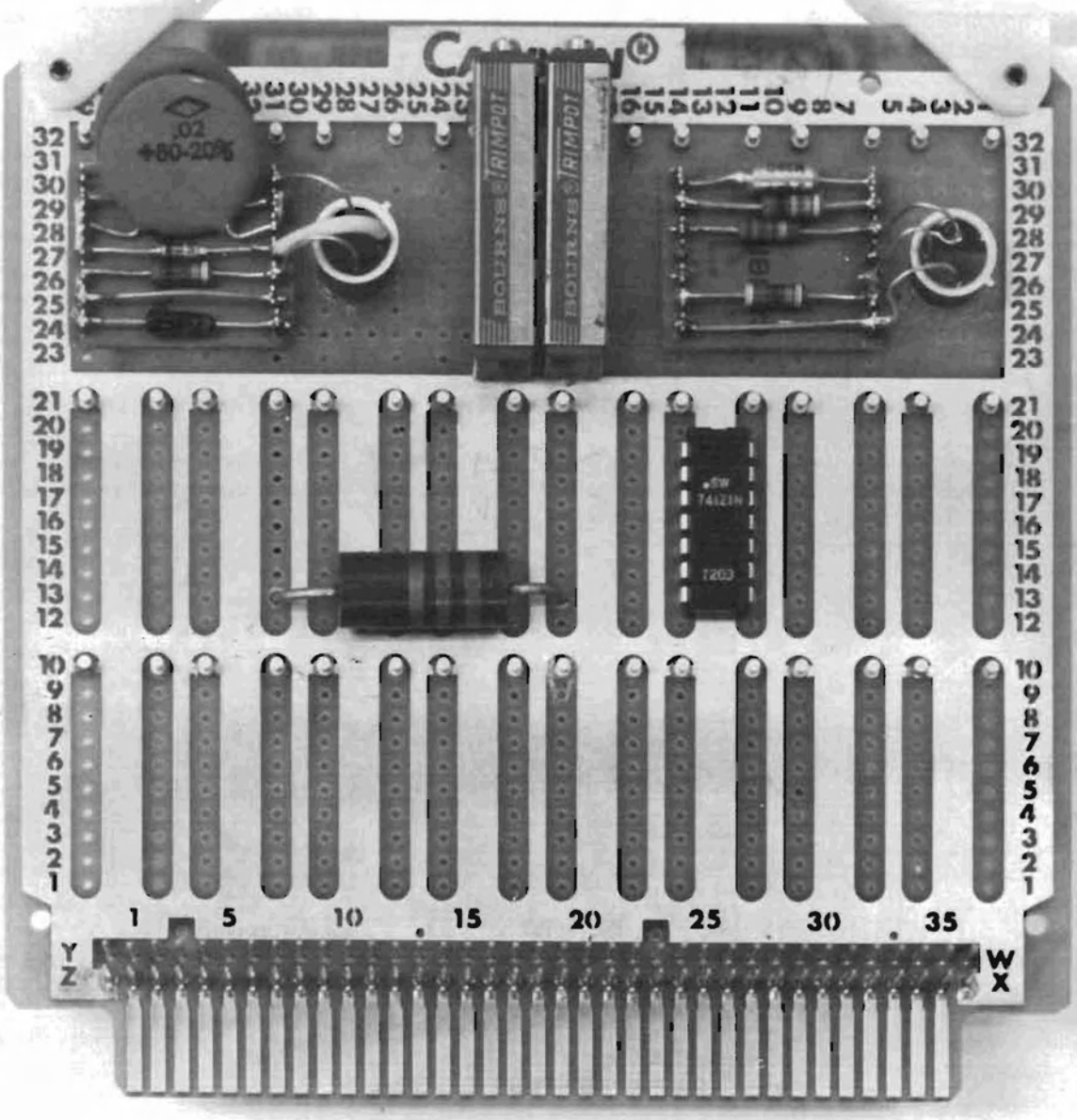
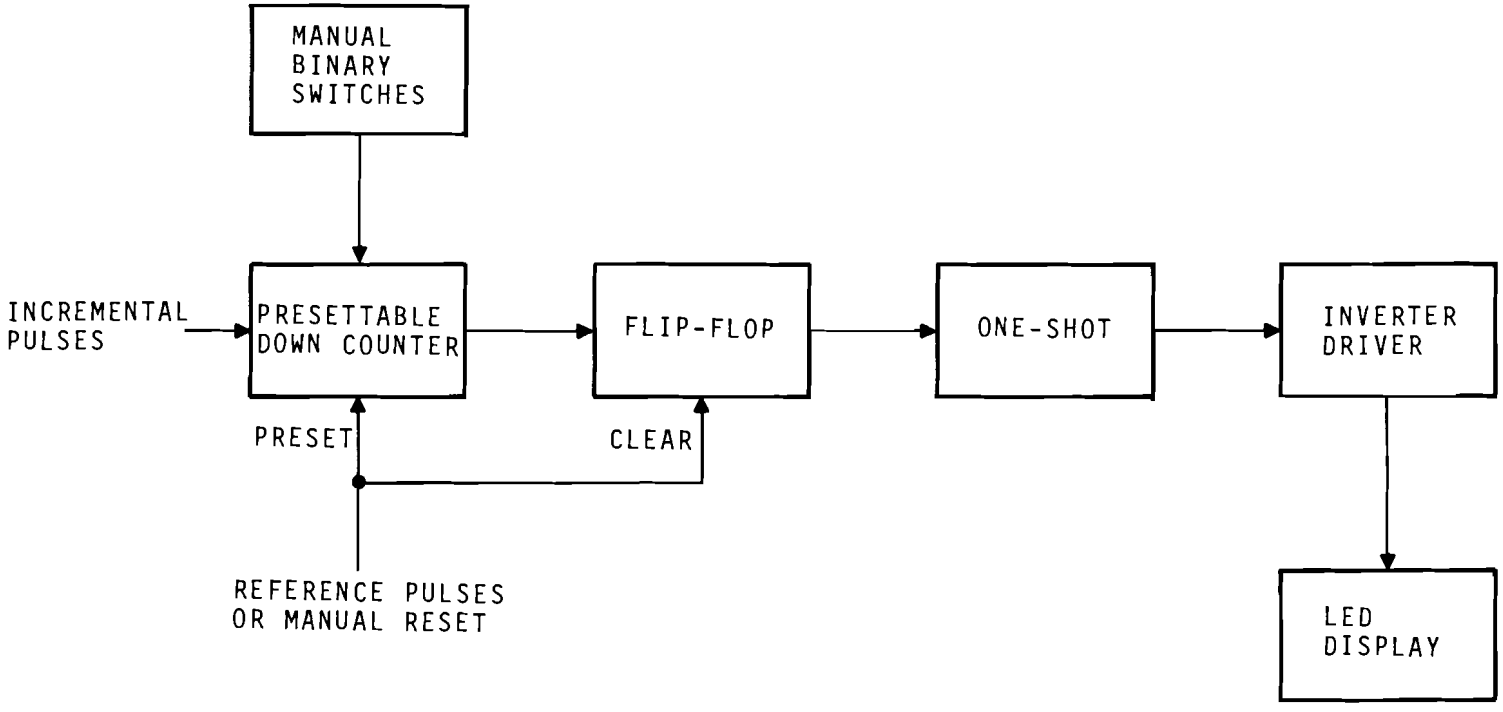


FIGURE 2-15. BUILT IN TEST GENERATOR PC BOARD



6-2567

FIGURE 2-16. PULSE COUNT MONITOR BLOCK DIAGRAM

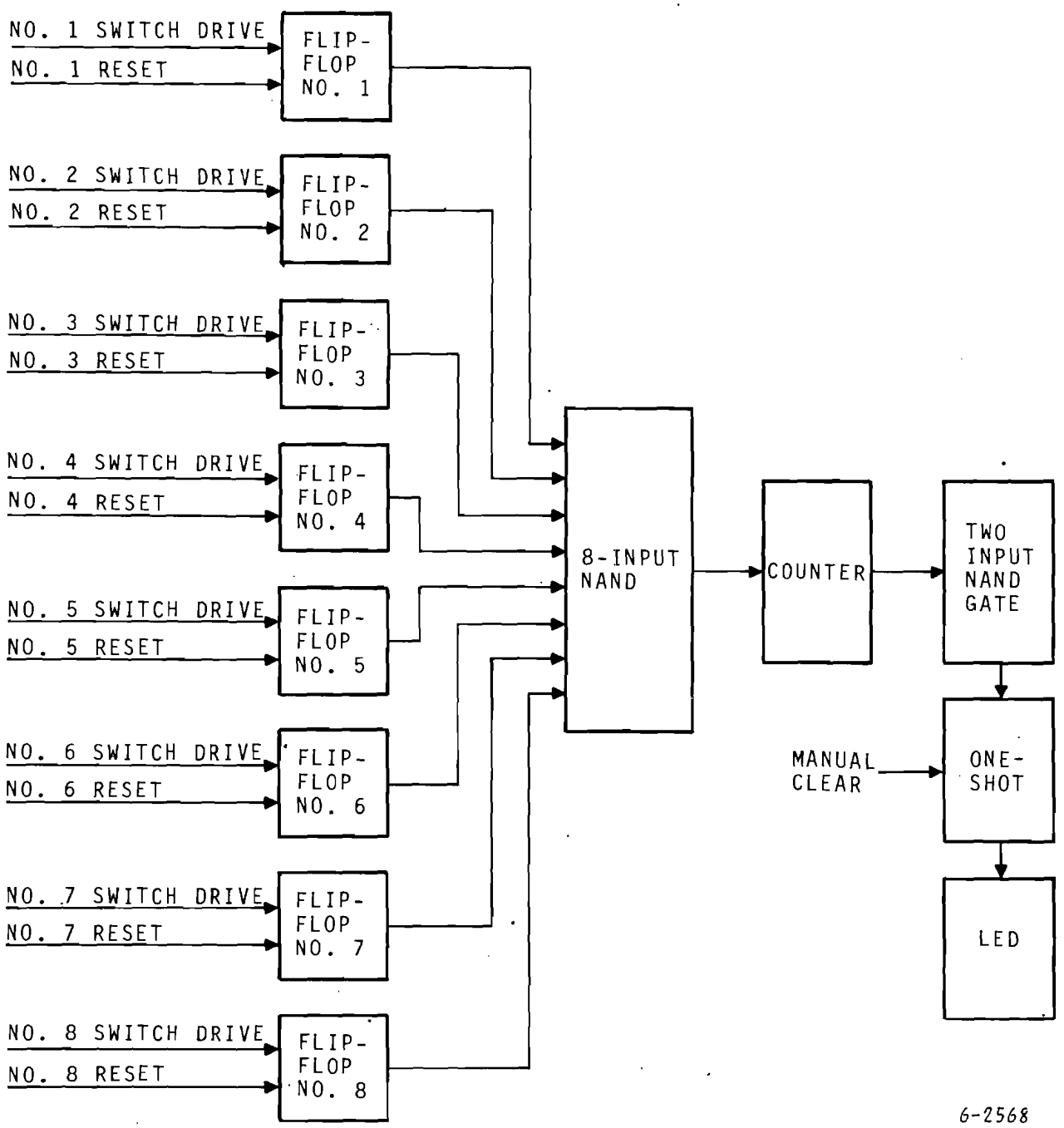


FIGURE 2-17. SWITCH MONITOR BLOCK DIAGRAM

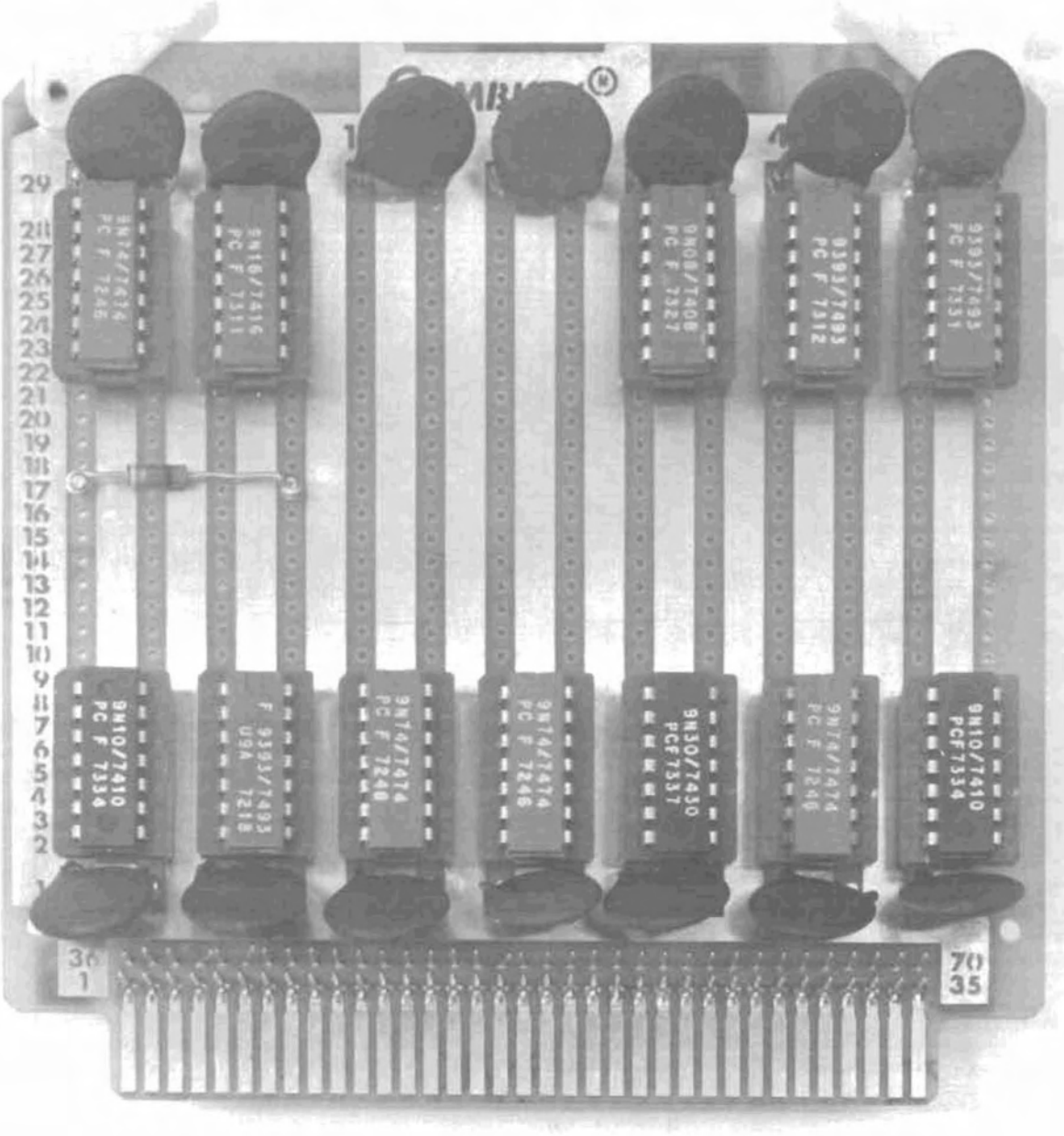


FIGURE 2-18. SWITCH MONITOR PC BOARD

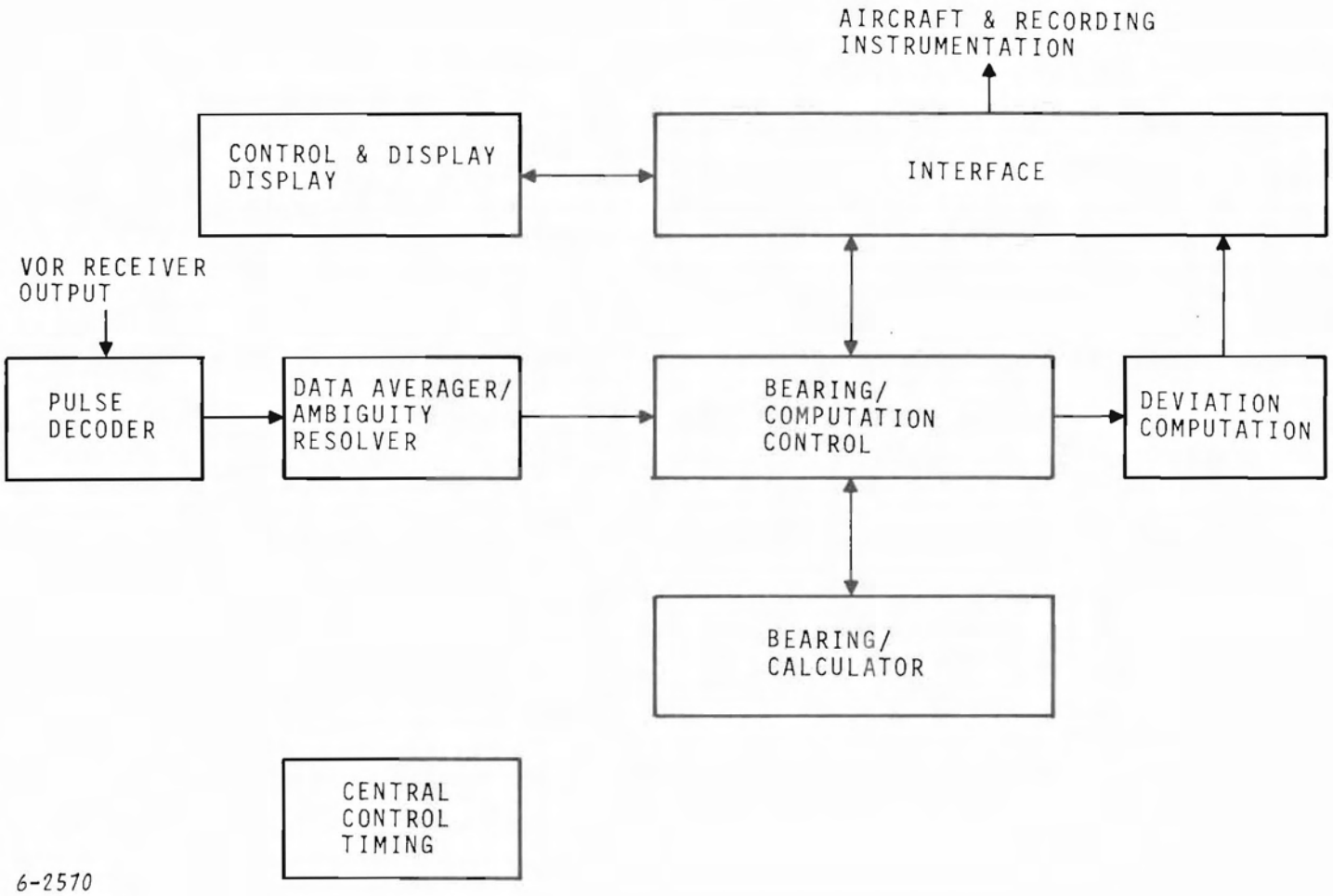


FIGURE 2-19. AIRBORNE PROCESSOR BLOCK DIAGRAM

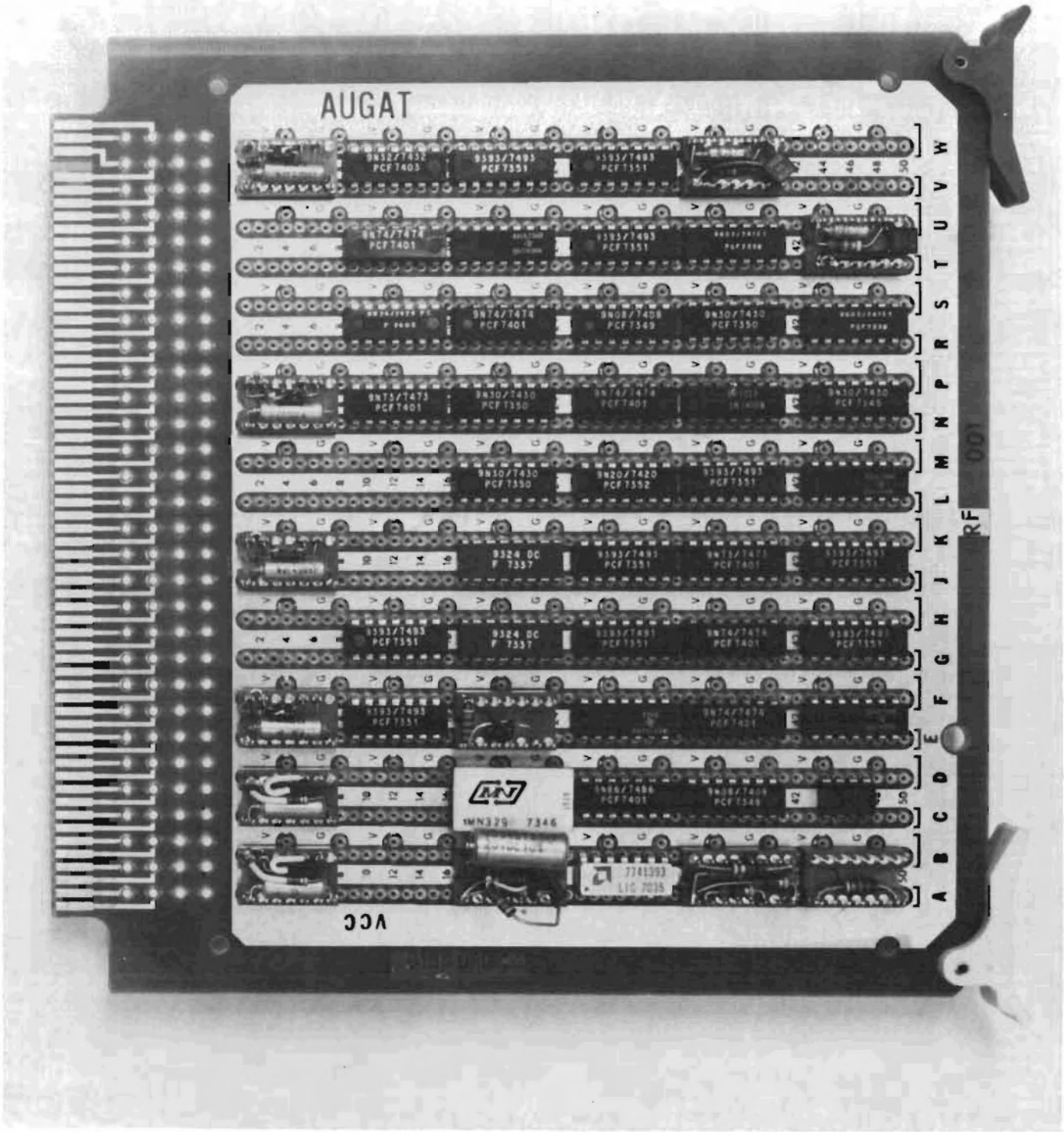


FIGURE 2-20. PULSE DECODER BOARD

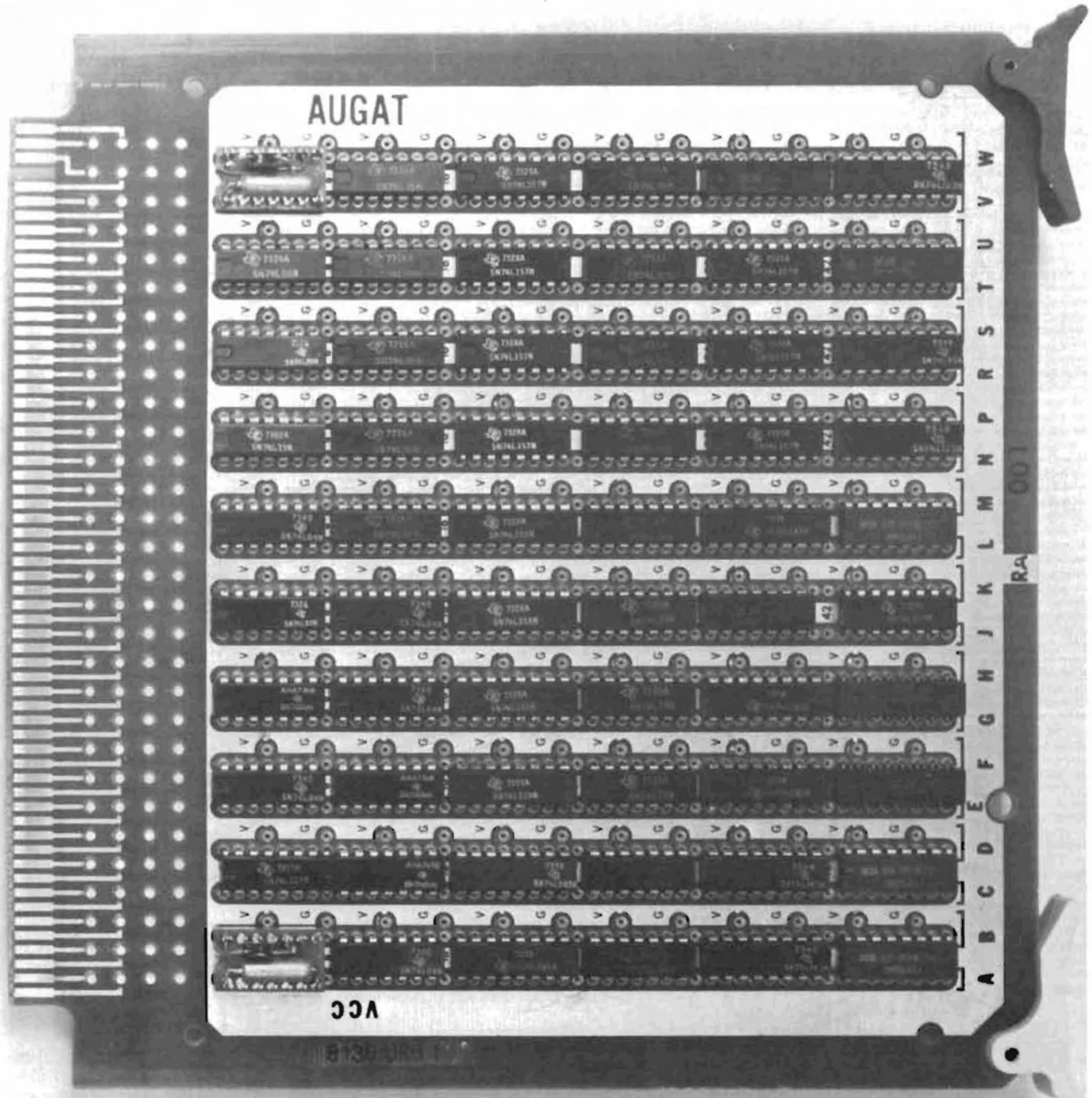


FIGURE 2-21. AMBIGUITY RESOLVER BOARD

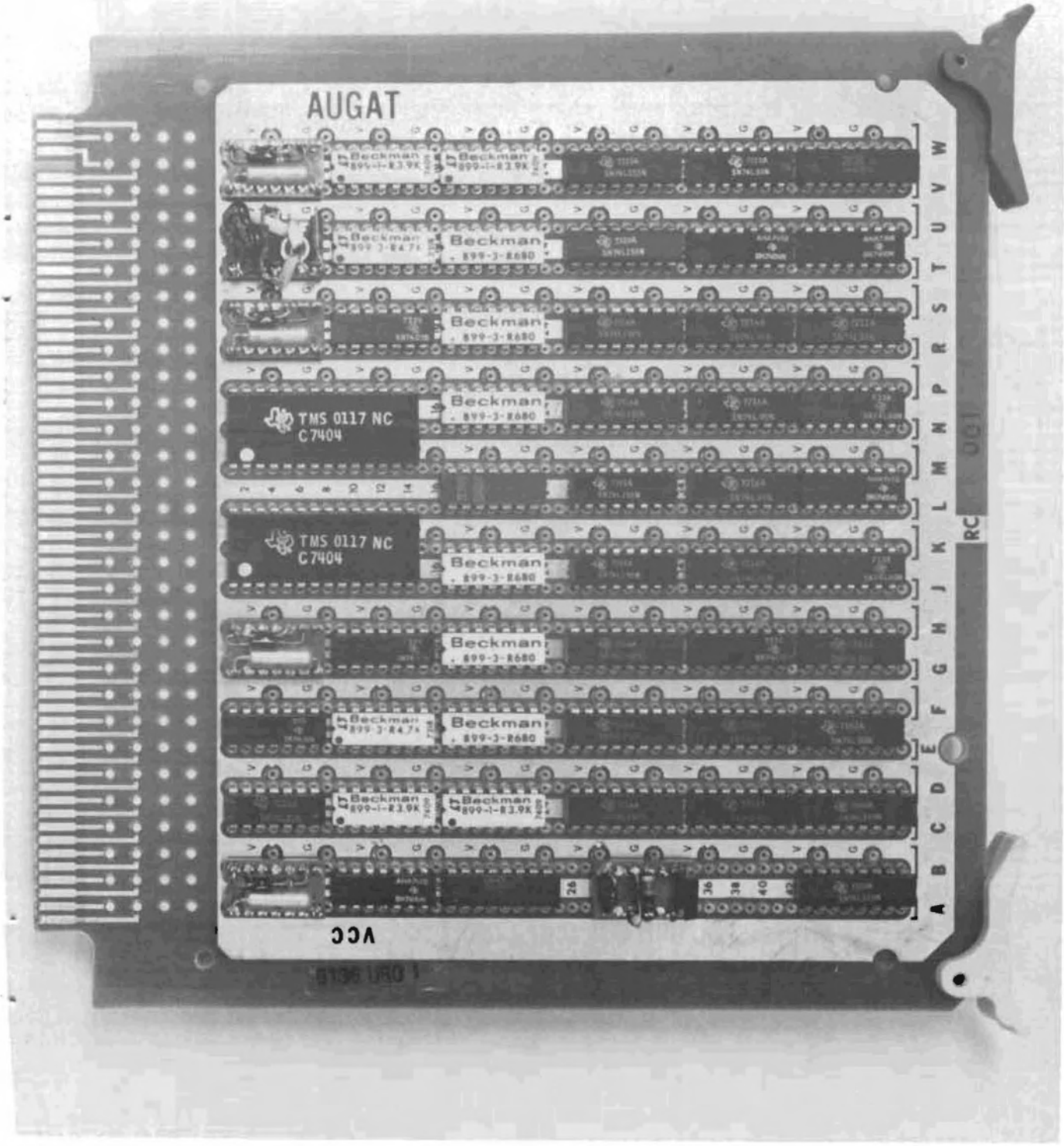


FIGURE 2-22. CALCULATOR BOARD

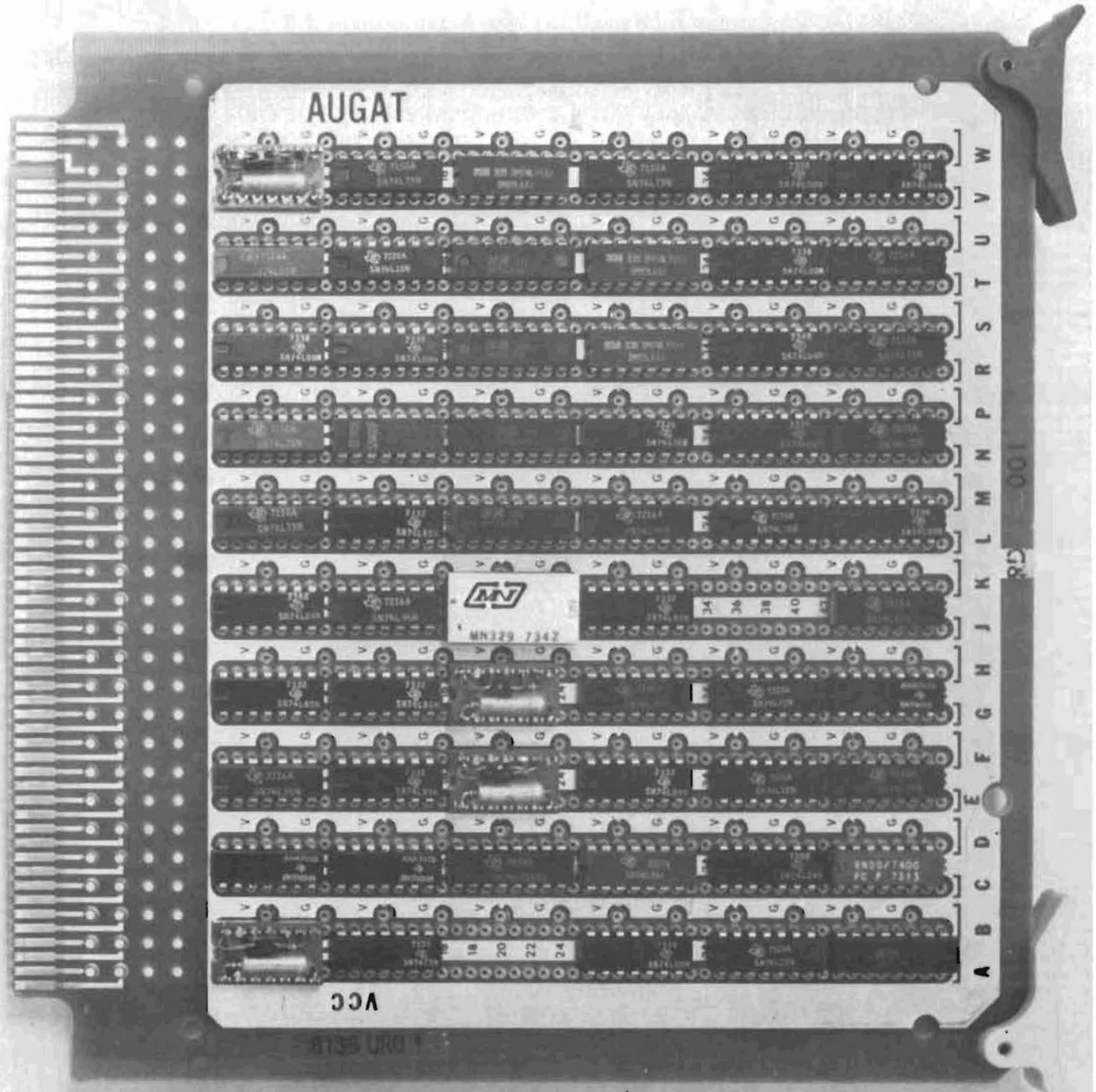


FIGURE 2-23. BEARING BOARD

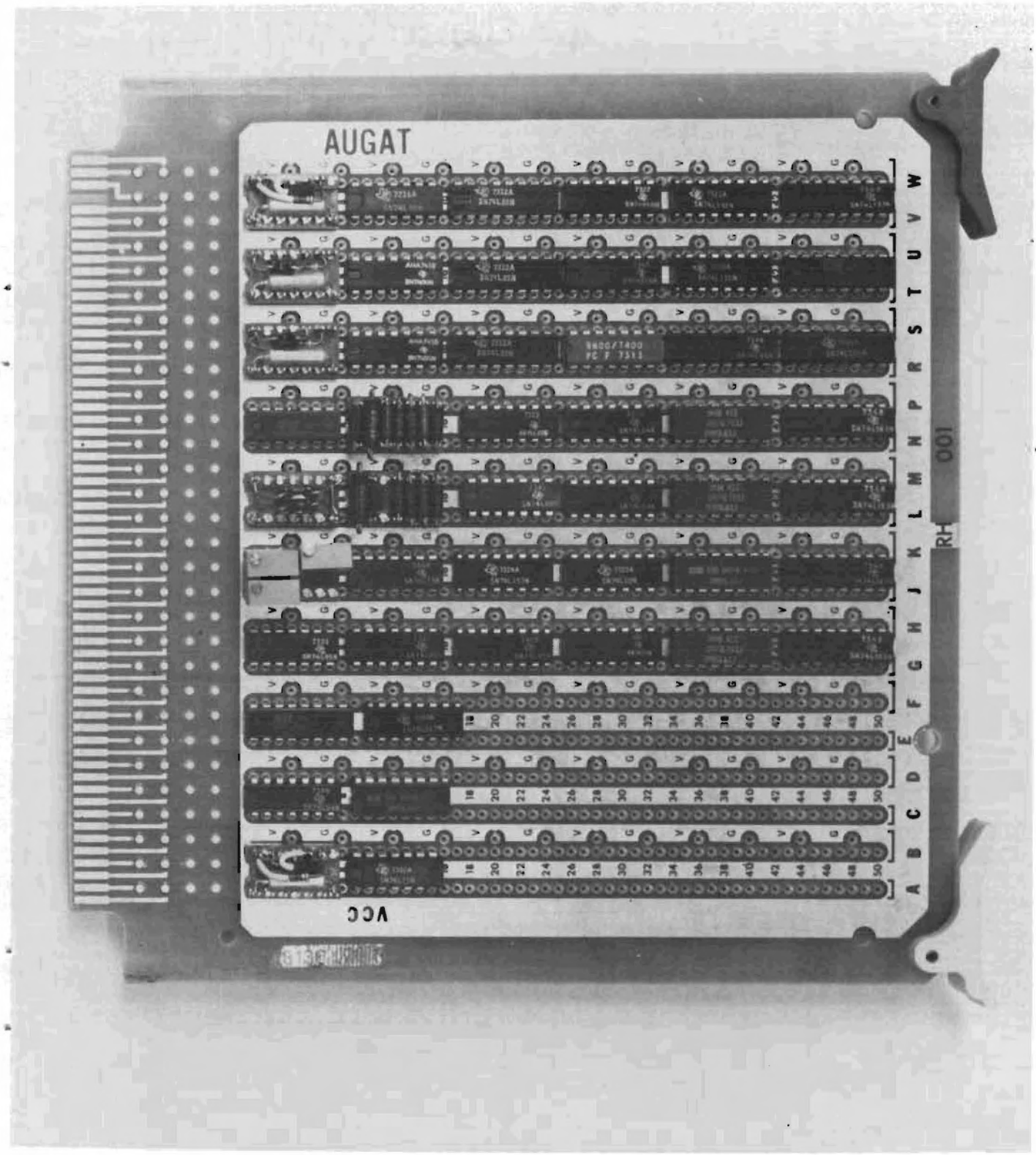


FIGURE 2-24. DEVIATION BOARD

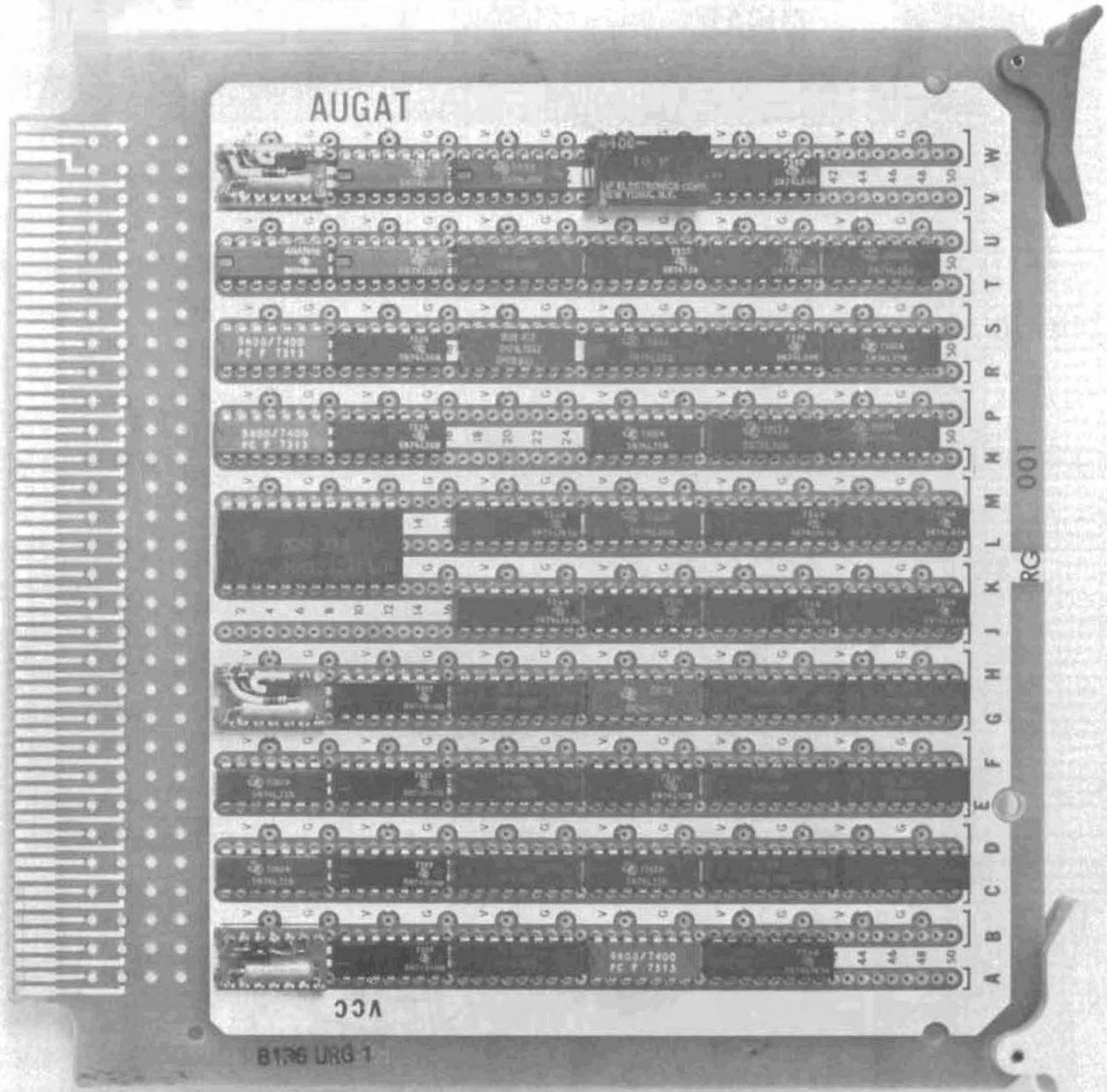


FIGURE 2-25. INTERFACE BOARD

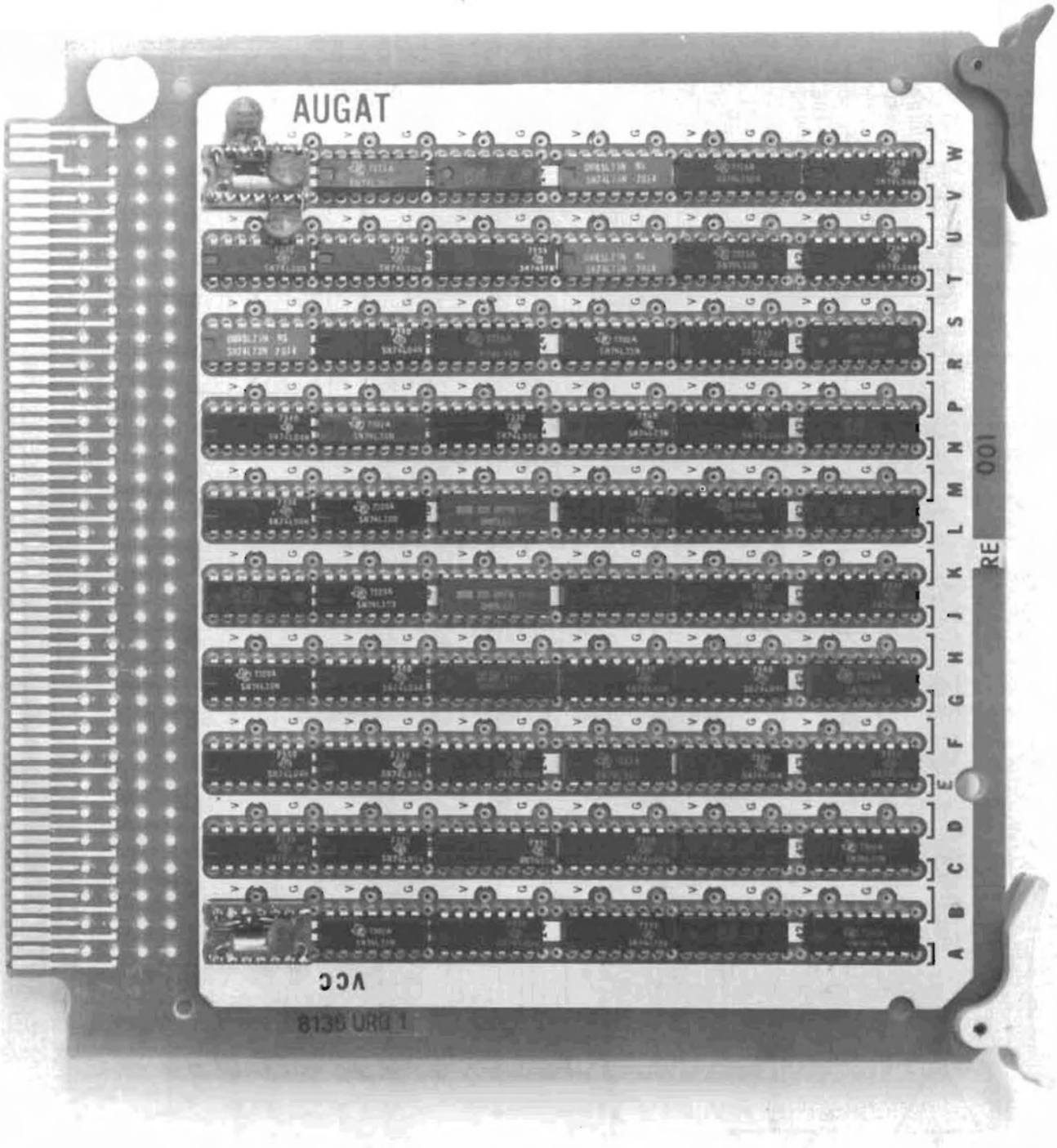


FIGURE 2-26. TIMING AND CONTROL BOARD

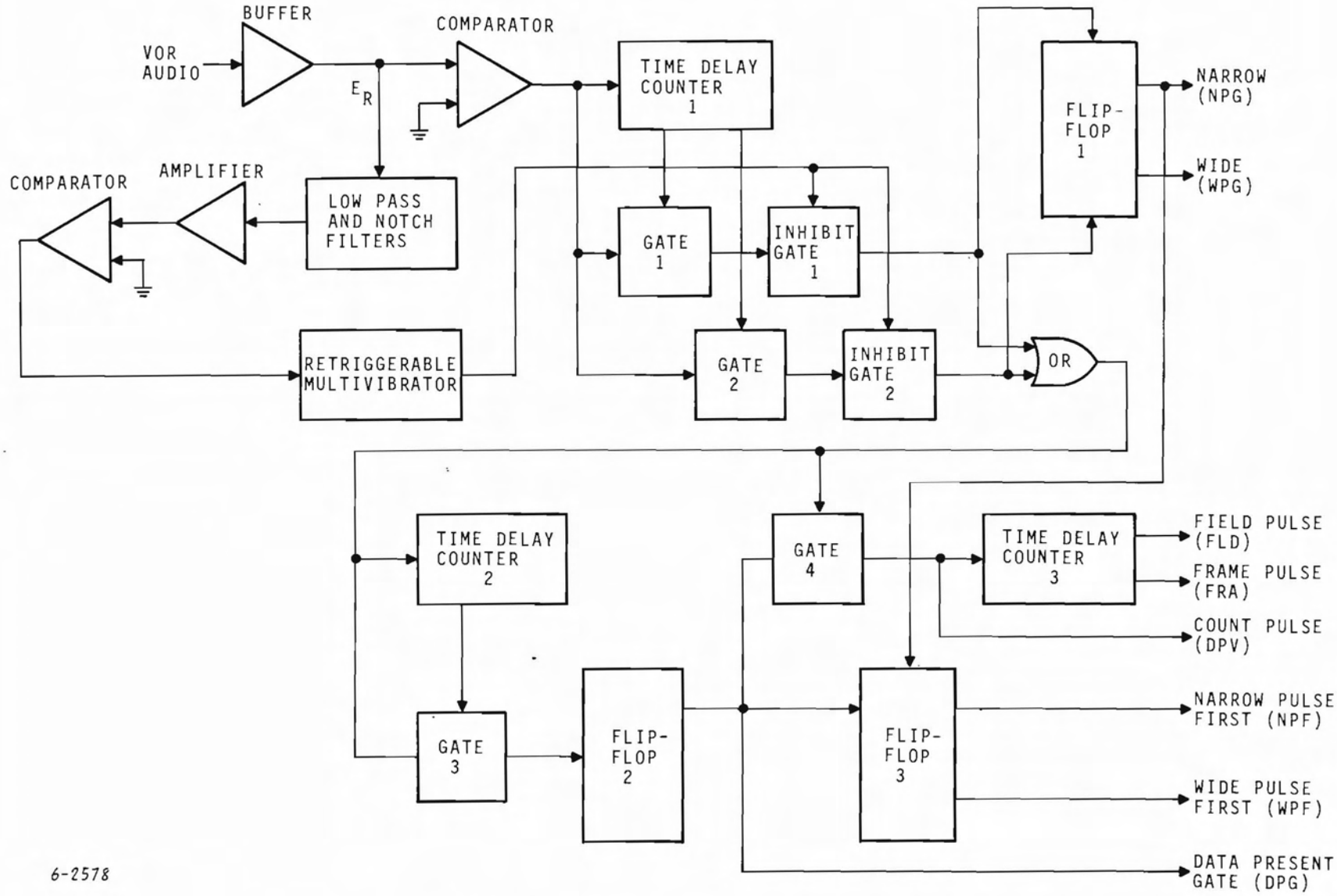


FIGURE 2-27. PULSE DECODER BLOCK DIAGRAM

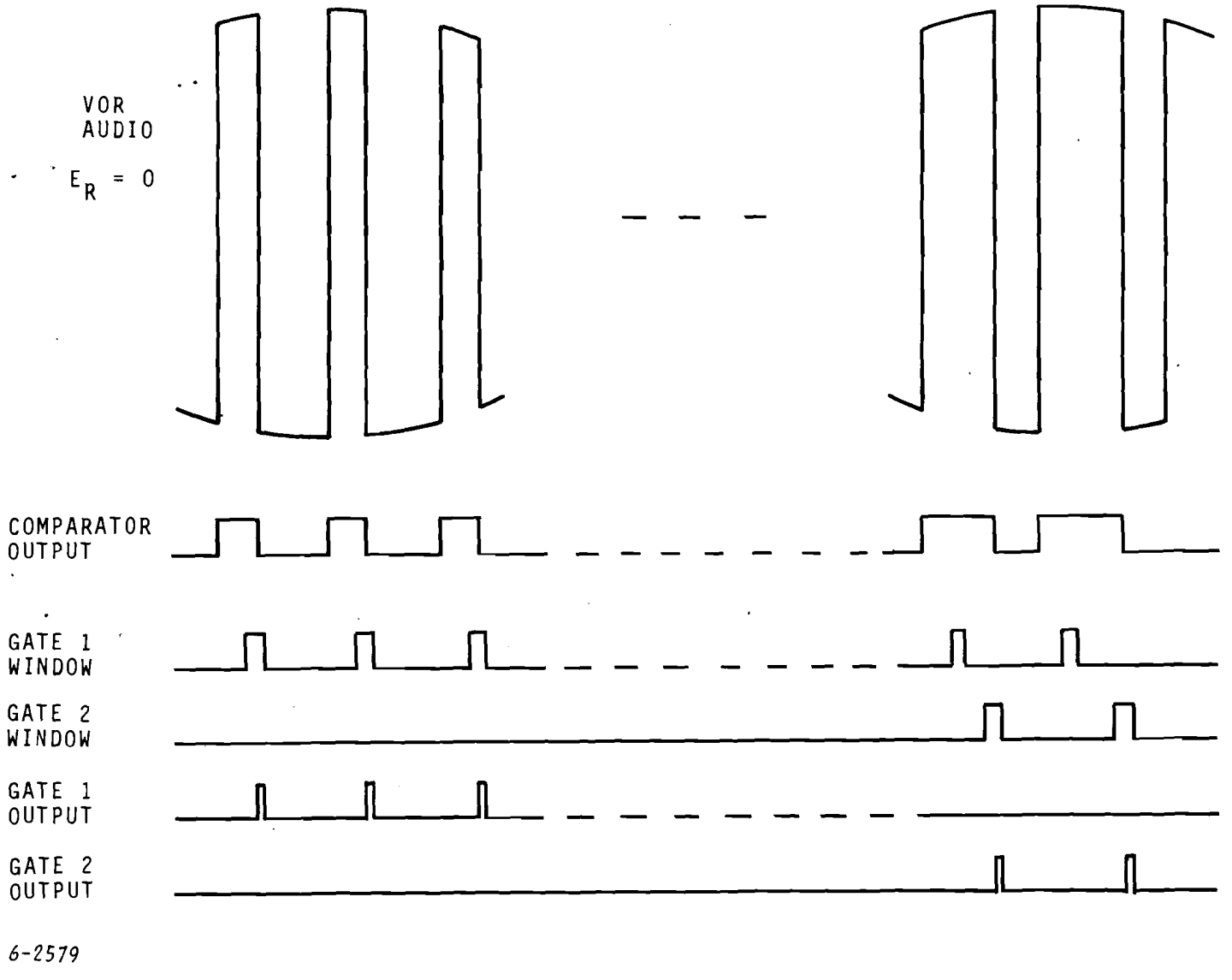


FIGURE 2-28. PULSE DECODER SIGNAL WAVEFORMS

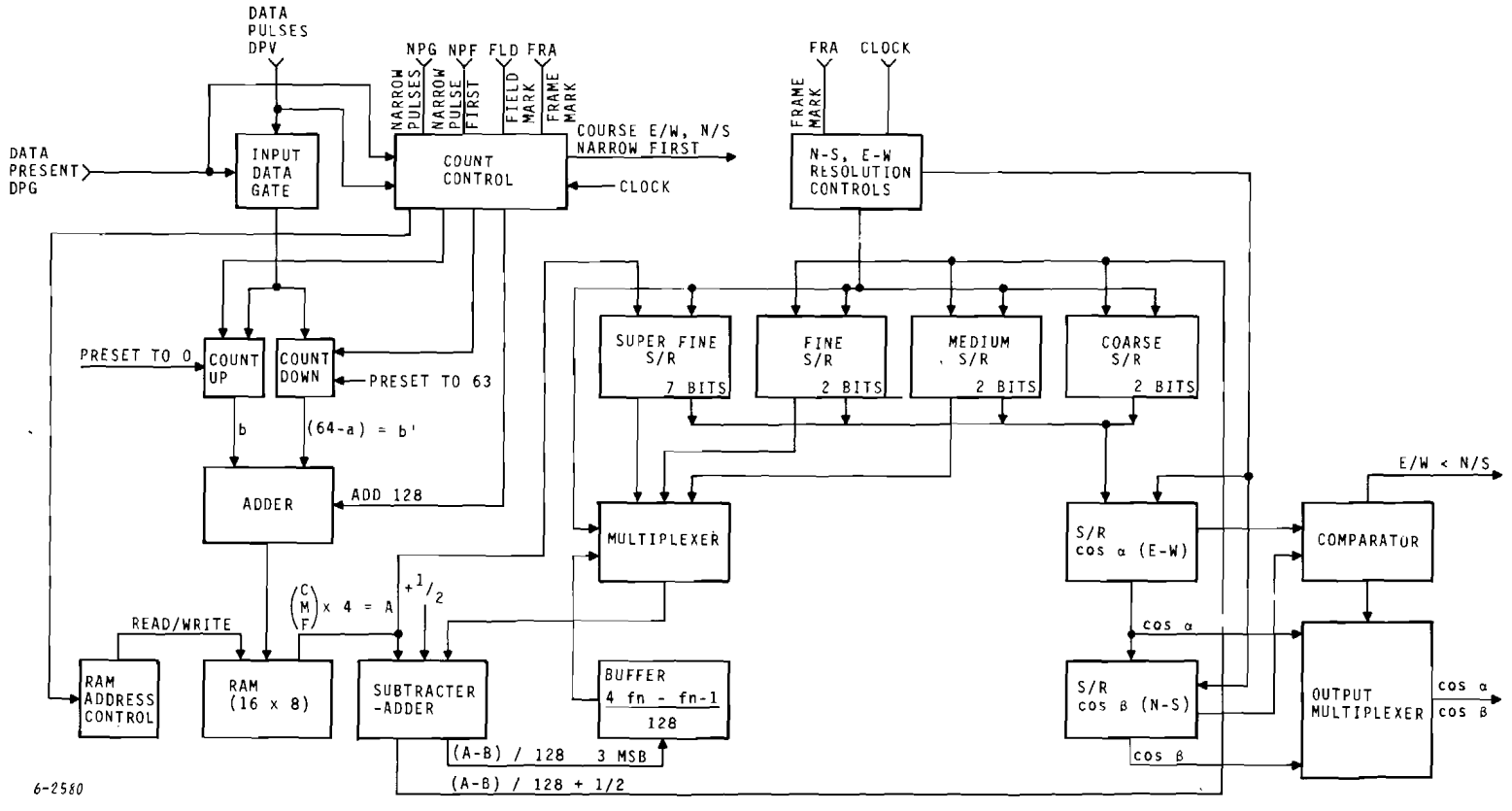


FIGURE 2-29. DATA AVERAGER - AMBIGUITY RESOLVER BLOCK DIAGRAM

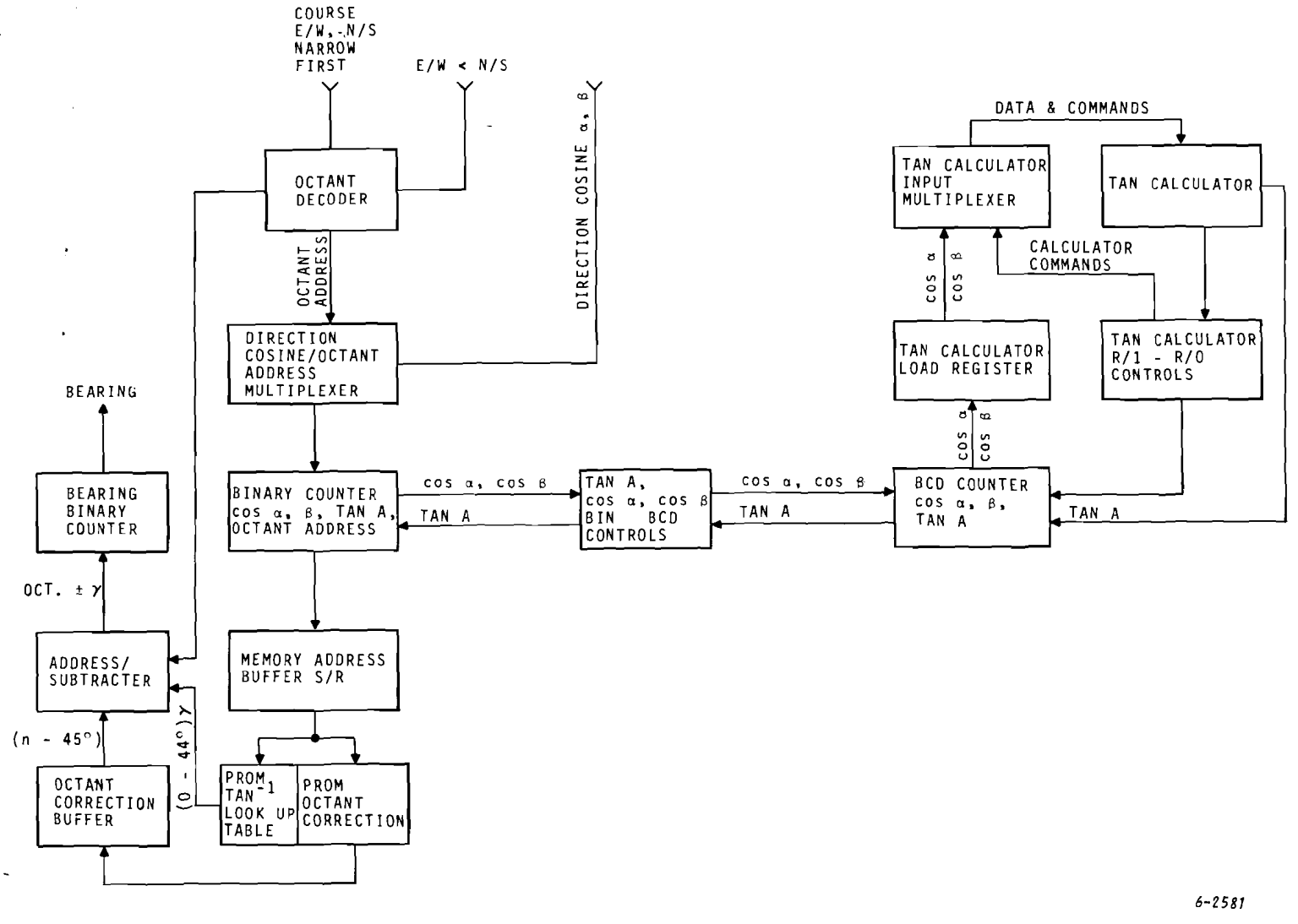
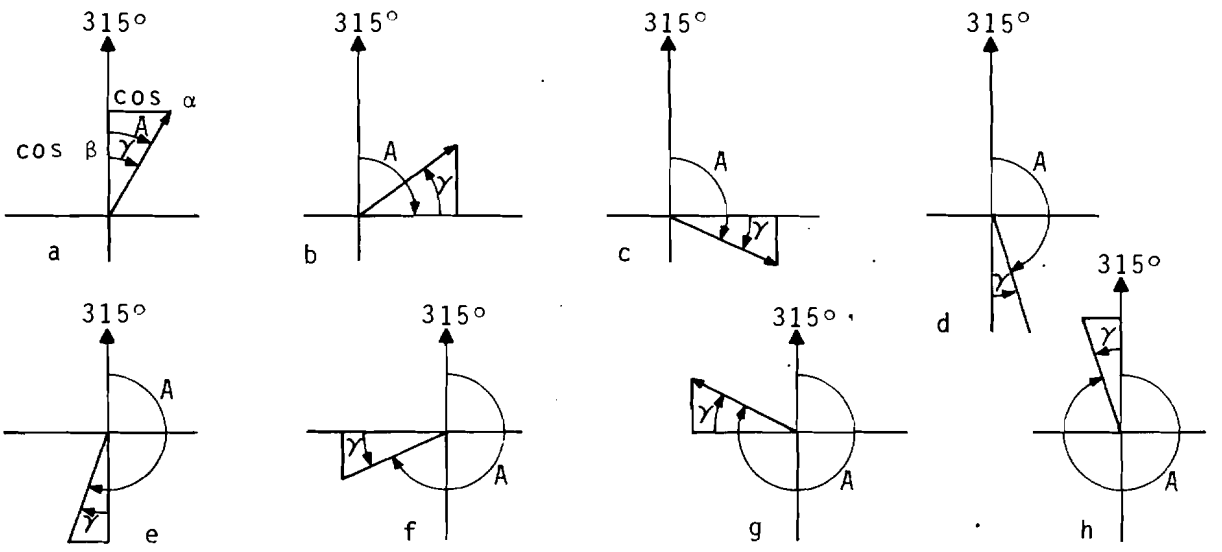


FIGURE 2-30. BEARING CALCULATION BLOCK DIAGRAM



SECTOR	BEARING ANGLE A
a	315° + γ
b	45° - γ
c	45° + γ
d	135° - γ
e	135° + γ
f	225° - γ
g	225° + γ
h	315° - γ

6-2582

FIGURE 2-31. BEARING ANGLE "A" AS A FUNCTION OF γ

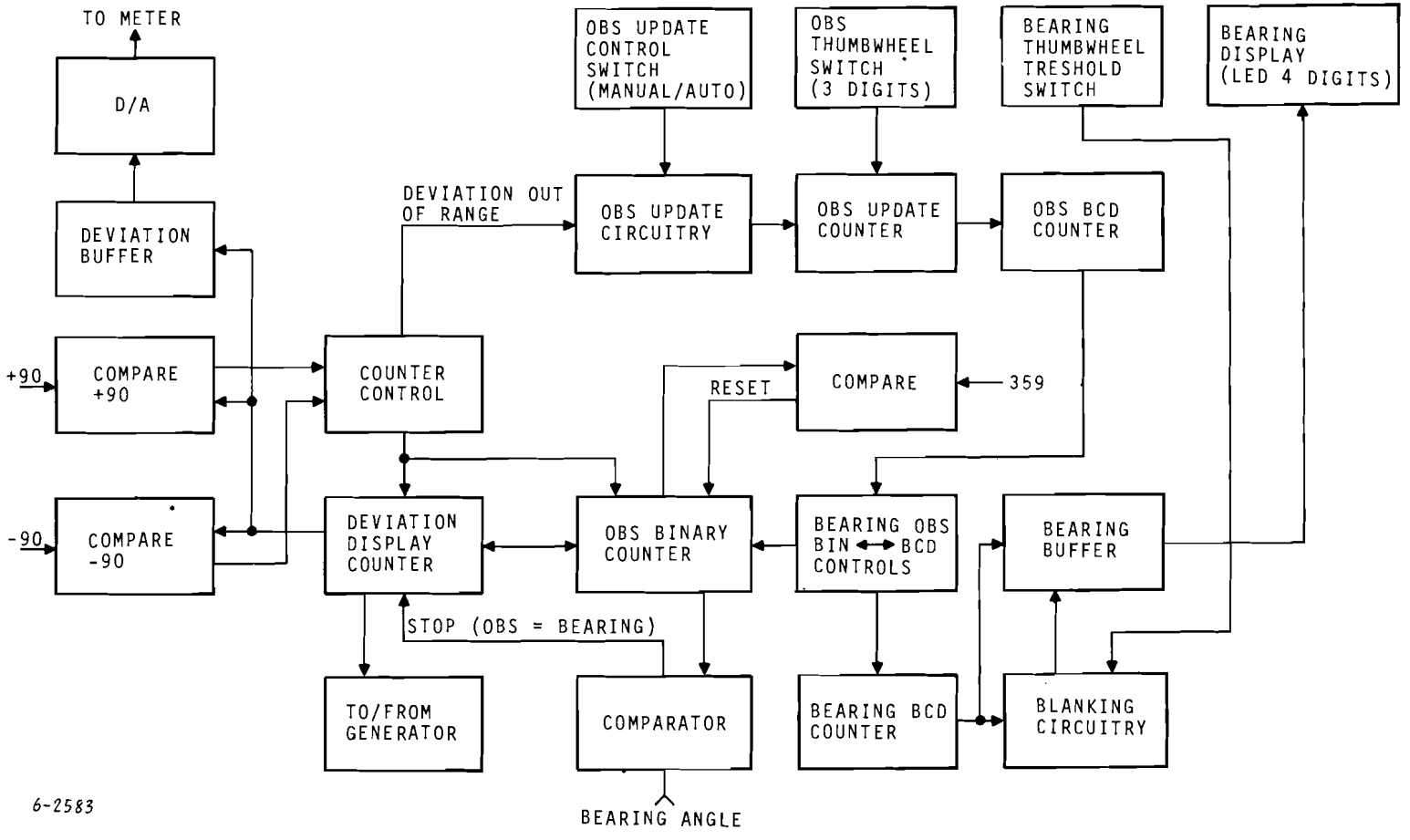


FIGURE 2-32. DEVIATION COMPUTATION BLOCK DIAGRAM

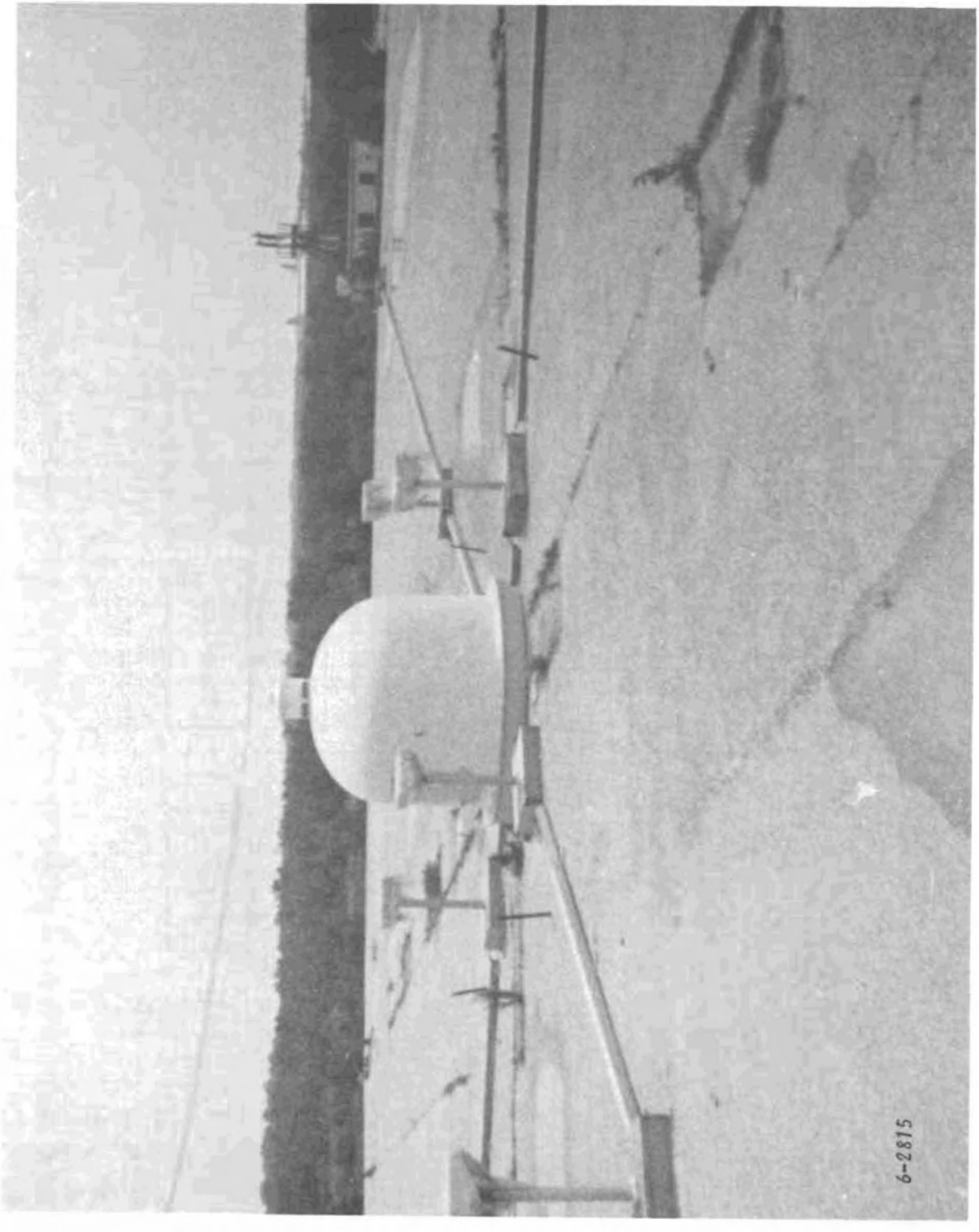


FIGURE 3-1. GROUND STATION

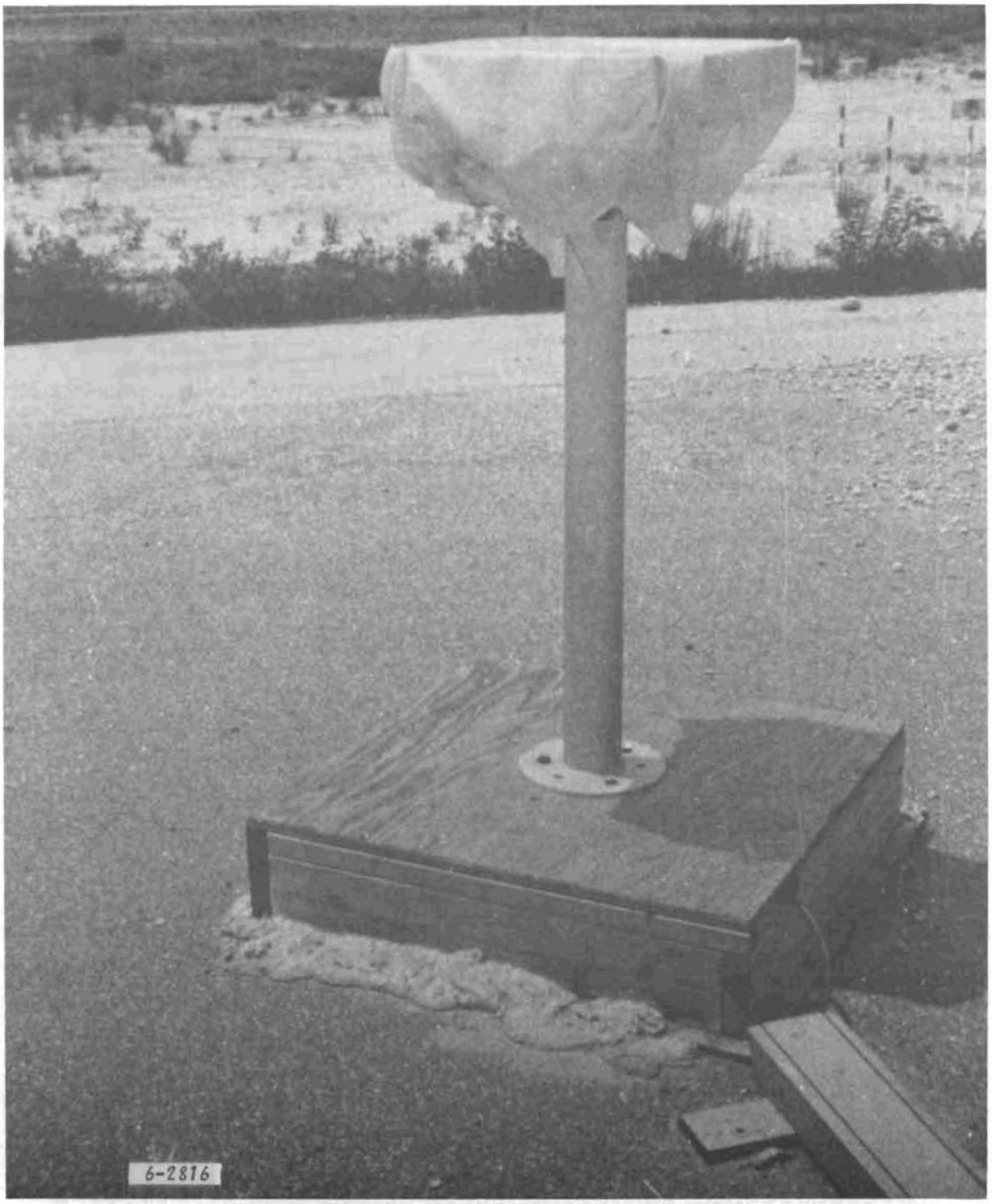


FIGURE 3-2. TRANSMITTING ANTENNA

194 DAY

WIDE APERATURE VOR, PROJECT NUMBER 041-307-000
ROBERT B. FLINT, PROJECT MANAGER, TEST DATA

HR	MIN	SEC	IAND	IAD	IAN1	IAZ	COS1	COS2	BEARING ANGLE	AC1	AC2	AC3	AC4	AC5	AC6	AC7	AC8	ELEVATION	F1	F2	F3	F1	E1	E2	E3	E4	SLANT RANGE	AZIMUTH	HGHT	ELEV
9	53	41.39	-0.269	0	1.536	1	734	6290	66.16	109	33	93	76	119	84	38	111	68	1	0	0	0	0	0	0	0	72025.22	66.05	5775.75	4.45
9	53	41.83	-0.310	0	1.533	1	731	6286	66.09	113	36	93	78	118	84	38	111	19	1	0	0	0	0	0	0	0	72014.86	65.92	5775.25	4.45
9	53	42.26	-0.171	0	1.501	1	727	6287	65.95	112	40	94	78	119	85	39	109	74	1	0	0	0	0	0	0	0	72007.45	65.78	5774.50	4.45
9	53	42.69	-0.415	0	1.519	1	723	6283	65.84	116	44	93	80	117	84	38	112	22	1	0	0	0	0	0	0	0	71998.74	65.65	5769.50	4.45
9	53	43.13	-0.391	0	1.533	1	718	6282	65.70	117	49	95	80	118	85	39	110	72	1	0	0	0	0	0	0	0	71989.87	65.52	5768.25	4.45
9	53	43.56	-0.452	0	1.509	1	713	6279	65.59	120	54	94	80	119	84	38	113	19	1	0	0	0	0	0	0	0	71987.14	65.39	5767.50	4.45
9	53	43.99	-0.603	0	1.558	1	708	6279	65.39	120	59	95	82	119	84	39	110	19	1	0	0	0	0	0	0	0	71984.25	65.26	5767.50	4.45
9	53	44.43	-0.537	0	1.519	1	701	6275	65.30	124	66	95	83	118	85	38	113	19	1	0	0	0	0	0	0	0	71973.96	65.13	5763.25	4.45
9	53	44.86	-0.615	0	1.560	1	696	6269	65.05	2	71	97	84	120	86	39	110	29	1	0	0	0	0	0	0	0	71966.96	65.00	5762.50	4.45
9	53	45.29	-0.598	0	1.538	1	691	6270	64.89	1	76	96	85	118	85	40	111	19	1	0	0	0	0	0	0	0	71958.32	64.87	5761.00	4.44
9	53	45.73	-0.576	0	1.553	1	687	6268	64.73	3	80	97	86	119	88	38	111	129	1	0	0	0	0	0	0	0	71953.95	64.74	5761.25	4.44
9	53	46.16	-0.242	0	1.531	1	681	6267	64.64	4	86	96	87	118	86	41	112	19	1	0	0	0	0	0	0	0	71952.90	64.61	5760.50	4.44
9	53	46.59	0.134	0	1.543	1	679	6264	64.44	7	88	97	89	120	88	39	111	114	1	0	0	0	0	0	0	0	71950.50	64.49	5760.50	4.44
9	53	47.03	0.564	0	1.536	1	674	6263	64.39	8	93	97	90	118	86	40	114	24	1	0	0	0	0	0	0	0	71948.12	64.36	5759.75	4.44
9	53	47.46	0.498	0	1.543	1	673	6261	64.23	10	94	98	90	120	89	39	112	110	1	0	0	0	0	0	0	0	71951.41	64.23	5759.25	4.44
9	53	47.89	0.771	0	1.506	1	667	6260	64.19	11	100	97	92	119	86	39	113	19	1	0	0	0	0	0	0	0	71943.13	64.10	5762.25	4.45
9	53	48.33	0.723	0	1.560	1	666	6257	64.03	14	101	98	93	121	88	40	112	20	1	0	0	0	0	0	0	0	71946.88	63.97	5762.50	4.45
9	53	48.76	0.818	0	1.521	1	660	6257	63.97	14	107	97	94	120	87	39	112	130	1	0	0	0	0	0	0	0	71938.57	63.84	5761.50	4.45
9	53	49.19	0.937	0	1.550	1	656	6255	63.83	16	111	99	93	121	90	40	113	19	1	0	0	0	0	0	0	0	71936.35	63.72	5761.75	4.45
9	53	49.63	0.854	0	1.536	1	653	6252	63.67	19	114	98	96	121	87	40	114	114	1	0	0	0	0	0	0	0	71935.31	63.54	5768.25	4.45
9	53	50.06	0.703	0	1.550	1	646	6252	63.56	19	121	99	96	121	90	40	113	19	1	0	0	0	0	0	0	0	71937.96	63.46	5768.75	4.45
9	53	50.50	0.681	0	1.560	1	642	6250	63.41	21	125	98	98	120	88	39	110	72	1	0	0	0	0	0	0	0	71935.86	63.33	5768.75	4.45
9	53	50.93	0.625	0	1.545	1	634	6249	63.25	22	5	100	99	122	90	39	114	24	1	0	0	0	0	0	0	0	71933.94	63.20	5769.25	4.45
9	53	51.36	0.583	0	1.562	1	630	6248	63.05	23	9	100	100	121	89	41	113	150	1	0	0	0	0	0	0	0	71938.00	63.07	5772.50	4.45
9	53	51.80	0.659	0	1.543	1	625	6246	62.94	25	14	100	101	121	90	39	113	22	1	0	0	0	0	0	0	0	71941.47	62.94	5772.00	4.45
9	53	52.23	0.474	0	1.533	1	620	6246	62.78	25	19	101	101	121	90	39	113	19	1	0	0	0	0	0	0	0	71946.02	62.81	5773.25	4.46
9	53	52.66	0.286	0	1.558	1	616	6244	62.64	27	23	100	102	121	91	39	113	129	1	0	0	0	0	0	0	0	71949.98	62.68	5775.25	4.46
9	53	53.10	0.430	0	1.570	1	613	6244	62.53	27	26	101	103	121	91	39	113	19	1	0	0	0	0	0	0	0	71954.11	62.54	5775.75	4.46
9	53	53.53	0.269	0	1.541	1	610	6242	62.42	29	29	100	104	121	91	40	115	29	1	0	0	0	0	0	0	0	71958.11	62.42	5775.50	4.46
9	53	53.96	0.330	0	1.519	1	607	6241	62.31	30	32	101	104	122	91	40	114	24	1	0	0	0	0	0	0	0	71959.79	62.28	5777.75	4.46
9	53	54.40	0.156	0	1.570	1	604	6240	62.27	31	35	101	106	122	90	40	113	114	1	0	0	0	0	0	0	0	71966.99	62.15	5779.75	4.46
9	53	54.83	0.336	0	1.545	1	600	6239	62.16	32	39	102	106	123	92	40	113	19	1	0	0	0	0	0	0	0	71971.48	62.02	5777.00	4.46
9	53	55.27	0.327	0	1.514	1	596	6238	62.06	33	43	101	107	121	91	40	114	70	1	0	0	0	0	0	0	0	71975.94	61.89	5780.00	4.46
9	53	55.70	0.391	0	1.516	1	591	6237	61.95	34	48	101	108	0	92	38	114	19	1	0	0	0	0	0	0	0	71980.19	61.76	5779.25	4.46
9	53	56.13	0.342	0	1.523	1	585	6235	61.80	36	54	102	108	122	92	40	114	69	1	0	0	0	0	0	0	0	71985.18	61.62	5779.75	4.46
9	53	56.57	0.752	0	1.494	1	579	6235	61.64	36	60	103	110	1	93	40	113	19	1	0	0	0	0	0	0	0	71989.77	61.49	5779.75	4.46
9	53	57.00	0.498	0	1.521	1	570	6235	61.48	36	69	103	111	124	92	39	116	148	1	0	0	0	0	0	0	0	71994.28	61.36	5779.75	4.46
9	53	57.43	0.576	0	1.484	1	569	6234	61.22	37	70	103	111	122	93	38	113	24	1	0	0	0	0	0	0	0	71999.28	61.22	5780.00	4.46
9	53	57.87	0.388	0	1.526	1	562	6234	61.17	37	77	104	113	123	94	39	116	150	1	0	0	0	0	0	0	0	72003.68	61.09	5779.75	4.46
9	53	58.30	0.488	0	1.514	1	559	6231	61.00	40	80	102	115	1	94	40	113	19	1	0	0	0	0	0	0	0	72008.26	60.96	5780.25	4.46
9	53	58.73	0.459	0	1.482	1	554	6230	60.91	41	85	104	117	124	94	40	114	20	1	0	0	0	0	0	0	0	72025.50	60.83	5780.75	4.46
9	53	59.17	0.417	0	1.504	1	550	6229	60.73	42	89	105	118	2	94	40	115	149	1	0	0	0	0	0	0	0	72029.98	60.70	5780.75	4.46
9	53	59.60	0.273	0	1.499	1	546	6229	60.64	42	93	104	118	1	95	40	116	74	1	0	0	0	0	0	0	0	72035.21	60.56	5780.75	4.46
9	54	0.03	0.354	0	1.484	1	544	6228	60.53	43	95	105	119	0	94	40	115	19	1	0	0	0	0	0	0	0	72051.79	60.44	5781.50	4.45
9	54	0.47	0.237	0	1.499	1	539	6226	60.47	45	100	104	121	1	93	38	116	109	1	0	0	0	0	0	0	0	72066.86	60.30	5779.50	4.45
9	54	0.90	0.308	0	1.487	1	536	6225	60.31	46	103	105	122	123	95	41	116	24	1	0	0	0	0	0	0	0	72079.84	60.18	5778.25	4.45
9	54	1.34	0.205	0	1.479	1	532	6223	60.20	48	107	105	123	123	94	43	117	22	1	0	0	0	0	0	0	0	72090.78	60.04	5775.50	4.45
9	54	1.77	0.146	0	1.506	1	530	6222	60.11	49	109	104	123	1	96	42	112	109	1	0	0	0	1	0	0	0	72096.11	59.91	5775.00	4.45
9	54	2.20	0.012	0	1.499	1	523	6221	60.05	50	116	105	2	124	95	40	116	19	1	0	0	0	1	0	0	0	72113.00	59.78	5772.00	4.44
9	54	2.64	-0.068	0	1.455	1	518	6219	59.83	52	121	106	2	124	96	44	113	22	1	0	0	0	1	0	0	0	72120.07	59.65	5772.75	4.44

6-1817

FIGURE 3-3. TYPICAL COMPUTER PRINT OUT

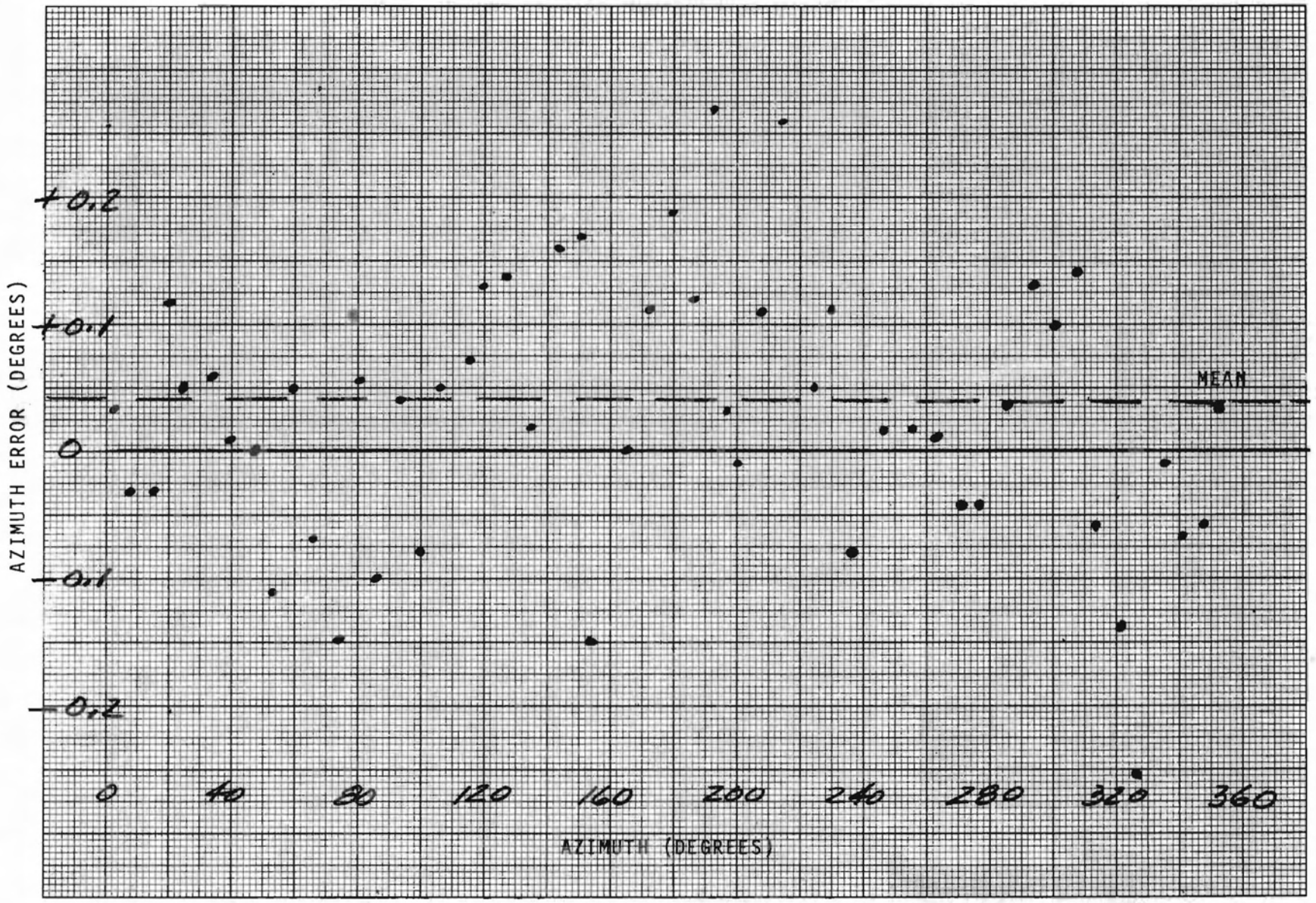


FIGURE 3-4 . 12 MILE ORBIT ERROR CURVE

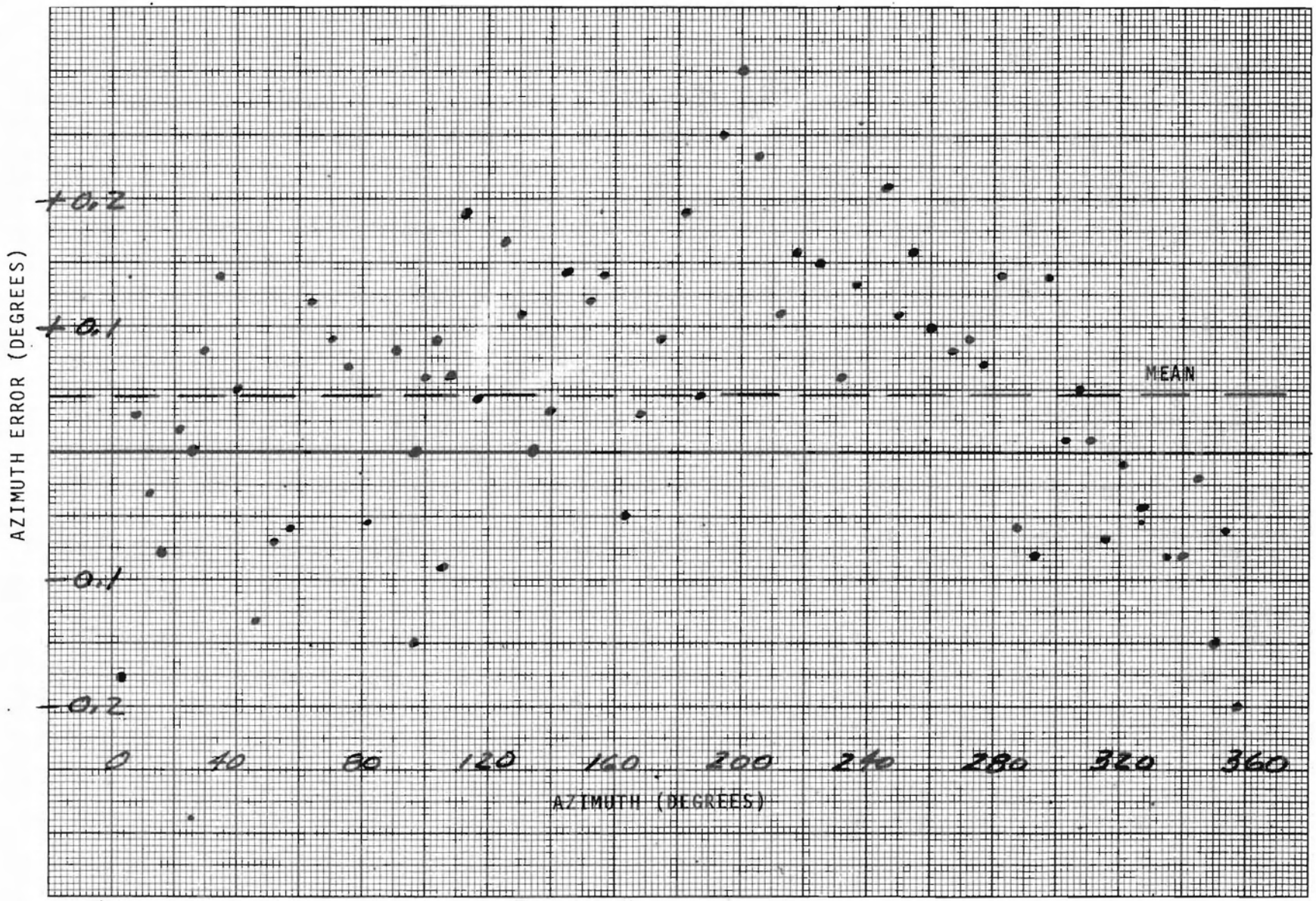


FIGURE 3-5 . 6 MILE ORBIT ERROR CURVE

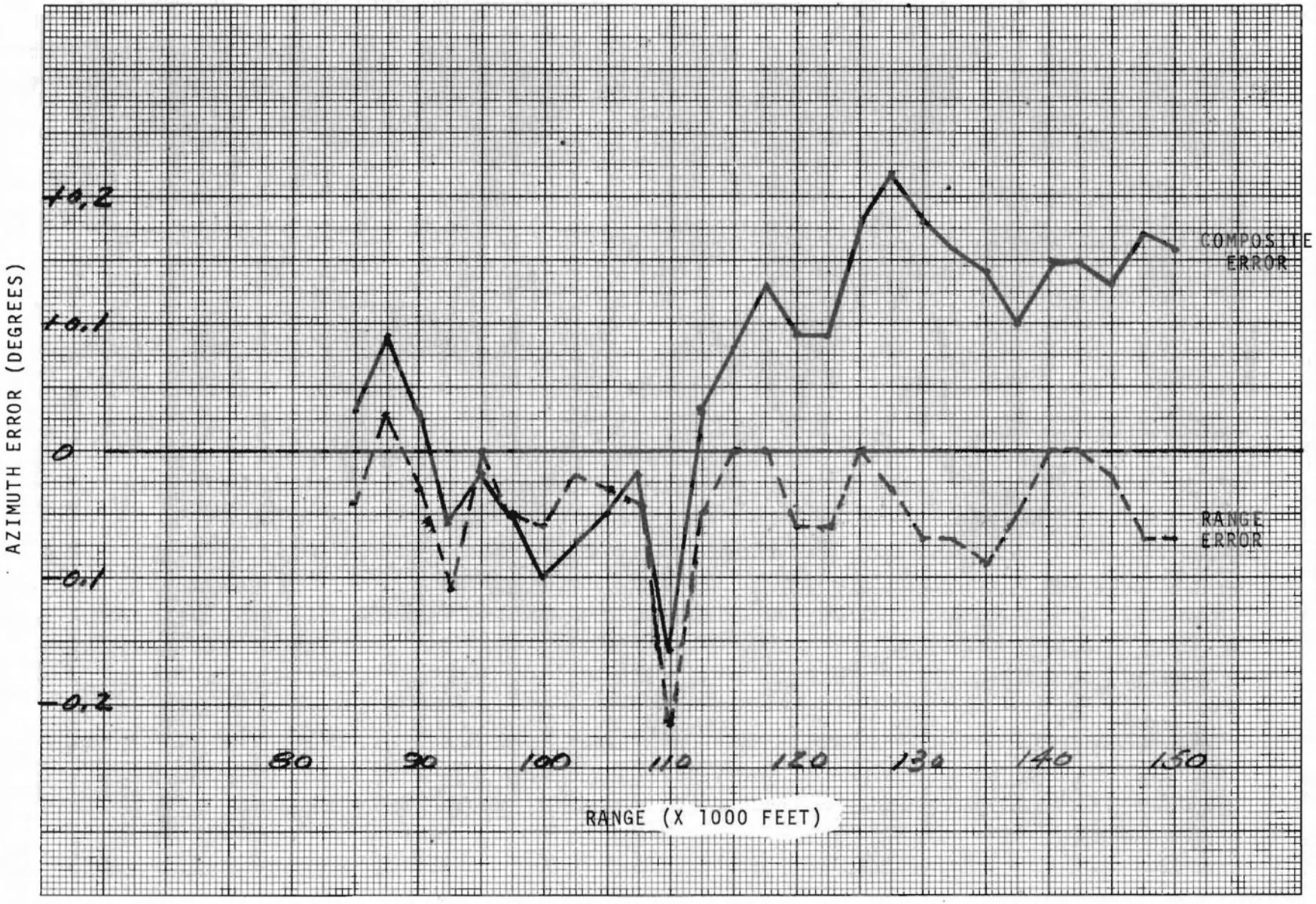


FIGURE 3-6. RADIAL ERROR CURVE

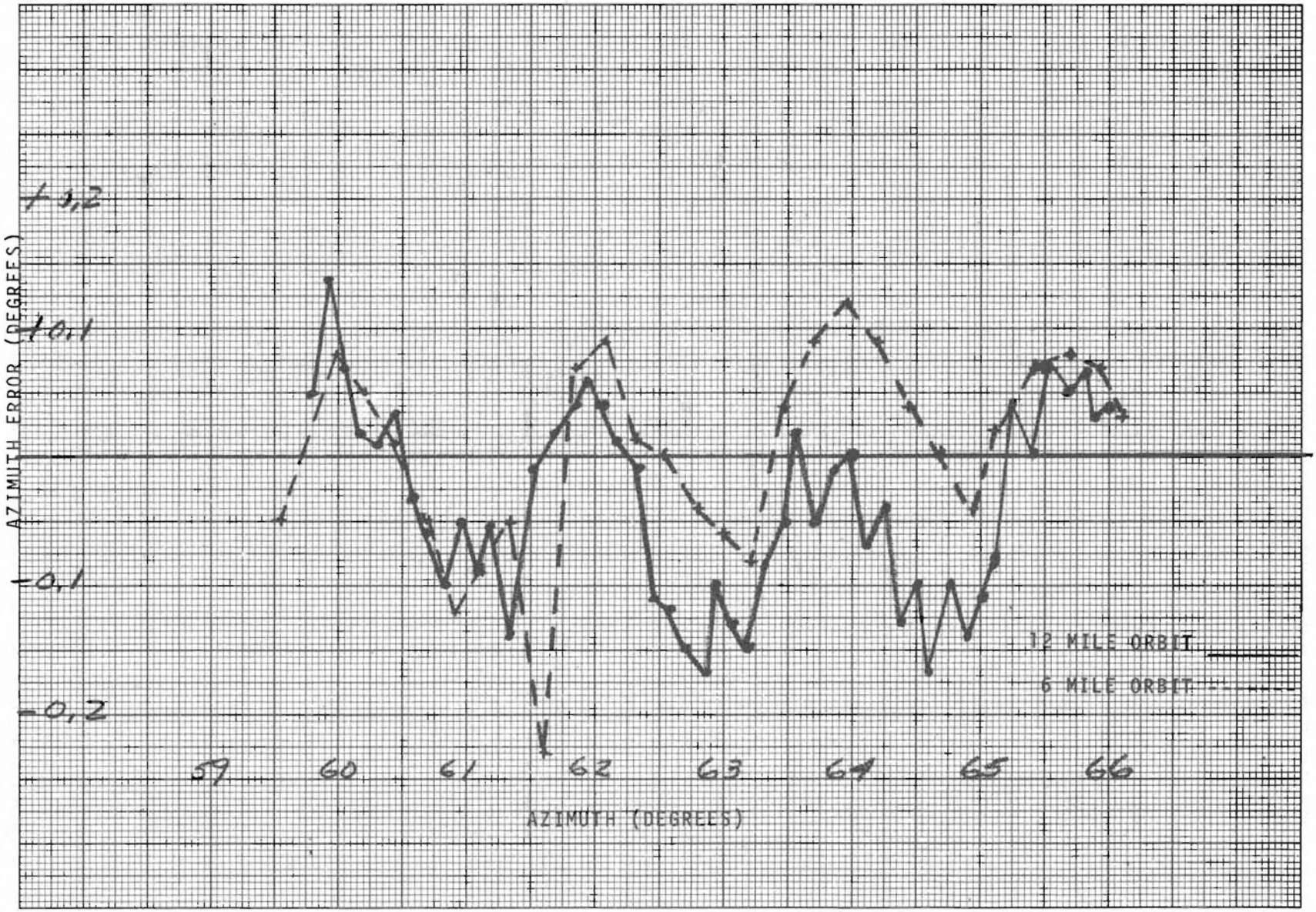


FIGURE 3-7 . 59/66 AZIMUTH SECTOR ERROR CURVE

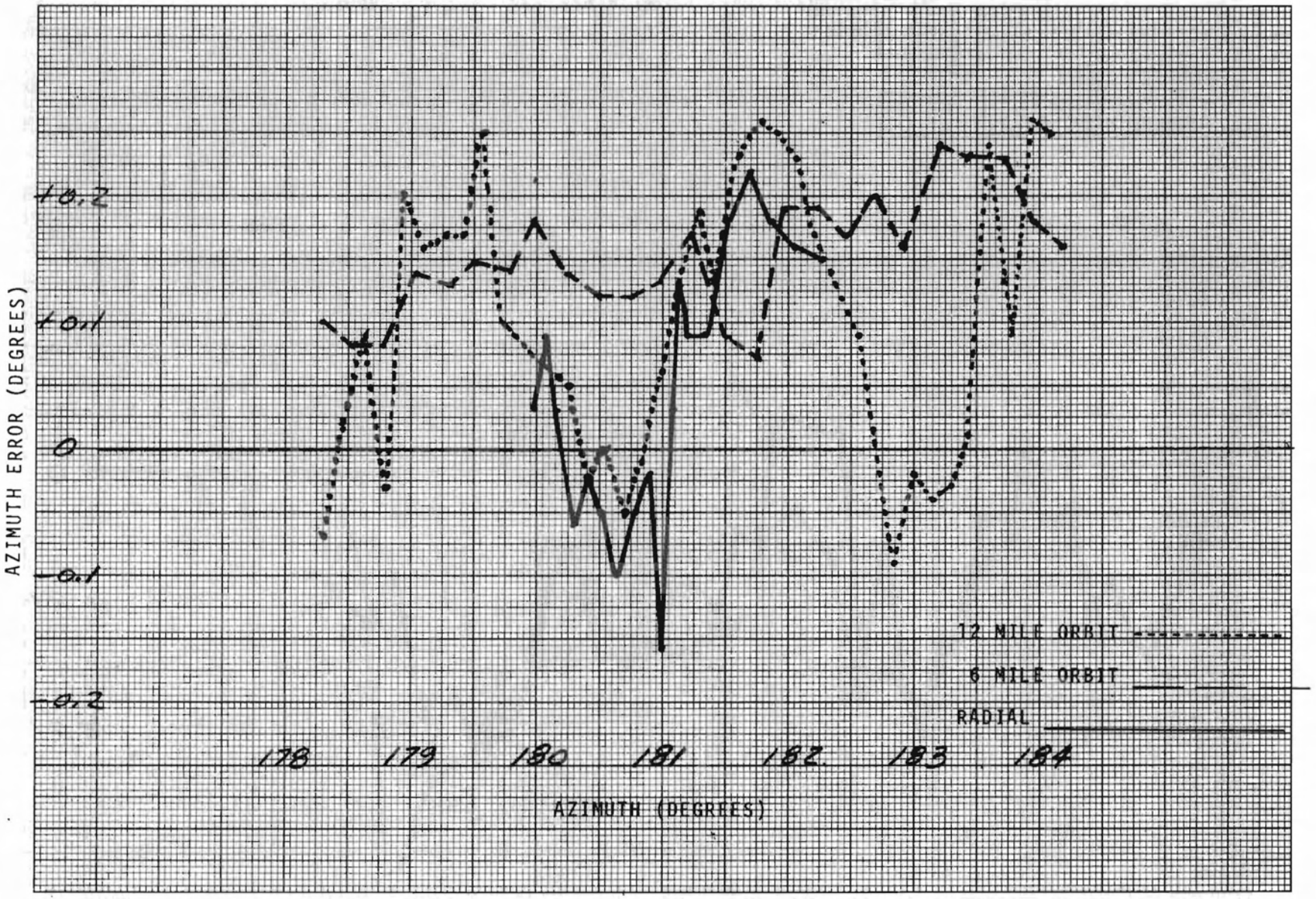


FIGURE 3-8. 178/184 AZIMUTH SECTOR ERROR CURVE

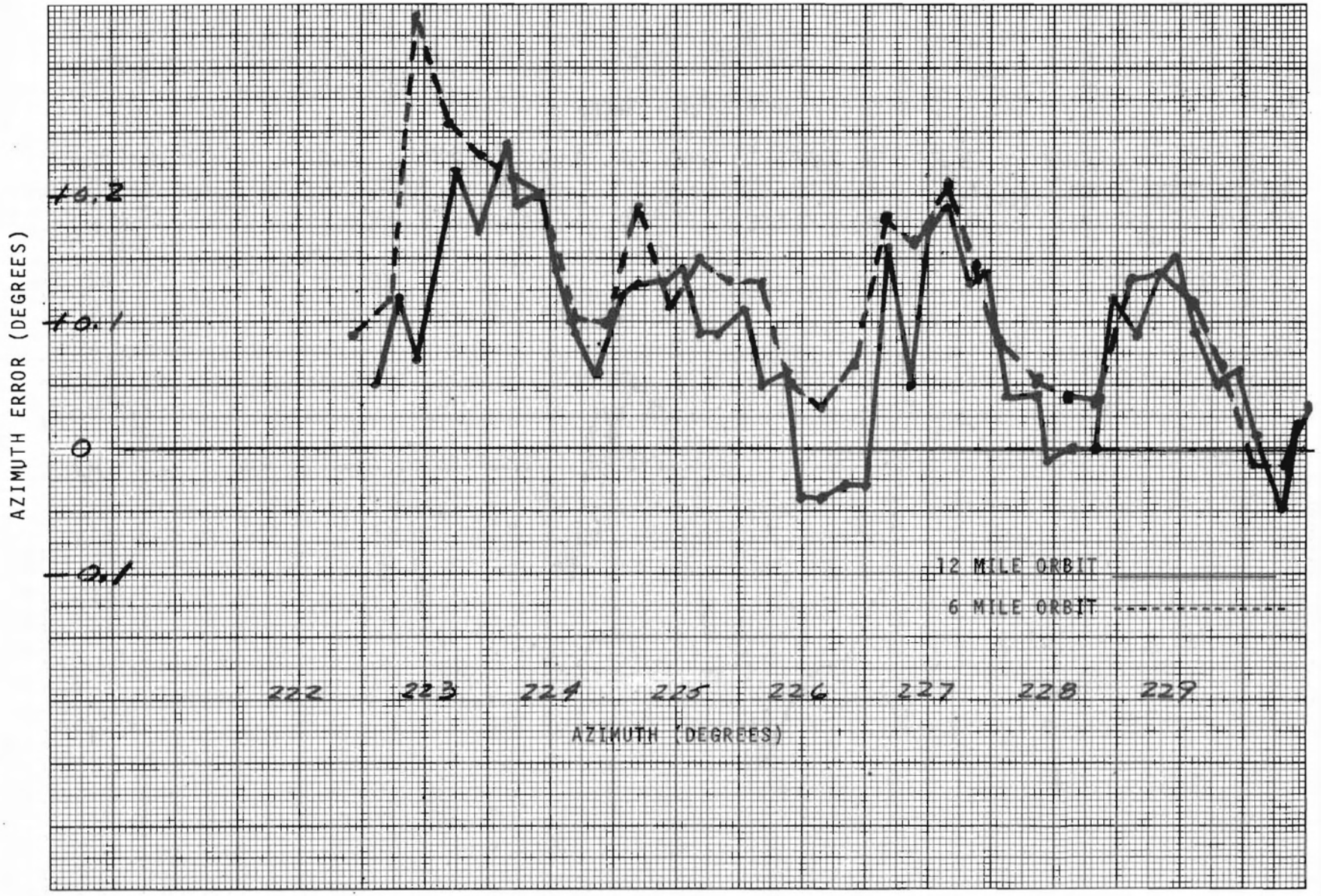


FIGURE 3-9 . 222/229 AZIMUTH SECTOR ERROR CURVE

GPO 912-832